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CHAPTER 1

INTRODUCTION

Chapter 1 - Introduction P14x

1 CHAPTER OVERVIEW

This chapter provides some general information about the technical manual and an introduction to the device(s) described in this technical manual.

This chapter contains the following sections:

Chapter Overview	3
Foreword	4
Product Scope	6
Features and Functions	7
Compliance	10
Functional Overview	11

Chapter 1 - Introduction P14x

2 FOREWORD

This technical manual provides a functional and technical description of General Electric's P141, P142, P143, P144, P145, as well as a comprehensive set of instructions for using the device. The level at which this manual is written assumes that you are already familiar with protection engineering and have experience in this discipline. The description of principles and theory is limited to that which is necessary to understand the product. For further details on general protection engineering theory, we refer you to General Electric's publication NPAG, which is available online or from our contact centre.

We have attempted to make this manual as accurate, comprehensive and user-friendly as possible. However we cannot guarantee that it is free from errors. Nor can we state that it cannot be improved. We would therefore be very pleased to hear from you if you discover any errors, or have any suggestions for improvement. Our policy is to provide the information necessary to help you safely specify, engineer, install, commission, maintain, and eventually dispose of this product. We consider that this manual provides the necessary information, but if you consider that more details are needed, please contact us.

All feedback should be sent to our contact centre via the following URL:

www.gegridsolutions.com/contact

2.1 TARGET AUDIENCE

This manual is aimed towards all professionals charged with installing, commissioning, maintaining, troubleshooting, or operating any of the products within the specified product range. This includes installation and commissioning personnel as well as engineers who will be responsible for operating the product.

The level at which this manual is written assumes that installation and commissioning engineers have knowledge of handling electronic equipment. Also, system and protection engineers have a thorough knowledge of protection systems and associated equipment.

2.2 TYPOGRAPHICAL CONVENTIONS

The following typographical conventions are used throughout this manual.

- The names for special keys appear in capital letters. For example: ENTER
- When describing software applications, menu items, buttons, labels etc as they appear on the screen are written in bold type.
 - For example: Select **Save** from the file menu.
- Filenames and paths use the courier font For example: Example\File.text
- Special terminology is written with leading capitals
 For example: Sensitive Earth Fault
- If reference is made to the IED's internal settings and signals database, the menu group heading (column) text is written in upper case italics
 For example: The SYSTEM DATA column
- If reference is made to the IED's internal settings and signals database, the setting cells and DDB signals are written in bold italics
 - For example: The *Language* cell in the *SYSTEM DATA* column
- If reference is made to the IED's internal settings and signals database, the value of a cell's content is written in the Courier font
 - For example: The *Language* cell in the *SYSTEM DATA* column contains the value *English*

2.3 NOMENCLATURE

Due to the technical nature of this manual, many special terms, abbreviations and acronyms are used throughout the manual. Some of these terms are well-known industry-specific terms while others may be special product-specific terms used by General Electric. The first instance of any acronym or term used in a particular chapter is explained. In addition, a separate glossary is available on the General Electric website, or from the General Electric contact centre.

We would like to highlight the following changes of nomenclature however:

- The word 'relay' is no longer used to describe the device itself. Instead, the device is referred to as the 'IED' (Intelligent Electronic Device), the 'device', or the 'product'. The word 'relay' is used purely to describe the electromechanical components within the device, i.e. the output relays.
- British English is used throughout this manual.
- The British term 'Earth' is used in favour of the American term 'Ground'.

Chapter 1 - Introduction P14x

3 PRODUCT SCOPE

The P14x range of feeder management IEDs has been designed for all applications where overcurrent and earth fault protection is required, from distribution to transmission voltage levels. All devices within the range are suitable for solidly-earthed, impedance-earthed, Petersen coil-earthed and isolated systems.

All devices provide an extensive range of protection functions as well as a comprehensive range of additional features to aid with power system diagnosis and fault analysis.

The P14x range consists of five models; the P141, P142, P143, P144 and P145.

- The P141 is the most basic model providing a cost-effective solution for most applications
- The P142 provides all the functionality of the P141, as well as four-shot three-pole autoreclose functionality.
- The P143 provides all the functionality of the P142, as well as a fourth VT for Check Synchronisation functionality. Due to its choice of larger case sizes, the P143 can also provide significantly more I/O (optoinputs and relay outputs). Model P also provides switch status and control for disconnectors, load break switches and earthing switches.
- The P145 provides all the functionality of the P143, but in addition has 10 function keys for integral scheme or operator control functionality such as circuit breaker control, autoreclose control and remote communications control. This makes it especially suitable where a complete scheme solution is required.
- The P144 has been designed such that it needs just two two Current Transformer inputs for two phases. The
 third phase is derived mathematically inside the IED. It also has a fourth VT input to be used for a measured
 neutral voltage (instead of check sync functionality) which makes it suitable for isolated and compensated
 systems.

The difference in model variants are summarised below:

Model			P14x				
Feature/Variant	P141	P142	P143	P144	P145		
Case	40TE	40TE	60TE/80TE	40Te	60TE		
Number of CT Inputs	5	5	5	4	5		
Number of VT inputs	3	3	4	4	4		
Optically coupled digital inputs	8	16	48	16	32		
Standard relay output contacts	8	15	16	15	32		
Function keys	0	0	0	0	10		
Check synchronisation	N	N	Y	Y	Y		
Autoreclose	N	Υ	Υ	Υ	Υ		
Programmable LEDs (tri-colour)	0	0	0	0	10		

3.1 ORDERING OPTIONS

All current models and variants for this product are defined in an interactive spreadsheet called the CORTEC. This is available on the company website.

Alternatively, you can obtain it via the Contact Centre at the following URL:

www.gegridsolutions.com/contact

A copy of the CORTEC is also supplied as a static table in the Appendices of this document. However, it should only be used for guidance as it provides a snapshot of the interactive data taken at the time of publication.

4 FEATURES AND FUNCTIONS

4.1 PROTECTION FUNCTIONS

The P14x range of devices provides the following protection functions:

ANSI	IEC 61850	Protection Function
37		Undercurrent detection (low load)
46	NgcPTOC	Negative sequence overcurrent
46BC	-	Broken Conductor
49	ThmPTTR	Thermal Overload
50 SOTF		Switch onto Fault
50BF	RBRF	CB Failure
50	OcpPTOC	Definite time overcurrent protection
50N	EfdPTOC	Earth Fault Definite time overcurrent protection Measured and Derived (standard EF CT), Derived (SEF CT)
51	OcpPTOC	IDMT overcurrent protection (stages)
51N	EfdPTOC	Neutral/Ground IDMT overcurrent protection
67	OcpPTOC	Directional Phase Overcurrent
67N	EfdPTOC	Directional Neutral Overcurrent
		Wattmetric Earth Fault
CLP		Cold load pick up
VTS		VT supervision
CTS		CT supervision
64N	RefPDIF	Restricted Earth Fault
		Sensitive Earth Fault (with SEF CT only)
68		2nd Harmonic Blocking
27	VtpPhsPTUV	Undervoltage
47		Negative sequence overvoltage
59	VtpPhsPTOV	Overvoltage
59N	VtpResPTOV	Residual Overvoltage
810	FrqPTOF	Overfrequency
81U	FrqPTUF	Underfrequency
81df/dt		Rate of change of frequency (df/dt)
81V	DfpPFRC	Undervoltage blocking of frequency protection
		Programmable curves
51V		Voltage Controlled Overcurrent
51R		Voltage Restrained Overcurrent
25		Check synchronising
32		Phase Directional Power
		Sensitive power
		Load Encroachment supervision (Load Blinders)
79	RREC	Autoreclose (3 phases)
21FL		Fault Locator
81RF	DfpPFRC	Frequency supervised rate of change of frequency

Chapter 1 - Introduction P14x

ANSI	IEC 61850	Protection Function
81RAV	DfpPFRC	Frequency supervised average rate of change of frequency
81R		Load Restoration
		Rate of change of voltage (dv/dt)
		Blocking scheme
		Programmable curves
		High Impedance Earth Fault
		CB Monitoring
86		Latching output contacts (Lockout)

4.2 CONTROL FUNCTIONS

Feature	IEC 61850	ANSI
Watchdog contacts		
Read-only mode		
Function keys	FnkGGIO	
Programmable LEDs	LedGGIO	
Programmable hotkeys		
Programmable allocation of digital inputs and outputs		
Fully customizable menu texts		
Circuit breaker control, status & condition monitoring	XCBR	52
CT supervision		
VT supervision		
Trip circuit and coil supervision		
Control inputs	PloGGIO1	
Power-up diagnostics and continuous self-monitoring		
Dual rated 1A and 5A CT inputs		
Alternative setting groups (4)		
Graphical programmable scheme logic (PSL)		
Fault locator	RFLO	

4.3 MEASUREMENT FUNCTIONS

Measurement Function	IEC 61850	ANSI
Measurement of all instantaneous & integrated values (Exact range of measurements depend on the device model)		MET
Disturbance recorder for waveform capture – specified in samples per cycle	RDRE	DFR
Fault Records		
Maintenance Records		
Event Records / Event logging		Event records
Time Stamping of Opto-inputs	Yes	Yes

4.4 COMMUNICATION FUNCTIONS

The device offers the following communication functions:

Feature	ANSI
NERC compliant cyber-security	
Front RS232 serial communication port for configuration	16S
Rear serial RS485 communication port for SCADA control	16S
2nd Additional rear serial communication ports for SCADA control and teleprotection (fibre and copper) (optional)	16S
Ethernet communication (optional)	16E
Redundant Ethernet communication (optional)	16E
Courier protocol	16S
IEC 61850 protocol (optional)	16E
IEC 60870-5-103 protocol (optional)	16S
Modbus protocol (optional)	16S
DNP3.0 protocol over serial link (optional)	16S
DNP3.0 protocol over Ethernet (optional)	16E
IRIG-B time synchronisation (optional)	CLK

Chapter 1 - Introduction P14x

5 COMPLIANCE

The device has undergone a range of extensive testing and certification processes to ensure and prove compatibility with all target markets. A detailed description of these criteria can be found in the Technical Specifications chapter.

6 FUNCTIONAL OVERVIEW

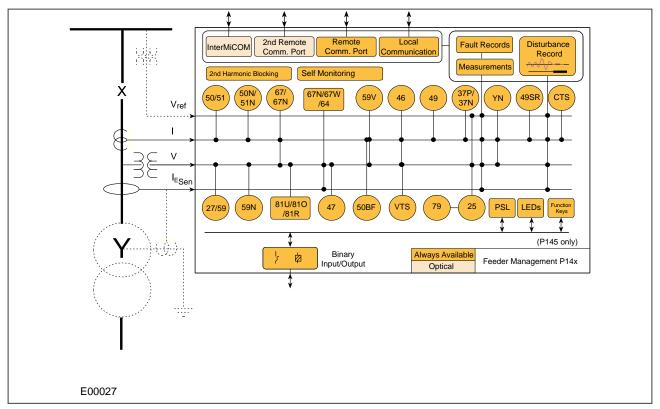


Figure 1: Functional Overview

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CHAPTER 2

SAFETY INFORMATION

1 CHAPTER OVERVIEW

This chapter provides information about the safe handling of the equipment. The equipment must be properly installed and handled in order to maintain it in a safe condition and to keep personnel safe at all times. You must be familiar with information contained in this chapter before unpacking, installing, commissioning, or servicing the equipment.

This chapter contains the following sections:

Chapter Overview	15
Health and Safety	16
Symbols	17
Installation, Commissioning and Servicing	18
Decommissioning and Disposal	23
Regulatory Compliance	24

2 HEALTH AND SAFETY

Personnel associated with the equipment must be familiar with the contents of this Safety Information.

When electrical equipment is in operation, dangerous voltages are present in certain parts of the equipment. Improper use of the equipment and failure to observe warning notices will endanger personnel.

Only qualified personnel may work on or operate the equipment. Qualified personnel are individuals who are:

- familiar with the installation, commissioning, and operation of the equipment and the system to which it is being connected.
- familiar with accepted safety engineering practises and are authorised to energise and de-energise equipment in the correct manner.
- trained in the care and use of safety apparatus in accordance with safety engineering practises
- trained in emergency procedures (first aid).

The documentation provides instructions for installing, commissioning and operating the equipment. It cannot, however cover all conceivable circumstances. In the event of questions or problems, do not take any action without proper authorisation. Please contact your local sales office and request the necessary information.

3 SYMBOLS

Throughout this manual you will come across the following symbols. You will also see these symbols on parts of the equipment.



Caution:

Refer to equipment documentation. Failure to do so could result in damage to the equipment



Warning:

Risk of electric shock



Earth terminal. Note: This symbol may also be used for a protective conductor (earth) terminal if that terminal is part of a terminal block or sub-assembly.



Protective conductor (earth) terminal



Instructions on disposal requirements

Note:

The term 'Earth' used in this manual is the direct equivalent of the North American term 'Ground'.

4 INSTALLATION, COMMISSIONING AND SERVICING

4.1 LIFTING HAZARDS

Many injuries are caused by:

- Lifting heavy objects
- Lifting things incorrectly
- Pushing or pulling heavy objects
- Using the same muscles repetitively

Plan carefully, identify any possible hazards and determine how best to move the product. Look at other ways of moving the load to avoid manual handling. Use the correct lifting techniques and Personal Protective Equipment (PPE) to reduce the risk of injury.

4.2 ELECTRICAL HAZARDS



Caution:

All personnel involved in installing, commissioning, or servicing this equipment must be familiar with the correct working procedures.



Caution:

Consult the equipment documentation before installing, commissioning, or servicing the equipment.



Caution:

Always use the equipment as specified. Failure to do so will jeopardise the protection provided by the equipment.



Warning:

Removal of equipment panels or covers may expose hazardous live parts. Do not touch until the electrical power is removed. Take care when there is unlocked access to the rear of the equipment.



Warning:

Isolate the equipment before working on the terminal strips.



Warning:

Use a suitable protective barrier for areas with restricted space, where there is a risk of electric shock due to exposed terminals.



Caution:

Disconnect power before disassembling. Disassembly of the equipment may expose sensitive electronic circuitry. Take suitable precautions against electrostatic voltage discharge (ESD) to avoid damage to the equipment.



Caution:

NEVER look into optical fibres or optical output connections. Always use optical power meters to determine operation or signal level.



Warning:

Testing may leave capacitors charged to dangerous voltage levels. Discharge capacitors by reducing test voltages to zero before disconnecting test leads.



Caution:

Operate the equipment within the specified electrical and environmental limits.



Caution:

Before cleaning the equipment, ensure that no connections are energised. Use a lint free cloth dampened with clean water.

Note:

Contact fingers of test plugs are normally protected by petroleum jelly, which should not be removed.

4.3 UL/CSA/CUL REQUIREMENTS

The information in this section is applicable only to equipment carrying UL/CSA/CUL markings.



Caution:

Equipment intended for rack or panel mounting is for use on a flat surface of a Type 1 enclosure, as defined by Underwriters Laboratories (UL).



Caution:

To maintain compliance with UL and CSA/CUL, install the equipment using UL/CSA-recognised parts for: cables, protective fuses, fuse holders and circuit breakers, insulation crimp terminals, and replacement internal batteries.

4.4 FUSING REQUIREMENTS



Caution:

Where UL/CSA listing of the equipment is required for external fuse protection, a UL or CSA Listed fuse must be used for the auxiliary supply. The listed protective fuse type is: Class J time delay fuse, with a maximum current rating of 15 A and a minimum DC rating of 250 V dc (for example type AJT15).



Caution:

Where UL/CSA listing of the equipment is not required, a high rupture capacity (HRC) fuse type with a maximum current rating of 16 Amps and a minimum dc rating of 250 V dc may be used for the auxiliary supply (for example Red Spot type NIT or TIA). For P50 models, use a 1A maximum T-type fuse.

For P60 models, use a 4A maximum T-type fuse.



Caution:

Digital input circuits should be protected by a high rupture capacity NIT or TIA fuse with maximum rating of 16 A. for safety reasons, current transformer circuits must never be fused. Other circuits should be appropriately fused to protect the wire used.



Caution:

CTs must NOT be fused since open circuiting them may produce lethal hazardous voltages

4.5 EQUIPMENT CONNECTIONS



Warnina:

Terminals exposed during installation, commissioning and maintenance may present a hazardous voltage unless the equipment is electrically isolated.



Caution:

Tighten M4 clamping screws of heavy duty terminal block connectors to a nominal torque of 1.3 Nm.

Tighten captive screws of terminal blocks to 0.5 Nm minimum and 0.6 Nm maximum.



Caution:

Always use insulated crimp terminations for voltage and current connections.



Caution:

Always use the correct crimp terminal and tool according to the wire size.



Caution:

Watchdog (self-monitoring) contacts are provided to indicate the health of the device on some products. We strongly recommend that you hard wire these contacts into the substation's automation system, for alarm purposes.

4.6 PROTECTION CLASS 1 EQUIPMENT REQUIREMENTS



Caution:

Earth the equipment with the supplied PCT (Protective Conductor Terminal).



Caution:

Do not remove the PCT.



Caution:

The PCT is sometimes used to terminate cable screens. Always check the PCT's integrity after adding or removing such earth connections.



Caution:

Use a locknut or similar mechanism to ensure the integrity of stud-connected PCTs.



Caution:

The recommended minimum PCT wire size is 2.5 mm² for countries whose mains supply is 230 V (e.g. Europe) and 3.3 mm² for countries whose mains supply is 110 V (e.g. North America). This may be superseded by local or country wiring regulations.

For P60 products, the recommended minimum PCT wire size is 6 mm². See product documentation for details.



Caution:

The PCT connection must have low-inductance and be as short as possible.



Caution:

All connections to the equipment must have a defined potential. Connections that are pre-wired, but not used, should be earthed, or connected to a common grouped potential.

4.7 PRE-ENERGISATION CHECKLIST



Caution:

Check voltage rating/polarity (rating label/equipment documentation).



Caution:

Check CT circuit rating (rating label) and integrity of connections.



Caution:

Check protective fuse or miniature circuit breaker (MCB) rating.



Caution:

Check integrity of the PCT connection.



Caution

Check voltage and current rating of external wiring, ensuring it is appropriate for the application.

4.8 PERIPHERAL CIRCUITRY



Warning:

Do not open the secondary circuit of a live CT since the high voltage produced may be lethal to personnel and could damage insulation. Short the secondary of the line CT before opening any connections to it.

Note:

For most General Electric equipment with ring-terminal connections, the threaded terminal block for current transformer termination is automatically shorted if the module is removed. Therefore external shorting of the CTs may not be required. Check the equipment documentation and wiring diagrams first to see if this applies.



Caution:

Where external components such as resistors or voltage dependent resistors (VDRs) are used, these may present a risk of electric shock or burns if touched.



Warning:

Take extreme care when using external test blocks and test plugs such as the MMLG, MMLB and P990, as hazardous voltages may be exposed. Ensure that CT shorting links are in place before removing test plugs, to avoid potentially lethal voltages.

4.9 UPGRADING/SERVICING



Warning:

Do not insert or withdraw modules, PCBs or expansion boards from the equipment while energised, as this may result in damage to the equipment. Hazardous live voltages would also be exposed, endangering personnel.



Caution:

Internal modules and assemblies can be heavy and may have sharp edges. Take care when inserting or removing modules into or out of the IED.

5

DECOMMISSIONING AND DISPOSAL



Caution:

Before decommissioning, completely isolate the equipment power supplies (both poles of any dc supply). The auxiliary supply input may have capacitors in parallel, which may still be charged. To avoid electric shock, discharge the capacitors using the external terminals before decommissioning.



Caution:

Avoid incineration or disposal to water courses. Dispose of the equipment in a safe, responsible and environmentally friendly manner, and if applicable, in accordance with country-specific regulations.

6 REGULATORY COMPLIANCE

Compliance with the European Commission Directive on EMC and LVD is demonstrated using a technical file.



6.1 EMC COMPLIANCE: 2014/30/EU

The product specific Declaration of Conformity (DoC) lists the relevant harmonised standard(s) or conformity assessment used to demonstrate compliance with the EMC directive.

6.2 LVD COMPLIANCE: 2014/35/EU

The product specific Declaration of Conformity (DoC) lists the relevant harmonized standard(s) or conformity assessment used to demonstrate compliance with the LVD directive.

Safety related information, such as the installation I overvoltage category, pollution degree and operating temperature ranges are specified in the Technical Data section of the relevant product documentation and/or on the product labelling.

Unless otherwise stated in the Technical Data section of the relevant product documentation, the equipment is intended for indoor use only. Where the equipment is required for use in an outdoor location, it must be mounted in a specific cabinet or housing to provide the equipment with the appropriate level of protection from the expected outdoor environment.

6.3 R&TTE COMPLIANCE: 2014/53/EU

Radio and Telecommunications Terminal Equipment (R&TTE) directive 2014/53/EU.

Conformity is demonstrated by compliance to both the EMC directive and the Low Voltage directive, to zero volts.

6.4 UL/CUL COMPLIANCE

If marked with this logo, the product is compliant with the requirements of the Canadian and USA Underwriters Laboratories.

The relevant UL file number and ID is shown on the equipment.



6.5 ATEX COMPLIANCE: 2014/34/EU

Products marked with the 'explosion protection' Ex symbol (shown in the example, below) are compliant with the ATEX directive. The product specific Declaration of Conformity (DoC) lists the Notified Body, Type Examination Certificate, and relevant harmonized standard or conformity assessment used to demonstrate compliance with the ATEX directive.

The ATEX Equipment Protection level, Equipment group, and Zone definition will be marked on the product.

For example:



Where:

'II' Equipment Group: Industrial.

'(2)G' High protection equipment category, for control of equipment in gas atmospheres in Zone 1 and 2. This equipment (with parentheses marking around the zone number) is not itself suitable for operation

within a potentially explosive atmosphere.

CHAPTER 3

HARDWARE DESIGN

1 CHAPTER OVERVIEW

This chapter provides information about the product's hardware design.

This chapter contains the following sections:	
Chapter Overview	29
Hardware Architecture	30
Mechanical Implementation	31
Front Panel	33
Rear Panel	37
Terminal Block Ingress Protection	39
Boards and Modules	40

2 HARDWARE ARCHITECTURE

The main components comprising devices based on the Px4x platform are as follows:

- The housing, consisting of a front panel and connections at the rear
- The Main processor module consisting of the main CPU (Central Processing Unit), memory and an interface to the front panel HMI (Human Machine Interface)
- A selection of plug-in boards and modules with presentation at the rear for the power supply, communication functions, digital I/O, analogue inputs, and time synchronisation connectivity

All boards and modules are connected by a parallel data and address bus, which allows the processor module to send and receive information to and from the other modules as required. There is also a separate serial data bus for conveying sampled data from the input module to the CPU. These parallel and serial databuses are shown as a single interconnection module in the following figure, which shows typical modules and the flow of data between them.

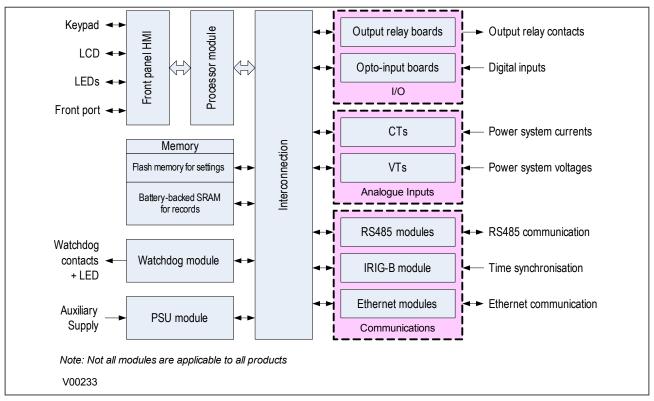


Figure 2: Hardware architecture

3 MECHANICAL IMPLEMENTATION

All products based on the Px4x platform have common hardware architecture. The hardware is modular and consists of the following main parts:

- Case and terminal blocks
- Boards and modules
- Front panel

The case comprises the housing metalwork and terminal blocks at the rear. The boards fasten into the terminal blocks and are connected together by a ribbon cable. This ribbon cable connects to the processor in the front panel.

The following diagram shows an exploded view of a typical product. The diagram shown does not necessarily represent exactly the product model described in this manual.

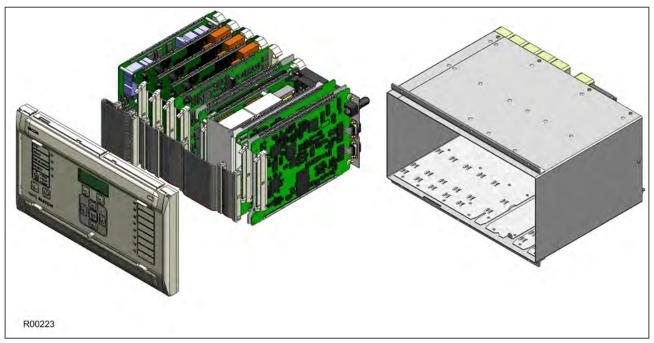


Figure 3: Exploded view of IED

3.1 HOUSING VARIANTS

The Px4x range of products are implemented in a range of case sizes. Case dimensions for industrial products usually follow modular measurement units based on rack sizes. These are: U for height and TE for width, where:

- 1U = 1.75 inches = 44.45 mm
- 1TE = 0.2 inches = 5.08 mm

The products are available in panel-mount or standalone versions. All products are nominally 4U high. This equates to 177.8 mm or 7 inches.

The cases are pre-finished steel with a conductive covering of aluminium and zinc. This provides good grounding at all joints, providing a low resistance path to earth that is essential for performance in the presence of external noise.

The case width depends on the product type and its hardware options. There are three different case widths for the described range of products: 40TE, 60TE and 80TE. The case dimensions and compatibility criteria are as follows:

Case width (TE)	Case width (mm)	Case width (inches)
40TE	203.2	8
60TE	304.8	12
80TE	406.4	16

Note:

Not all case sizes are available for all models.

3.2 LIST OF BOARDS

The product's hardware consists of several modules drawn from a standard range. The exact specification and number of hardware modules depends on the model number and variant. Depending on the exact model, the product in question will use a selection of the following boards.

Board	Use
Main Processor board – 40TE or smaller	Main Processor board – without support for function keys
Main Processor board – 60TE or larger	Main Processor board – with support for function keys
Power supply board 24/54V DC	Power supply input. Accepts DC voltage between 24V and 54V
Power supply board - 48/125V DC	Power supply input. Accepts DC voltage between 48V and 125V
Power supply board 110/250V DC	Power supply input. Accepts DC voltage between 110V and 125V
Transformer board	Contains the voltage and current transformers
Input board	Contains the A/D conversion circuitry
Input board with opto-inputs	Contains the A/D conversion circuitry + 8 digital opto-inputs
IRIG-B board - modulated	Interface board for modulated IRIG-B timing signal
IRIG-B - demodulated input	Interface board for demodulated IRIG-B timing signal
Fibre board	Interface board for fibre-based RS485 connection
Fibre + IRIG-B	Interface board for fibre-based RS485 connection + demodulated IRIG-B
2nd rear communications board	Interface board for RS232 / RS485 connections
2nd rear communications board with IRIG-B input	Interface board for RS232 / RS485 + IRIG-B connections
100MhZ Ethernet board	Standard 100MHz Ethernet board for LAN connection (fibre + copper)
100MhZ Ethernet board with modulated IRIG-B	Standard 100MHz Ethernet board (fibre / copper) + modulated IRIG-B
100MhZ Ethernet board with demodulated IRIG-B	Standard 100MHz Ethernet board (fibre / copper)+ demodulated IRIG-B
Redundant Ethernet SHP + modulated IRIG-B	Redundant SHP Ethernet board (2 fibre ports) + modulated IRIG-B input
Redundant Ethernet SHP + demodulated IRIG-B	Redundant SHP Ethernet board (2 fibre ports) + demodulated IRIG-B input
Redundant Ethernet RSTP + modulated IRIG-B	Redundant RSTP Ethernet board (2 fibre ports) + modulated IRIG-B input
Redundant Ethernet RSTP+ demodulated IRIG-B	Redundant RSTP Ethernet board (2 fibre ports) + demodulated IRIG-B input
Redundant Ethernet DHP + modulated IRIG-B	Redundant DHP Ethernet board (2 fibre ports) + modulated IRIG-B input
Redundant Ethernet DHP + demodulated IRIG-B	Redundant DHP Ethernet board (2 fibre ports) + demodulated IRIG-B input
Redundant Ethernet PRP + modulated IRIG-B	Redundant PRP Ethernet board (2 fibre ports) + modulated IRIG-B input
Redundant Ethernet PRP + demodulated IRIG-B	Redundant PRP Ethernet board (2 fibre ports) + demodulated IRIG-B input
Redundant Ethernet HSR + modulated IRIG-B	Redundant HSREthernet board (2 fibre ports) + modulated IRIG-B input
Redundant Ethernet HSR + demodulated IRIG-B	Redundant HRSEthernet board (2 fibre ports) + demodulated IRIG-B input
Output relay output board (8 outputs)	Standard output relay board with 8 outputs

4 FRONT PANEL

4.1 FRONT PANEL

Depending on the exact model and chosen options, the product will be housed in either a 40TE, 60TE or 80TE case. By way of example, the following diagram shows the front panel of a typical 60TE unit. The front panels of the products based on 40TE and 80TE cases have a lot of commonality and differ only in the number of hotkeys and user-programmable LEDs. The hinged covers at the top and bottom of the front panel are shown open. An optional transparent front cover physically protects the front panel.

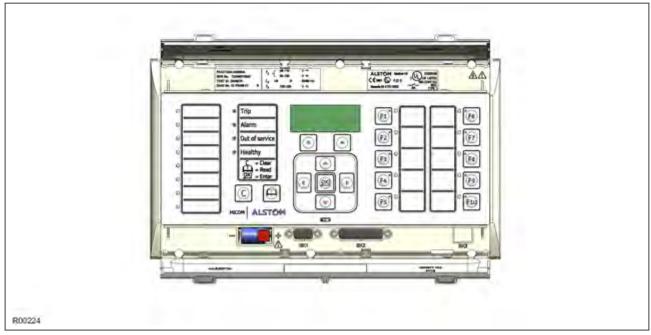


Figure 4: Front panel (60TE)

The front panel consists of:

- Top and bottom compartments with hinged cover
- LCD display
- Keypad
- 9 pin D-type serial port
- 25 pin D-type parallel port
- Fixed function LEDs
- Function keys and LEDs (60TE and 80TE models)
- Programmable LEDs (60TE and 80TE models)

4.1.1 FRONT PANEL COMPARTMENTS

The top compartment contains labels for the:

- Serial number
- Current and voltage ratings.

The bottom compartment contains:

- A compartment for a 1/2 AA size backup battery (used to back up the real time clock and event, fault, and disturbance records).
- A 9-pin female D-type front port for an EIA(RS)232 serial connection to a PC.
- A 25-pin female D-type parallel port for monitoring internal signals and downloading software and language text.

4.1.2 HMI PANEL

The keypad provides full access to the device functionality using a range of menu options. The information is displayed on the LCD. The LCD is a high resolution monochrome display with 16 characters by 3 lines and controllable back light.

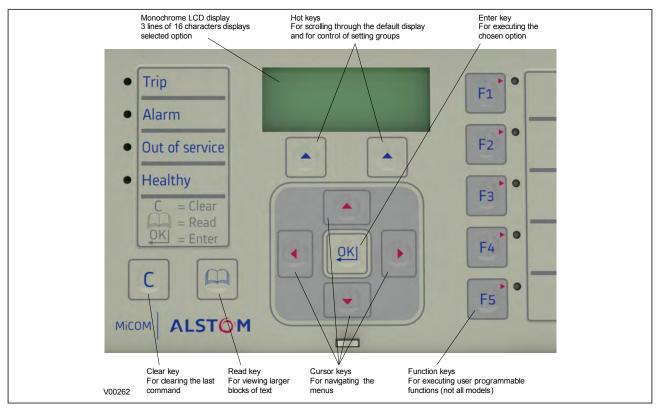


Figure 5: HMI panel

Note

As the LCD display has a resolution of 16 characters by 3 lines, some of the information is in a condensed mnemonic form.

4.1.3 FRONT SERIAL PORT (SK1)

The front serial port is a 9-pin female D-type connector, providing RS232 serial data communication. It is situated under the bottom hinged cover, and is used to communicate with a locally connected PC. It is used to transfer settings data between the PC and the IED.

The port is intended for temporary connection during testing, installation and commissioning. It is not intended to be used for permanent SCADA communications. This port supports the Courier communication protocol only. Courier is a proprietary communication protocol to allow communication with a range of protection equipment, and between the device and the Windows-based support software package.

This port can be considered as a DCE (Data Communication Equipment) port, so you can connect this port device to a PC with an EIA(RS)232 serial cable up to 15 m in length.

The inactivity timer for the front port is set to 15 minutes. This controls how long the unit maintains its level of password access on the front port. If no messages are received on the front port for 15 minutes, any password access level that has been enabled is cancelled.

Note:

The front serial port does not support automatic extraction of event and disturbance records, although this data can be accessed manually.

4.1.3.1 FRONT SERIAL PORT (SK1) CONNECTIONS

The port pin-out follows the standard for Data Communication Equipment (DCE) device with the following pin connections on a 9-pin connector.

	Pin number	Description
2		Tx Transmit data
3		Rx Receive data
5		0 V Zero volts common

You must use the correct serial cable, or the communication will not work. A straight-through serial cable is required, connecting pin 2 to pin 2, pin 3 to pin 3, and pin 5 to pin 5.

Once the physical connection from the unit to the PC is made, the PC's communication settings must be set to match those of the IED. The following table shows the unit's communication settings for the front port.

Protocol	Courier
Baud rate	19,200 bps
Courier address	1
Message format	11 bit - 1 start bit, 8 data bits, 1 parity bit (even parity), 1 stop bit

4.1.4 FRONT PARALLEL PORT (SK2)

The front parallel port uses a 25 pin D-type connector. It is used for commissioning, downloading firmware updates and menu text editing.

4.1.5 FIXED FUNCTION LEDS

Four fixed-function LEDs on the left-hand side of the front panel indicate the following conditions.

- Trip (Red) switches ON when the IED issues a trip signal. It is reset when the associated fault record is cleared from the front display. Also the trip LED can be configured as self-resetting.
- Alarm (Yellow) flashes when the IED registers an alarm. This may be triggered by a fault, event or maintenance record. The LED flashes until the alarms have been accepted (read), then changes to constantly ON. When the alarms are cleared, the LED switches OFF.
- Out of service (Yellow) is ON when the IED's functions are unavailable.
- Healthy (Green) is ON when the IED is in correct working order, and should be ON at all times. It goes OFF if
 the unit's self-tests show there is an error in the hardware or software. The state of the healthy LED is
 reflected by the watchdog contacts at the back of the unit.

4.1.6 FUNCTION KEYS

The programmable function keys are available for custom use for some models.

Factory default settings associate specific functions to these keys, but by using programmable scheme logic, you can change the default functions of these keys to fit specific needs. Adjacent to these function keys are programmable LEDs, which are usually set to be associated with their respective function keys.

4.1.7 PROGRAMABLE LEDS

The device has a number of programmable LEDs, which can be associated with PSL-generated signals. The programmable LEDs for most models are tri-colour and can be set to RED, YELLOW or GREEN. However the programmable LEDs for some models are single-colour (red) only. The single-colour LEDs can be recognised by virtue of the fact they are large and slightly oval, whereas the tri-colour LEDs are small and round.

5 REAR PANEL

The MiCOM Px40 series uses a modular construction. Most of the internal workings are on boards and modules which fit into slots. Some of the boards plug into terminal blocks, which are bolted onto the rear of the unit. However, some boards such as the communications boards have their own connectors. The rear panel consists of these terminal blocks plus the rears of the communications boards.

The back panel cut-outs and slot allocations vary. This depends on the product, the type of boards and the terminal blocks needed to populate the case. The following diagram shows a typical rear view of a case populated with various boards.

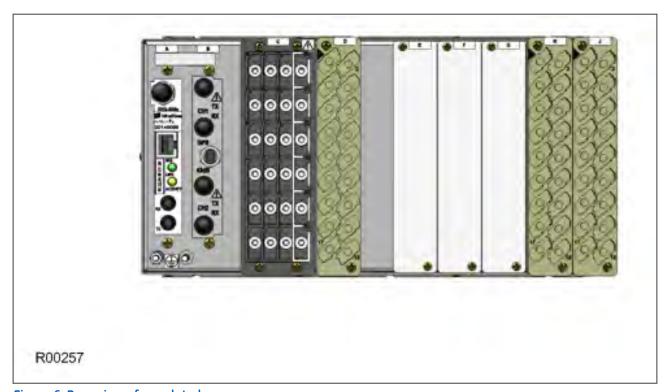


Figure 6: Rear view of populated case

Note

This diagram is just an example and may not show the exact product described in this manual. It also does not show the full range of available boards, just a typical arrangement.

Not all slots are the same size. The slot width depends on the type of board or terminal block. For example, HD (heavy duty) terminal blocks, as required for the analogue inputs, require a wider slot size than MD (medium duty) terminal blocks. The board positions are not generally interchangeable. Each slot is designed to house a particular type of board. Again, this is model-dependent.

The device may use one or more of the terminal block types shown in the following diagram. The terminal blocks are fastened to the rear panel with screws.

- Heavy duty (HD) terminal blocks for CT and VT circuits
- Medium duty (MD) terminal blocks for the power supply, opto-inputs, relay outputs and rear communications port
- RTD/CLIO terminal block for connection to analogue transducers

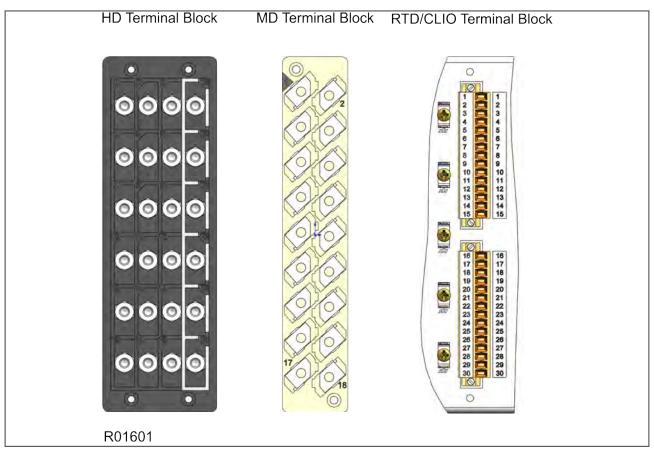


Figure 7: Terminal block types

Note:

Not all products use all types of terminal blocks. The product described in this manual may use one or more of the above types.

6 TERMINAL BLOCK INGRESS PROTECTION

IP2x shields and side cover panels are designed to provide IP20 ingress protection for MiCOM terminal blocks. The shields and covers may be attached during installation or retrofitted to upgrade existing installations—see figure below. For more information, contact your local sales office or our worldwide Contact Centre.

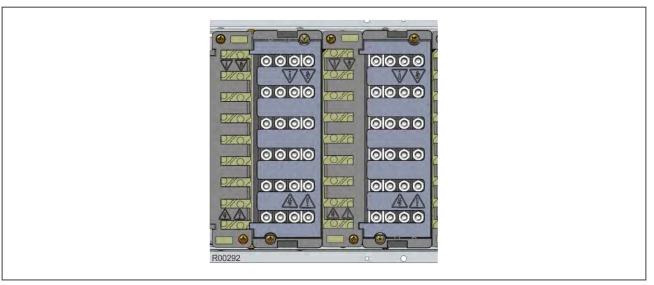


Figure 8: Example—fitted IP2x shields (cabling omitted for clarity)

7 BOARDS AND MODULES

Each product comprises a selection of PCBs (Printed Circuit Boards) and subassemblies, depending on the chosen configuration.

7.1 PCBS

A PCB typically consists of the components, a front connector for connecting into the main system parallel bus via a ribbon cable, and an interface to the rear. This rear interface may be:

- Directly presented to the outside world (as is the case for communication boards such as Ethernet Boards)
- Presented to a connector, which in turn connects into a terminal block bolted onto the rear of the case (as is the case for most of the other board types)

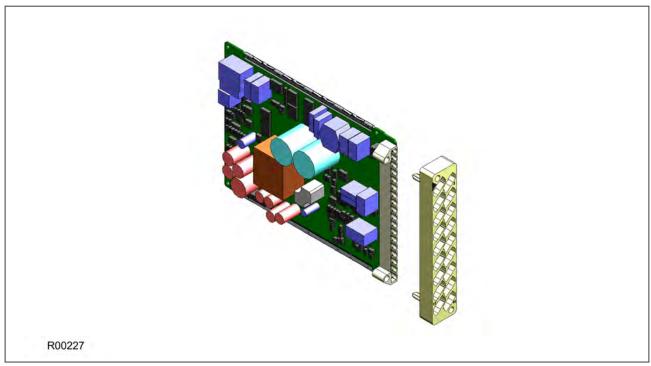


Figure 9: Rear connection to terminal block

7.2 SUBASSEMBLIES

A sub-assembly consists of two or more boards bolted together with spacers and connected with electrical connectors. It may also have other special requirements such as being encased in a metal housing for shielding against electromagnetic radiation.

Boards are designated by a part number beginning with ZN, whereas pre-assembled sub-assemblies are designated with a part number beginning with GN. Sub-assemblies, which are put together at the production stage, do not have a separate part number.

The products in the Px40 series typically contain two sub-assemblies:

- The power supply assembly comprising:
 - A power supply board
 - An output relay board
- The input module comprising:
 - One or more transformer boards, which contains the voltage and current transformers (partially or fully populated)
 - One or more input boards
 - Metal protective covers for EM (electromagnetic) shielding

The input module is pre-assembled and is therefore assigned a GN number, whereas the power supply module is assembled at production stage and does not therefore have an individual part number.

7.3 MAIN PROCESSOR BOARD

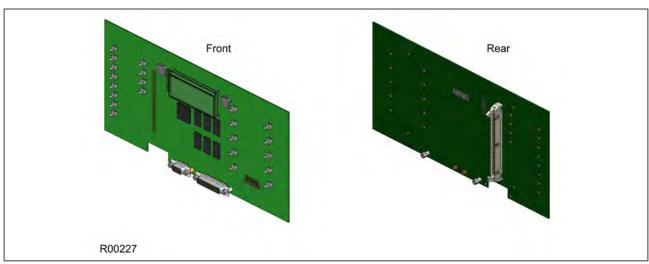


Figure 10: Main processor board

The main processor board performs all calculations and controls the operation of all other modules in the IED, including the data communication and user interfaces. This is the only board that does not fit into one of the slots. It resides in the front panel and connects to the rest of the system using an internal ribbon cable.

The LCD and LEDs are mounted on the processor board along with the front panel communication ports.

The memory on the main processor board is split into two categories: volatile and non-volatile. The volatile memory is fast access SRAM, used by the processor to run the software and store data during calculations. The non-volatile memory is sub-divided into two groups:

- Flash memory to store software code, text and configuration data including the present setting values.
- Battery-backed SRAM to store disturbance, event, fault and maintenance record data.

There are two board types available depending on the size of the case:

- For models in 40TE cases
- For models in 60TE cases and larger

7.4 POWER SUPPLY BOARD

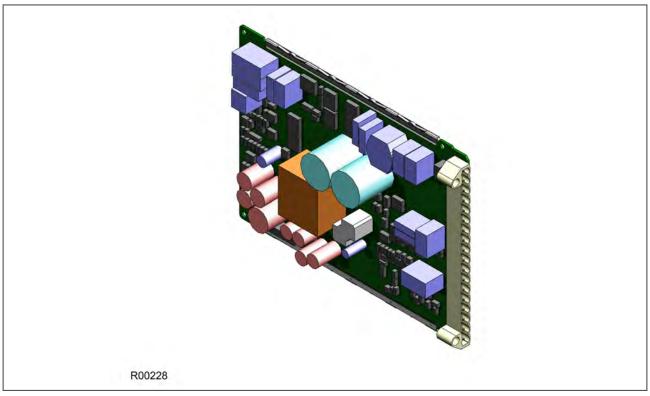


Figure 11: Power supply board

The power supply board provides power to the unit. One of three different configurations of the power supply board can be fitted to the unit. This is specified at the time of order and depends on the magnitude of the supply voltage that will be connected to it.

There are three board types, which support the following voltage ranges:

- 24/54 V DC
- 48/125 V DC or 40-100V AC
- 110/250 V DC or 100-240V AC

The power supply board connector plugs into a medium duty terminal block. This terminal block is always positioned on the right hand side of the unit looking from the rear.

The power supply board is usually assembled together with a relay output board to form a complete subassembly, as shown in the following diagram.

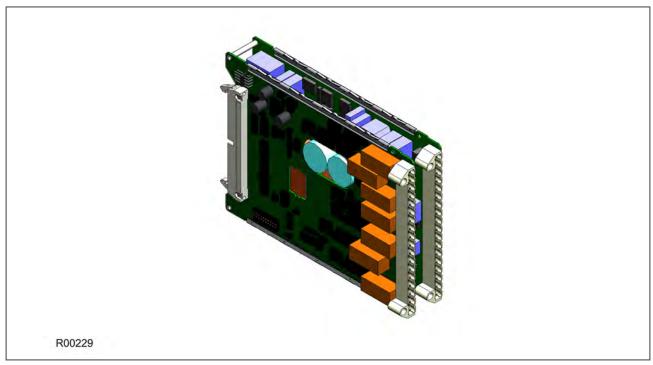


Figure 12: Power supply assembly

The power supply outputs are used to provide isolated power supply rails to the various modules within the unit. Three voltage levels are used by the unit's modules:

- 5.1 V for all of the digital circuits
- +/- 16 V for the analogue electronics such as on the input board
- 22 V for driving the output relay coils.

All power supply voltages, including the 0 V earth line, are distributed around the unit by the 64-way ribbon cable.

The power supply board incorporates inrush current limiting. This limits the peak inrush current to approximately 10 A.

Power is applied to pins 1 and 2 of the terminal block, where pin 1 is negative and pin 2 is positive. The pin numbers are clearly marked on the terminal block as shown in the following diagram.

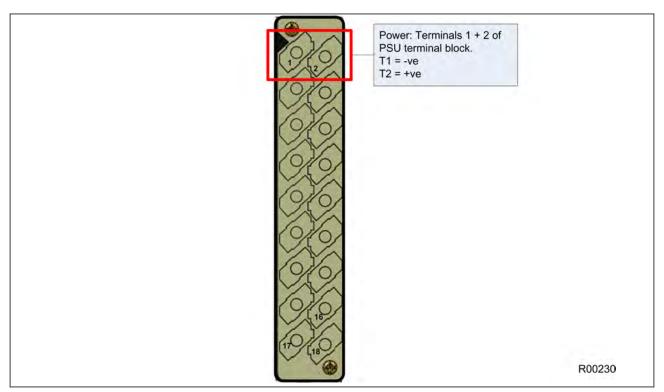


Figure 13: Power supply terminals

7.4.1 WATCHDOG

The Watchdog contacts are also hosted on the power supply board. The Watchdog facility provides two output relay contacts, one normally open and one normally closed. These are used to indicate the health of the device and are driven by the main processor board, which continually monitors the hardware and software when the device is in service.

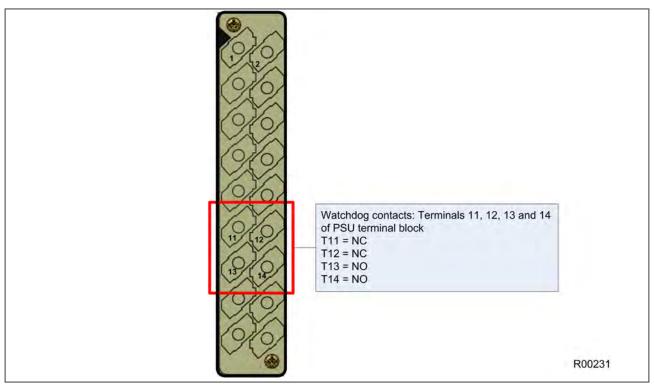


Figure 14: Watchdog contact terminals

7.4.2 REAR SERIAL PORT

The rear serial port (RP1) is housed on the power supply board. This is a three-terminal EIA(RS)485 serial communications port and is intended for use with a permanently wired connection to a remote control centre for SCADA communication. The interface supports half-duplex communication and provides optical isolation for the serial data being transmitted and received.

The physical connectivity is achieved using three screw terminals; two for the signal connection, and the third for the earth shield of the cable. These are located on pins 16, 17 and 18 of the power supply terminal block, which is on the far right looking from the rear. The interface can be selected between RS485 and K-bus. When the K-Bus option is selected, the two signal connections are not polarity conscious.

The polarity independent K-bus can only be used for the Courier data protocol. The polarity conscious MODBUS, IEC 60870-5-103 and DNP3.0 protocols need RS485.

The following diagram shows the rear serial port. The pin assignments are as follows:

- Pin 16: Earth shield
- Pin 17: Negative signal
- Pin 18: Positive signal

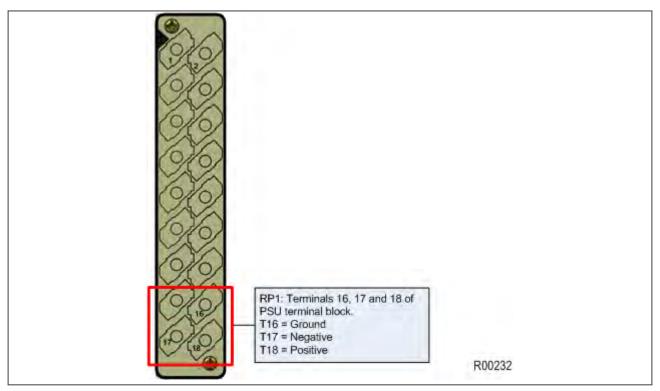


Figure 15: Rear serial port terminals

An additional serial port with D-type presentation is available as an optional board, if required.

7.5 INPUT MODULE - 1 TRANSFORMER BOARD

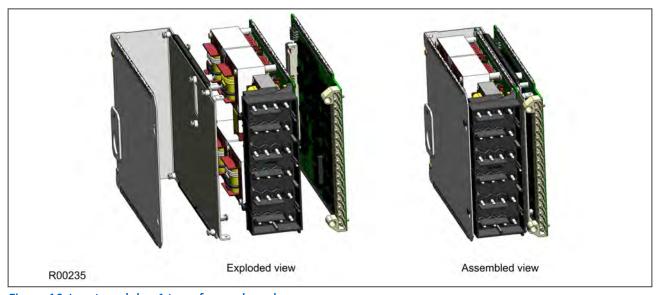


Figure 16: Input module - 1 transformer board

The input module consists of the main input board coupled together with an instrument transformer board. The instrument transformer board contains the voltage and current transformers, which isolate and scale the analogue input signals delivered by the system transformers. The input board contains the A/D conversion and digital processing circuitry, as well as eight digital isolated inputs (opto-inputs).

The boards are connected together physically and electrically. The module is encased in a metal housing for shielding against electromagnetic interference.

Optical 8 digital inputs Optical Isolator Isolator Noise Noise filter filter Parallel Bus Buffer Transformer board VT Serial Link Serial A/D Converter interface VT V00239

7.5.1 INPUT MODULE CIRCUIT DESCRIPTION

Figure 17: Input module schematic

A/D Conversion

The differential analogue inputs from the CT and VT transformers are presented to the main input board as shown. Each differential input is first converted to a single input quantity referenced to the input board's earth potential. The analogue inputs are sampled and converted to digital, then filtered to remove unwanted properties. The samples are then passed through a serial interface module which outputs data on the serial sample data bus.

The calibration coefficients are stored in non-volatile memory. These are used by the processor board to correct for any amplitude or phase errors introduced by the transformers and analogue circuitry.

Opto-isolated inputs

The other function of the input board is to read in the state of the digital inputs. As with the analogue inputs, the digital inputs must be electrically isolated from the power system. This is achieved by means of the 8 on-board optical isolators for connection of up to 8 digital signals. The digital signals are passed through an optional noise filter before being buffered and presented to the unit's processing boards in the form of a parallel data bus.

This selectable filtering allows the use of a pre-set filter of ½ cycle which renders the input immune to induced power-system noise on the wiring. Although this method is secure it can be slow, particularly for inter-tripping. This can be improved by switching off the ½ cycle filter, in which case one of the following methods to reduce ac noise should be considered.

- Use double pole switching on the input
- Use screened twisted cable on the input circuit

The opto-isolated logic inputs can be configured for the nominal battery voltage of the circuit for which they are a part, allowing different voltages for different circuits such as signalling and tripping.

Note:

The opto-input circuitry can be provided without the A/D circuitry as a separate board, which can provide supplementary opto-inputs.

7.5.2 TRANSFORMER BOARD

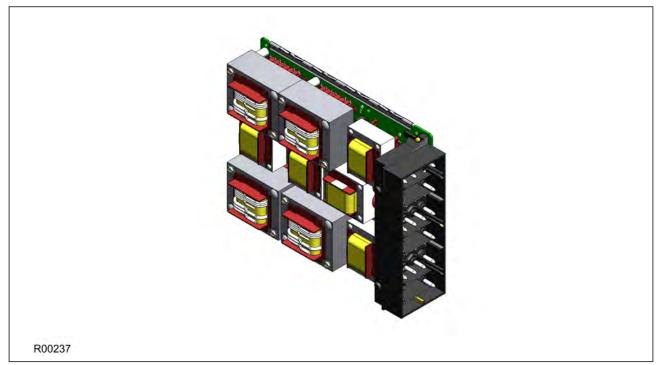


Figure 18: Transformer board

The transformer board hosts the current and voltage transformers. These are used to step down the currents and voltages originating from the power systems' current and voltage transformers to levels that can be used by the devices' electronic circuitry. In addition to this, the on-board CT and VT transformers provide electrical isolation between the unit and the power system.

The transformer board is connected physically and electrically to the input board to form a complete input module. For terminal connections, please refer to the wiring diagrams.

7.5.3 INPUT BOARD

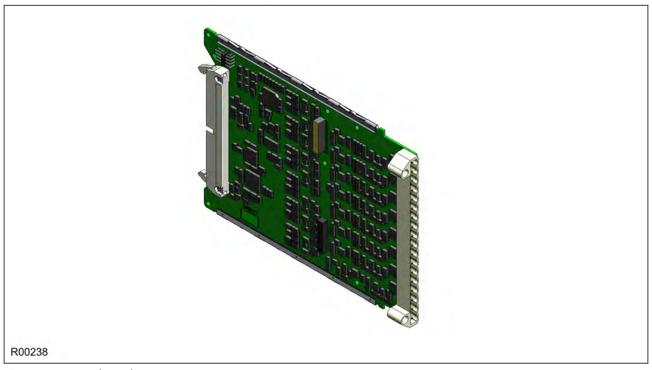


Figure 19: Input board

The input board is used to convert the analogue signals delivered by the current and voltage transformers into digital quantities used by the IED. This input board also has on-board opto-input circuitry, providing eight optically-isolated digital inputs and associated noise filtering and buffering. These opto-inputs are presented to the user by means of a MD terminal block, which sits adjacent to the analogue inputs HD terminal block.

The input board is connected physically and electrically to the transformer board to form a complete input module.

The terminal numbers of the opto-inputs are as follows:

Terminal Number	Opto-input
Terminal 1	Opto 1 -ve
Terminal 2	Opto 1 +ve
Terminal 3	Opto 2 -ve
Terminal 4	Opto 2 +ve
Terminal 5	Opto 3 -ve
Terminal 6	Opto 3 +ve
Terminal 7	Opto 4 -ve
Terminal 8	Opto 4 +ve
Terminal 9	Opto 5 -ve
Terminal 10	Opto 5 +ve
Terminal 11	Opto 6 -ve
Terminal 12	Opto 6 +ve
Terminal 13	Opto 7 -ve
Terminal 14	Opto 7 +ve
Terminal 15	Opto 8 -ve
Terminal 16	Opto 8 +ve

Terminal Number	Opto-input
Terminal 17	Common
Terminal 18	Common

7.6 STANDARD OUTPUT RELAY BOARD

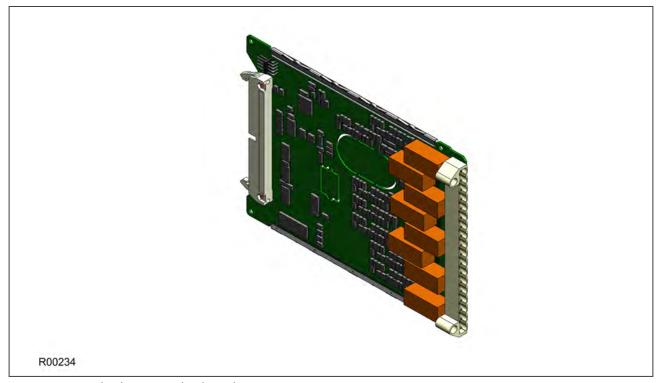


Figure 20: Standard output relay board - 8 contacts

This output relay board has 8 relays with 6 Normally Open contacts and 2 Changeover contacts.

The output relay board is provided together with the power supply board as a complete assembly, or independently for the purposes of relay output expansion.

There are two cut-out locations in the board. These can be removed to allow power supply components to protrude when coupling the output relay board to the power supply board. If the output relay board is to be used independently, these cut-out locations remain intact.

The terminal numbers are as follows:

Terminal Number	Output Relay
Terminal 1	Relay 1 NO
Terminal 2	Relay 1 NO
Terminal 3	Relay 2 NO
Terminal 4	Relay 2 NO
Terminal 5	Relay 3 NO
Terminal 6	Relay 3 NO
Terminal 7	Relay 4 NO
Terminal 8	Relay 4 NO
Terminal 9	Relay 5 NO
Terminal 10	Relay 5 NO

Terminal Number	Output Relay
Terminal 11	Relay 6 NO
Terminal 12	Relay 6 NO
Terminal 13	Relay 7 changeover
Terminal 14	Relay 7 changeover
Terminal 15	Relay 7 common
Terminal 16	Relay 8 changeover
Terminal 17	Relay 8 changeover
Terminal 18	Relay 8 common

7.7 IRIG-B BOARD

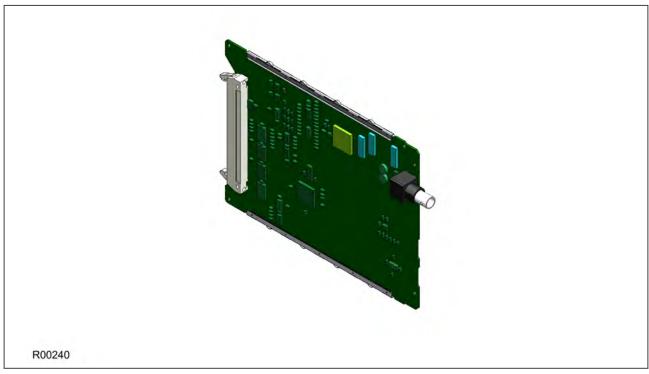


Figure 21: IRIG-B board

The IRIG-B board can be fitted to provide an accurate timing reference for the device. The IRIG-B signal is connected to the board via a BNC connector. The timing information is used to synchronise the IED's internal real-time clock to an accuracy of 1 ms. The internal clock is then used for time tagging events, fault, maintenance and disturbance records.

IRIG-B interface is available in modulated or demodulated formats.

The IRIG-B facility is provided in combination with other functionality on a number of additional boards, such as:

- Fibre board with IRIG-B
- Second rear communications board with IRIG-B
- Ethernet board with IRIG-B
- Redundant Ethernet board with IRIG-B

There are two types of each of these boards; one type which accepts a modulated IRIG-B input and one type which accepts a demodulated IRIG-B input.

7.8 FIBRE OPTIC BOARD

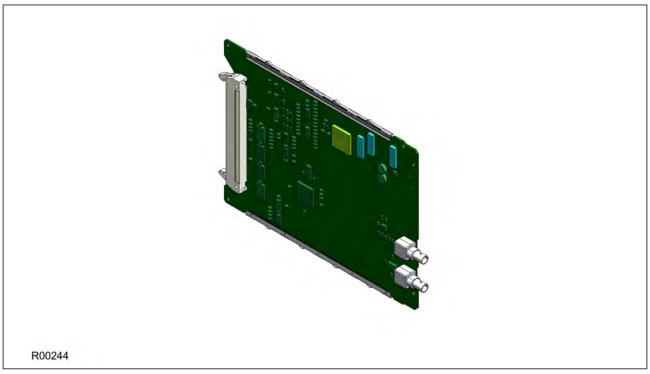


Figure 22: Fibre optic board

This board provides an interface for communicating with a master station. This communication link can use all compatible protocols (Courier, IEC 60870-5-103, MODBUS and DNP 3.0). It is a fibre-optic alternative to the metallic RS485 port presented on the power supply terminal block. The metallic and fibre optic ports are mutually exclusive.

The fibre optic port uses BFOC 2.5 ST connectors.

The board comes in two varieties; one with an IRIG-B input and one without:

7.9 REAR COMMUNICATION BOARD

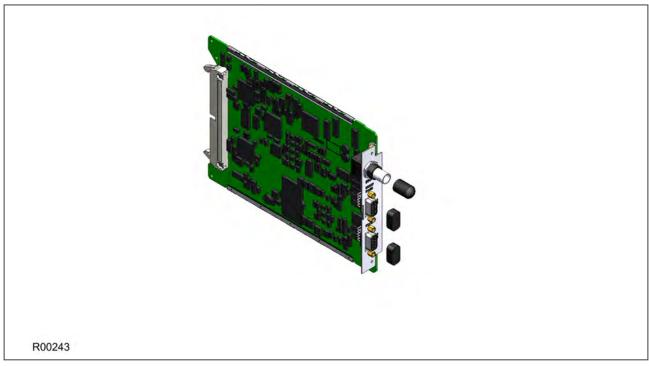


Figure 23: Rear communication board

The optional communications board containing the secondary communication ports provide two serial interfaces presented on 9 pin D-type connectors. These interfaces are known as SK4 and SK5. Both connectors are female connectors, but are configured as DTE ports. This means pin 2 is used to transmit information and pin 3 to receive.

SK4 can be used with RS232, RS485 and K-bus. SK5 can only be used with RS232 and is used for electrical teleprotection. The optional rear communications board and IRIG-B board are mutually exclusive since they use the same hardware slot. However, the board comes in two varieties; one with an IRIG-B input and one without.

7.10 ETHERNET BOARD



Figure 24: Ethernet board

This is a communications board that provides a standard 100-Base Ethernet interface. This board supports one electrical copper connection and one fibre-pair connection.

There are several variants for this board as follows:

- 100 Mbps Ethernet board
- 100 Mbps Ethernet with on-board modulated IRIG-B input
- 100 Mbps Ethernet with on-board unmodulated IRIG-B input

Two of the variants provide an IRIG-B interface. IRIG-B provides a timing reference for the unit – one board for modulated IRIG-B and one for demodulated. The IRIG B signal is connected to the board with a BNC connector.

The Ethernet and other connection details are described below:

IRIG-B Connector

• Centre connection: Signal

Outer connection: Earth

LEDs

LED	Function	On	Off	Flashing
Green	Link	Link ok	Link broken	
Yellow	Activity			Traffic

Optical Fibre Connectors

Connector	Function	
Rx	Receive	
Tx	Transmit	

RJ45connector

Pin	Signal name	Signal definition		
1	TXP	Transmit (positive)		
2	TXN	Transmit (negative)		
3	RXP	Receive (positive)		
4	-	Not used		
5	-	Not used		
6	RXN	Receive (negative)		
7	-	Not used		
8	-	Not used		

7.11 REDUNDANT ETHERNET BOARD

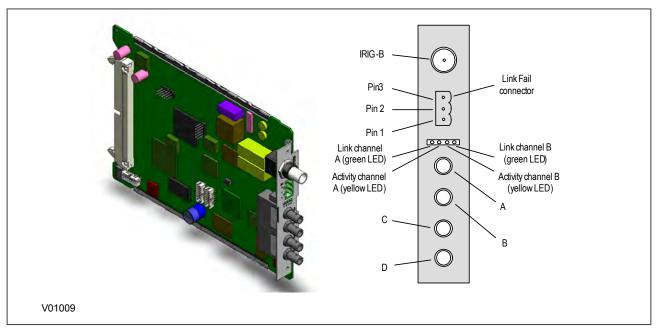


Figure 25: Redundant Ethernet board

This board provides dual redundant Ethernet (supported by two fibre pairs) together with an IRIG-B interface for timing.

Different board variants are available, depending on the redundancy protocol and the type of IRIG-B signal (unmodulated or modulated). The available redundancy protocols are:

- SHP (Self healing Protocol)
- RSTP (Rapid Spanning Tree Protocol)
- DHP (Dual Homing Protocol)
- PRP (Parallel Redundancy Protocol)
- HSR (High-availability Seamless Redundancy)

There are several variants for this board as follows:

- 100 Mbps redundant Ethernet running RSTP, with on-board modulated IRIG-B
- 100 Mbps redundant Ethernet running RSTP, with on-board unmodulated IRIG-B
- 100 Mbps redundant Ethernet running SHP, with on-board modulated IRIG-B
- 100 Mbps redundant Ethernet running SHP, with on-board unmodulated IRIG-B
- 100 Mbps redundant Ethernet running DHP, with on-board modulated IRIG-B
- 100 Mbps redundant Ethernet running DHP, with on-board unmodulated IRIG-B
- 100 Mbps redundant Ethernet running PRP, with on-board modulated IRIG-B
- 100 Mbps redundant Ethernet running PRP, with on-board demodulated IRIG-B
- 100 Mbps redundant Ethernet running HSR, with on-board modulated IRIG-B
- 100 Mbps redundant Ethernet running HSR, with on-board demodulated IRIG-B

The Ethernet and other connection details are described below:

IRIG-B Connector

- Centre connection: Signal
- Outer connection: Earth

Link Fail Connector (Ethernet Board Watchdog Relay)

Pin Closed		Open
1-2	Link fail Channel 1 (A)	Link ok Channel 1 (A)
2-3	Link fail Channel 2 (B)	Link ok Channel 2 (B)

LEDs

LED Function		On	Off	Flashing
Green	Link	Link ok	Link broken	
Yellow	Activity	SHP running		PRP, RSTP or DHP traffic

Optical Fibre Connectors (ST)

Connector	DHP	RSTP	SHP	PRP
Α	RXA	RX1	RS	RXA
В	TXA	TX1	ES	TXA
С	RXB	RX2	RP	RXB
D	TXB	TX2	EP	TXB

RJ45connector

Pin	Signal name	Signal definition
1	TXP	Transmit (positive)
2	TXN	Transmit (negative)
3	RXP	Receive (positive)
4	-	Not used
5	-	Not used
6	RXN	Receive (negative)
7	-	Not used
8	-	Not used

CHAPTER 4

SOFTWARE DESIGN

64

1	$C \coprod A$	PTER	\cap	/CDL	
1	СПА	PIEK	UV	/EKV	/IEVV

Protection and Control Functions

This chapter describes the software design of the IED.	
This chapter contains the following sections:	
Chapter Overview	59
Sofware Design Overview	60
System Level Software	61
Platform Software	63

2 SOFWARE DESIGN OVERVIEW

The device software can be conceptually categorized into several elements as follows:

- The system level software
- The platform software
- The protection and control software

These elements are not distinguishable to the user, and the distinction is made purely for the purposes of explanation. The following figure shows the software architecture.

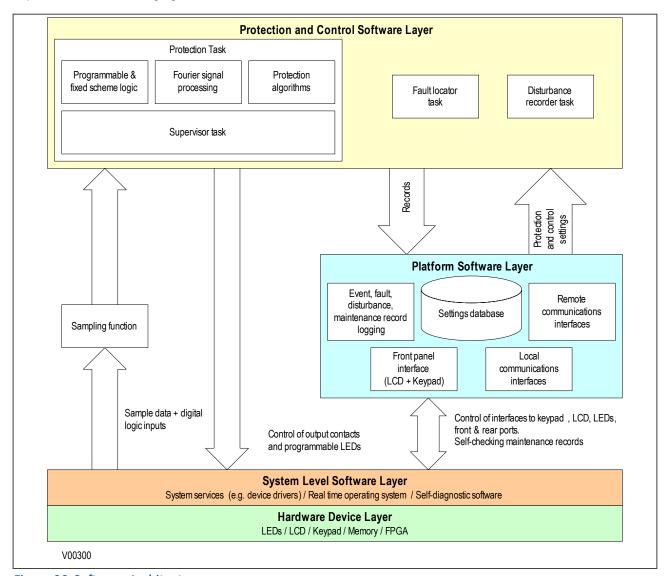


Figure 26: Software Architecture

The software, which executes on the main processor, can be divided into a number of functions as illustrated above. Each function is further broken down into a number of separate tasks. These tasks are then run according to a scheduler. They are run at either a fixed rate or they are event driven. The tasks communicate with each other as and when required.

3 SYSTEM LEVEL SOFTWARE

3.1 REAL TIME OPERATING SYSTEM

The real-time operating system is used to schedule the processing of the various tasks. This ensures that they are processed in the time available and in the desired order of priority. The operating system also plays a part in controlling the communication between the software tasks, through the use of operating system messages.

3.2 SYSTEM SERVICES SOFTWARE

The system services software provides the layer between the hardware and the higher-level functionality of the platform software and the protection and control software. For example, the system services software provides drivers for items such as the LCD display, the keypad and the remote communication ports. It also controls things like the booting of the processor and the downloading of the processor code into RAM at startup.

3.3 SELF-DIAGNOSTIC SOFTWARE

The device includes several self-monitoring functions to check the operation of its hardware and software while in service. If there is a problem with the hardware or software, it should be able to detect and report the problem, and attempt to resolve the problem by performing a reboot. In this case, the device would be out of service for a short time, during which the 'Healthy' LED on the front of the device is switched OFF and the watchdog contact at the rear is ON. If the restart fails to resolve the problem, the unit takes itself permanently out of service; the 'Healthy' LED stays OFF and watchdog contact stays ON.

If a problem is detected by the self-monitoring functions, the device attempts to store a maintenance record to allow the nature of the problem to be communicated to the user.

The self-monitoring is implemented in two stages: firstly a thorough diagnostic check which is performed on bootup, and secondly a continuous self-checking operation, which checks the operation of the critical functions whilst it is in service.

3.4 STARTUP SELF-TESTING

The self-testing takes a few seconds to complete, during which time the IED's measurement, recording, control, and protection functions are unavailable. On a successful start-up and self-test, the 'health-state' LED on the front of the unit is switched on. If a problem is detected during the start-up testing, the device remains out of service until it is manually restored to working order.

The operations that are performed at start-up are:

- 1. System boot
- 2. System software initialisation
- 3. Platform software initialisation and monitoring

3.4.1 SYSTEM BOOT

The integrity of the Flash memory is verified using a checksum before the program code and stored data is loaded into RAM for execution by the processor. When the loading has been completed, the data held in RAM is compared to that held in the Flash memory to ensure that no errors have occurred in the data transfer and that the two are the same. The entry point of the software code in RAM is then called. This is the IED's initialisation code.

3.4.2 SYSTEM LEVEL SOFTWARE INITIALISATION

The initialization process initializes the processor registers and interrupts, starts the watchdog timers (used by the hardware to determine whether the software is still running), starts the real-time operating system and creates and starts the supervisor task. In the initialization process the device checks the following:

- The status of the backup battery
- The integrity of the battery-backed SRAM that is used to store event, fault and disturbance records
- The operation of the LCD controller
- The watchdog operation

At the conclusion of the initialization software the supervisor task begins the process of starting the platform software.

3.4.3 PLATFORM SOFTWARE INITIALISATION AND MONITORING

When starting the platform software, the IED checks the following:

- The integrity of the data held in non-volatile memory (using a checksum)
- The operation of the real-time clock
- The optional IRIG-B function (if applicable)
- The presence and condition of the input board
- The analog data acquisition system (it does this by sampling the reference voltage)

At the successful conclusion of all of these tests the unit is entered into service and the application software is started up.

3.5 CONTINUOUS SELF-TESTING

When the IED is in service, it continually checks the operation of the critical parts of its hardware and software. The checking is carried out by the system services software and the results are reported to the platform software. The functions that are checked are as follows:

- The Flash memory containing all program code and language text is verified by a checksum.
- The code and constant data held in system memory is checked against the corresponding data in Flash memory to check for data corruption.
- The system memory containing all data other than the code and constant data is verified with a checksum.
- The integrity of the digital signal I/O data from the opto-inputs and the output relay coils is checked by the data acquisition function every time it is executed.
- The operation of the analog data acquisition system is continuously checked by the acquisition function every time it is executed. This is done by sampling the reference voltages.
- The operation of the optional Ethernet board is checked by the software on the main processor card. If the Ethernet board fails to respond an alarm is raised and the card is reset in an attempt to resolve the problem.
- The operation of the optional IRIG-B function is checked by the software that reads the time and date from the board.

In the event that one of the checks detects an error in any of the subsystems, the platform software is notified and it attempts to log a maintenance record.

If the problem is with the battery status or the IRIG-B board, the device continues in operation. For problems detected in any other area, the device initiates a shutdown and re-boot, resulting in a period of up to 10 seconds when the functionality is unavailable.

A restart should clear most problems that may occur. If, however, the diagnostic self-check detects the same problem that caused the IED to restart, it is clear that the restart has not cleared the problem, and the device takes itself permanently out of service. This is indicated by the "health-state' LED on the front of the device, which switches OFF, and the watchdog contact which switches ON.

4 PLATFORM SOFTWARE

The platform software has three main functions:

- To control the logging of records generated by the protection software, including alarms, events, faults, and maintenance records
- To store and maintain a database of all of the settings in non-volatile memory
- To provide the internal interface between the settings database and the user interfaces, using the front panel interface and the front and rear communication ports

4.1 RECORD LOGGING

The logging function is used to store all alarms, events, faults and maintenance records. The records are stored in non-volatile memory to provide a log of what has happened. The IED maintains four types of log on a first in first out basis (FIFO). These are:

- Alarms
- Event records
- Fault records
- Maintenance records

The logs are maintained such that the oldest record is overwritten with the newest record. The logging function can be initiated from the protection software. The platform software is responsible for logging a maintenance record in the event of an IED failure. This includes errors that have been detected by the platform software itself or errors that are detected by either the system services or the protection software function. See the Monitoring and Control chapter for further details on record logging.

4.2 SETTINGS DATABASE

The settings database contains all the settings and data, which are stored in non-volatile memory. The platform software manages the settings database and ensures that only one user interface can modify the settings at any one time. This is a necessary restriction to avoid conflict between different parts of the software during a setting change.

Changes to protection settings and disturbance recorder settings, are first written to a temporary location SRAM memory. This is sometimes called 'Scratchpad' memory. These settings are not written into non-volatile memory immediately. This is because a batch of such changes should not be activated one by one, but as part of a complete scheme. Once the complete scheme has been stored in SRAM, the batch of settings can be committed to the non-volatile memory where they will become active.

4.3 INTERFACES

The settings and measurements database must be accessible from all of the interfaces to allow read and modify operations. The platform software presents the data in the appropriate format for each of the interfaces (LCD display, keypad and all the communications interfaces).

5 PROTECTION AND CONTROL FUNCTIONS

The protection and control software processes all of the protection elements and measurement functions. To achieve this it has to communicate with the system services software, the platform software as well as organise its own operations.

The protection task software has the highest priority of any of the software tasks in the main processor board. This ensures the fastest possible protection response.

The protection and control software provides a supervisory task, which controls the start-up of the task and deals with the exchange of messages between the task and the platform software.

5.1 ACQUISITION OF SAMPLES

After initialization, the protection and control task waits until there are enough samples to process. The acquisition of samples on the main processor board is controlled by a 'sampling function' which is called by the system services software.

This sampling function takes samples from the input module and stores them in a two-cycle FIFO buffer. The sample rate is 24 samples per cycle. This results in a nominal sample rate of 1,200 samples per second for a 50 Hz system and 1,440 samples per second for a 60 Hz system. However the sample rate is not fixed. It tracks the power system frequency as described in the next section.

5.2 FREQUENCY TRACKING

The device provides a frequency tracking algorithm so that there are always 24 samples per cycle irrespective of frequency drift within a certain frequency range (see technical specifications). If the frequency falls outside this range, the sample rate reverts to its default rate of 1200 Hz for 50 Hz or 1440 Hz for 60 Hz.

The frequency tracking of the analog input signals is achieved by a recursive Fourier algorithm which is applied to one of the input signals. It works by detecting a change in the signal's measured phase angle. The calculated value of the frequency is used to modify the sample rate being used by the input module, in order to achieve a constant sample rate per cycle of the power waveform. The value of the tracked frequency is also stored for use by the protection and control task.

The frequency tracks off any voltage or current in the order VA, VB, VC, IA, IB, IC, down to 10%Vn for voltage and 5%In for current.

5.3 DIRECT USE OF SAMPLE VALUES

Most of the IED's protection functionality uses the Fourier components calculated by the device's signal processing software. However RMS measurements and some special protection algorithms available in some products use the sampled values directly.

The disturbance recorder also uses the samples from the input module, in an unprocessed form. This is for waveform recording and the calculation of true RMS values of current, voltage and power for metering purposes.

In the case of special protection algorithms, using the sampled values directly provides exceptionally fast response because you do not have to wait for the signal processing task to calculate the fundamental. You can act on the sampled values immediately.

5.4 FOURIER SIGNAL PROCESSING

When the protection and control task is re-started by the sampling function, it calculates the Fourier components for the analog signals. Although some protection algorithms use some Fourier-derived harmonics (e.g. second harmonic for magnetizing inrush), most protection functions are based on the Fourier-derived fundamental components of the measured analog signals. The Fourier components of the input current and voltage signals are stored in memory so that they can be accessed by all of the protection elements' algorithms.

The Fourier components are calculated using single-cycle Fourier algorithm. This Fourier algorithm always uses the most recent 24 samples from the 2-cycle buffer.

Most protection algorithms use the fundamental component. In this case, the Fourier algorithm extracts the power frequency fundamental component from the signal to produce its magnitude and phase angle. This can be represented in either polar format or rectangular format, depending on the functions and algorithms using it.

The Fourier function acts as a filter, with zero gain at DC and unity gain at the fundamental, but with good harmonic rejection for all harmonic frequencies up to the nyquist frequency. Frequencies beyond this nyquist frequency are known as alias frequencies, which are introduced when the sampling frequency becomes less than twice the frequency component being sampled. However, the Alias frequencies are significantly attenuated by an anti-aliasing filter (low pass filter), which acts on the analog signals before they are sampled. The ideal cut-off point of an anti-aliasing low pass filter would be set at:

(samples per cycle) \times (fundamental frequency)/2

At 24 samples per cycle, this would be nominally 600 Hz for a 50 Hz system, or 720 Hz for a 60 Hz system.

The following figure shows the nominal frequency response of the anti-alias filter and the Fourier filter for a 24-sample single cycle fourier algorithm acting on the fundamental component:

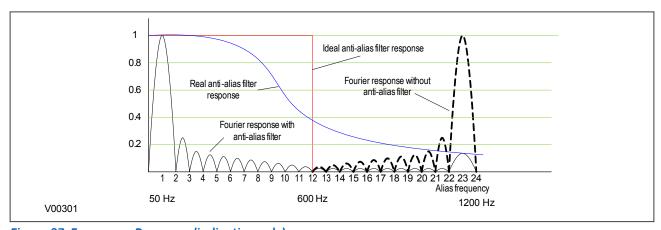


Figure 27: Frequency Response (indicative only)

5.5 PROGRAMMABLE SCHEME LOGIC

The purpose of the programmable scheme logic (PSL) is to allow you to configure your own protection schemes to suit your particular application. This is done with programmable logic gates and delay timers. To allow greater flexibility, different PSL is allowed for each of the four setting groups.

The input to the PSL is any combination of the status of the digital input signals from the opto-isolators on the input board, the outputs of the protection elements such as protection starts and trips, and the outputs of the fixed protection scheme logic (FSL). The fixed scheme logic provides the standard protection schemes. The PSL consists of software logic gates and timers. The logic gates can be programmed to perform a range of different logic functions and can accept any number of inputs. The timers are used either to create a programmable delay, and/or to condition the logic outputs, such as to create a pulse of fixed duration on the output regardless of the length of the pulse on the input. The outputs of the PSL are the LEDs on the front panel of the relay and the output contacts at the rear.

The execution of the PSL logic is event driven. The logic is processed whenever any of its inputs change, for example as a result of a change in one of the digital input signals or a trip output from a protection element. Also, only the part of the PSL logic that is affected by the particular input change that has occurred is processed. This reduces the amount of processing time that is used by the PSL. The protection & control software updates the logic delay timers and checks for a change in the PSL input signals every time it runs.

The PSL can be configured to create very complex schemes. Because of this PSL desing is achieved by means of a PC support package called the PSL Editor. This is available as part of the settings application software MiCOm S1 Agile, or as a standalone software module.

5.6 EVENT RECORDING

A change in any digital input signal or protection element output signal is used to indicate that an event has taken place. When this happens, the protection and control task sends a message to the supervisor task to indicate that an event is available to be processed and writes the event data to a fast buffer controlled by the supervisor task. When the supervisor task receives an event record, it instructs the platform software to create the appropriate log in non-volatile memory (battery backed-up SRAM). The operation of the record logging to battery backed-up SRAM is slower than the supervisor buffer. This means that the protection software is not delayed waiting for the records to be logged by the platform software. However, in the rare case when a large number of records to be logged are created in a short period of time, it is possible that some will be lost, if the supervisor buffer is full before the platform software is able to create a new log in battery backed-up SRAM. If this occurs then an event is logged to indicate this loss of information.

Maintenance records are created in a similar manner, with the supervisor task instructing the platform software to log a record when it receives a maintenance record message. However, it is possible that a maintenance record may be triggered by a fatal error in the relay in which case it may not be possible to successfully store a maintenance record, depending on the nature of the problem.

For more information, see the Monitoring and Control chapter.

5.7 DISTURBANCE RECORDER

The disturbance recorder operates as a separate task from the protection and control task. It can record the waveforms of the calibrated analog channels, plus the values of the digital signals. The recording time is user selectable up to a maximum of 10.5 seconds. The disturbance recorder is supplied with data by the protection and control task once per cycle, and collates the received data into the required length disturbance record. The disturbance records can be extracted using application software or the SCADA system, which can also store the data in COMTRADE format, allowing the use of other packages to view the recorded data.

For more information, see the Monitoring and Control chapter.

5.8 FAULT LOCATOR

The fault locator uses 12 cycles of the analog input signals to calculate the fault location. The result is returned to the protection and control task, which includes it in the fault record. The pre-fault and post-fault voltages are also presented in the fault record. When the fault record is complete, including the fault location, the protection and control task sends a message to the supervisor task to log the fault record.

The Fault Locator is not available on all models.

5.9 FUNCTION KEY INTERFACE

The function keys interface directly into the PSL as digital input signals. A change of state is only recognized when a key press is executed on average for longer than 200 ms. The time to register a change of state depends on whether the function key press is executed at the start or the end of a protection task cycle, with the additional hardware and software scan time included. A function key press can provide a latched (toggled mode) or output on key press only (normal mode) depending on how it is programmed. It can be configured to individual protection scheme requirements. The latched state signal for each function key is written to non-volatile memory and read from non-volatile memory during relay power up thus allowing the function key state to be reinstated after power-up, should power be inadvertently lost.

CHAPTER 5

CONFIGURATION

1 CHAPTER OVERVIEW

Each product has different configuration parameters according to the functions it has been designed to perform. There is, however, a common methodology used across the entire product series to set these parameters.

Some of the communications setup can only be carried out using the HMI, and cannot be carried out using settings applications software. This chapter includes concise instructions of how to configure the device, particularly with respect to the communications setup, as well as a description of the common methodology used to configure the device in general.

This chapter contains the following sections:

Chapter Overview	69
Settings Application Software	70
Using the HMI Panel	71
Date and Time Configuration	82
Settings Group Selection	85

2 SETTINGS APPLICATION SOFTWARE

To configure this device you will need to use the Settings Application Software. The settings application software used in this range of IEDs is called MiCOM S1 Agile. It is a collection of software tools, which is used for setting up and managing the IEDs.

Although you can change many settings using the front panel HMI, some of the features cannot be configured without the Settings Application Software; for example the programmable scheme logic, or IEC61850 communications.

If you do not already have a copy of the Settings Application Software, you can obtain it from General Electric contact centre.

To configure your product, you will need a data model that matches your product. When you launch the Settings Application Software, you will be presented with a panel that allows you to invoke the "Data Model Manager". This will close the other aspects of the software in order to allow an efficient import of the chosen data model. If you don't have, or can't find, the data model relating to your product, please call the General Electric contact centre.

When you have loaded all the data models you need, you should restart the Settings Application Software and start to create a model of your system using the "System Explorer" panel.

The software is designed to be intuitive, but help is available in an online help system and also the Settings Application Software user guide P40-M&CR-SAS-UG-EN-n, where 'Language' is a 2 letter code designating the language version of the user guide and 'n' is the latest version of the settings application software.

3 USING THE HMI PANEL

Using the HMI, you can:

- Display and modify settings
- View the digital I/O signal status
- Display measurements
- Display fault records
- Reset fault and alarm indications

The keypad provides full access to the device functionality using a range of menu options. The information is displayed on the LCD.

Keys	Description	Function	
	Up and down cursor keys	To change the menu level or change between settings in a particular column, or changing values within a cell	
Left and right cursor keys		To change default display, change between column headings, or changing values within a cell	
DK	ENTER key	For changing and executing settings	
	Hotkeys	For executing commands and settings for which shortcuts have been defined	
	Cancel key	To return to column header from any menu cell	
	Read key	To read alarm messages	
P	Function keys (not all models)	For executing user programmable functions	

Note:

As the LCD display has a resolution of 16 characters by 3 lines, some of the information is in a condensed mnemonic form.

3.1 NAVIGATING THE HMI PANEL

The cursor keys are used to navigate the menus. These keys have an auto-repeat function if held down continuously. This can be used to speed up both setting value changes and menu navigation. The longer the key is held pressed, the faster the rate of change or movement.

The navigation map below shows how to navigate the menu items.

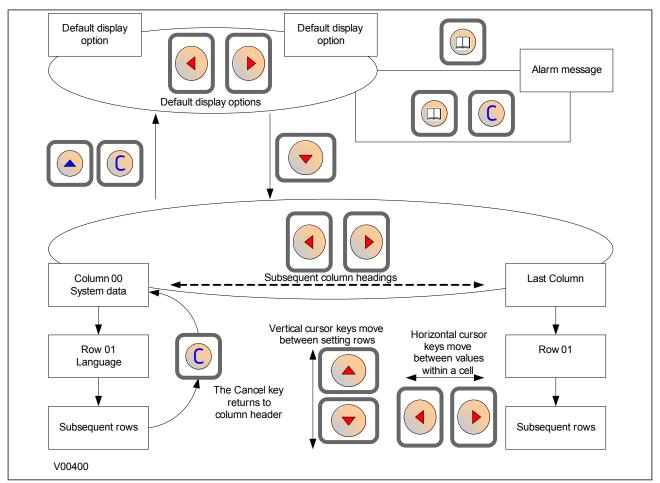


Figure 28: Navigating the HMI

3.2 GETTING STARTED

When you first start the IED, it will go through its power up procedure. After a few seconds it will settle down into one of the top level menus. There are two menus at this level:

- The Alarms menu for when there are alarms present
- The default display menu for when there are no alarms present.

If there are alarms present, the yellow Alarms LED will be flashing and the menu display will read as follows:

Alarms / Faults
Present

Even though the device itself should be in full working order when you first start it, an alarm could still be present, for example, if there is no network connection for a device fitted with a network card. If this is the case, you can read the alarm by pressing the 'Read' key.

ALARMS NIC Link Fail

If the device is fitted with an Ethernet card, you will first need to connect the device to an active Ethernet network to clear the alarm and get the default display.

If there are other alarms present, these must also be cleared before you can get into the default display menu options.

3.3 DEFAULT DISPLAY

The HMI contains a range of possible options that you can choose to be the default display. The options available are:

NERC Compliant banner

If the device is a cyber-security model, it will provide a NERC-compliant default display. If the device does not contain the cyber-security option, this display option is not available.

ACCESS ONLY FOR AUTHORISED USERS HOWKEY

Date and time

For example:

11:09:15 23 Nov 2011 HOWKEY

Description (user-defined)

For example:

Description
MiCOM P14NB

Plant reference (user-defined)

For example:

Plant Reference MiCOM HOTKEY

Access Level

For example:



In addition to the above, there are also displays for the system voltages, currents, power and frequency etc., depending on the device model.

3.4 DEFAULT DISPLAY NAVIGATION

The following diagram is an example of the default display navigation. In this example, we have used a cyber-secure model. This is an example only and may not apply in its entirety to all models. The actual display options available depend on the exact model.

Use the horizontal cursor keys to step through from one display to the next.

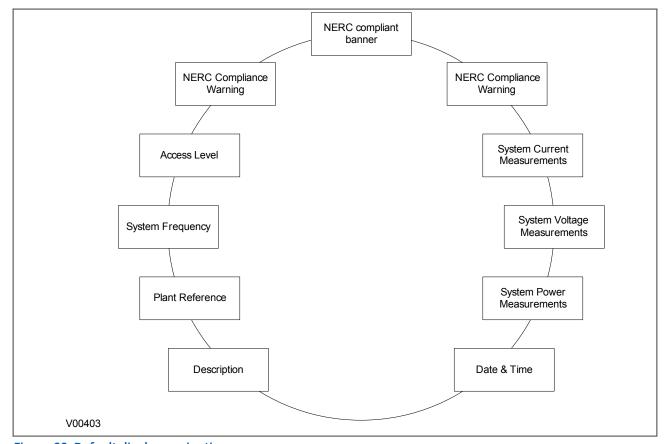


Figure 29: Default display navigation

If the device is cyber-secure but is not yet configured for NERC compliance (see Cyber-security chapter), a warning will appear when moving from the "NERC compliant" banner. The warning message is as follows:

DISPLAY NOT NERC COMPLIANT. OK?

You will have to confirm with the **Enter** button before you can go any further.

Note:

Whenever the IED has an uncleared alarm the default display is replaced by the text Alarms/ Faults present. You cannot override this default display. However, you can enter the menu structure from the default display, even if the display shows the Alarms/Faults present message.

3.5 PASSWORD ENTRY

Configuring the default display (in addition to modification of other settings) requires level 3 access. You will be prompted for a password before you can make any changes, as follows. The default level 3 password is AAAA.

Enter Password

- 1. A flashing cursor shows which character field of the password can be changed. Press the up or down cursor keys to change each character (tip: pressing the up arrow once will return an upper case "A" as required by the default level 3 password).
- 2. Use the left and right cursor keys to move between the character fields of the password.
- 3. Press the **Enter** key to confirm the password. If you enter an incorrect password, an invalid password message is displayed then the display reverts to *Enter password*. On entering a valid password a message appears indicating that the password is correct and which level of access has been unlocked. If this level is sufficient to edit the selected setting, the display returns to the setting page to allow the edit to continue. If the correct level of password has not been entered, the password prompt page appears again.
- 4. To escape from this prompt press the **Clear** key. Alternatively, enter the password using the **Password** setting in the SYSTEM DATA column. If the keypad is inactive for 15 minutes, the password protection of the front panel user interface reverts to the default access level.

To manually reset the password protection to the default level, select **Password**, then press the CLEAR key instead of entering a password.

Note:

In the SECURITY CONFIG column, you can set the maximum number of attemps, the time window in which the failed attempts are counted and the time duration for which the user is blocked.

3.6 PROCESSING ALARMS AND RECORDS

If there are any alarm messages, they will appear on the default display and the yellow alarm LED flashes. The alarm messages can either be self-resetting or latched. If they are latched, they must be cleared manually.

- 1. To view the alarm messages, press the **Read** key. When all alarms have been viewed but not cleared, the alarm LED changes from flashing to constantly on, and the latest fault record appears (if there is one).
- 2. Scroll through the pages of the latest fault record, using the cursor keys. When all pages of the fault record have been viewed, the following prompt appears.

Press Clear To Reset Alarms

- 3. To clear all alarm messages, press the **Clear** key. To return to the display showing alarms or faults present, and leave the alarms uncleared, press the **Read** key.
- 4. Depending on the password configuration settings, you may need to enter a password before the alarm messages can be cleared.
- 5. When all alarms are cleared, the yellow alarm LED switches off. If the red LED was on, this will also be switched off.

Note:

To speed up the procedure, you can enter the alarm viewer using the **Read** key and subsequently pressing the **Clear** key. This goes straight to the fault record display. Press the **Clear** key again to move straight to the alarm reset prompt, then press the **Clear** key again to clear all alarms.

3.7 MENU STRUCTURE

Settings, commands, records and measurements are stored in a local database inside the IED. When using the Human Machine Interface (HMI) it is convenient to visualise the menu navigation system as a table. Each item in the menu is known as a cell, which is accessed by reference to a column and row address. Each column and row is assigned a 2-digit hexadecimal numbers, resulting in a unique 4-digit cell address for every cell in the database. The main menu groups are allocated columns and the items within the groups are allocated rows, meaning a particular item within a particular group is a cell.

Each column contains all related items, for example all of the disturbance recorder settings and records are in the same column.

There are three types of cell:

- Settings: this is for parameters that can be set to different values
- Commands: this is for commands to be executed
- Data: this is for measurements and records to be viewed, which are not settable

Note

Sometimes the term "Setting" is used generically to describe all of the three types.

The table below, provides an example of the menu structure:

SYSTEM DATA (Col 00)	VIEW RECORDS (Col 01)	MEASUREMENTS 1 (Col 02)	
Language (Row 01)	"Select Event [0n]" (Row 01)	IA Magnitude (Row 01)	
Password (Row 02)	word (Row 02) IA Phase Angle (Row 02)		
Sys Fn Links (Row 03)	Time & Date (Row 03)	IB Magnitude (Row 03)	

It is convenient to specify all the settings in a single column, detailing the complete Courier address for each setting. The above table may therefore be represented as follows:

Setting	Column	Row	Description
SYSTEM DATA	00	00	First Column definition
Language (Row 01)	00	01	First setting within first column
Password (Row 02)	00	02	Second setting within first column
Sys Fn Links (Row 03)	00	03	Third setting within first column
VIEW RECORDS	01	00	Second Column definition
Select Event [0n]	01	01	First setting within second column
Menu Cell Ref	01	02	Second setting within second column
Time & Date	01	03	Third setting within second column
MEASUREMENTS 1	02	00	Third Column definition
IA Magnitude	02	01	First setting within third column
IA Phase Angle	02	02	Second setting within third column
IB Magnitude	02	03	Third setting within third column

The first three column headers are common throughout much of the product ranges. However the rows within each of these column headers may differ according to the product type. Many of the column headers are the same for all products within the series. However, there is no guarantee that the addresses will be the same for a particular column header. Therefore you should always refer to the product settings documentation and not make any assumptions.

3.8 CHANGING THE SETTINGS

- 1. Starting at the default display, press the **Down** cursor key to show the first column heading.
- 2. Use the horizontal cursor keys to select the required column heading.
- 3. Use the vertical cursor keys to view the setting data in the column.
- 4. To return to the column header, either press the Up cursor key for a second or so, or press the **Clear** key once. It is only possible to move across columns at the column heading level.
- 5. To return to the default display, press the Up cursor key or the **Clear** key from any of the column headings. If you use the auto-repeat function of the Up cursor key, you cannot go straight to the default display from one of the column cells because the auto-repeat stops at the column heading.
- 6. To change the value of a setting, go to the relevant cell in the menu, then press the **Enter** key to change the cell value. A flashing cursor on the LCD shows that the value can be changed. You may be prompted for a password first.
- 7. To change the setting value, press the **Up** and **Down** cursor keys. If the setting to be changed is a binary value or a text string, select the required bit or character to be changed using the horizontal cursor keys.

- 8. Press the **Enter** key to confirm the new setting value or the **Clear** key to discard it. The new setting is automatically discarded if it is not confirmed within 15 seconds.
- 9. For protection group settings and disturbance recorder settings, the changes must be confirmed before they are used. When all required changes have been entered, return to the column heading level and press the Down cursor key. Before returning to the default display, the following prompt appears.

Update settings? ENTER or CLEAR

10. Press the **Enter** key to accept the new settings or press the **Clear** key to discard the new settings.

Note:

For the protection group and disturbance recorder settings, if the menu time-out occurs before the changes have been confirmed, the setting values are discarded. Control and support settings, howeverr, are updated immediately after they are entered, without the **Update settings?** prompt.

3.9 DIRECT ACCESS (THE HOTKEY MENU)

For settings and commands that need to be executed quickly or on a regular basis, the IED provides a pair of keys directly below the LCD display. These so called **Hotkeys** can be used to execute specified settings and commands directly.

The functions available for direct access using these keys are:

- Setting group selection
- Control inputs
- Circuit Breaker (CB) control functions

The availability of these functions is controlled by the *Direct Access* cell in the *CONFIGURATION* column. There are four options: *Disabled, Enabled, CB Ctrl only* and *Hotkey only*.

For the Setting Group selection and Control inputs, this cell must be set to either <code>Enabled</code> or <code>Hotkey only</code>. For CB Control functions, the cell must be set to <code>Enabled</code> or <code>CB Ctrl only</code>.

3.9.1 SETTING GROUP SELECTION USING HOTKEYS

In some models you can use the hotkey menu to select the settings group. By default, only Setting group 1 is enabled. Other setting groups will only be available if they are first enabled. To be able to select a different setting group, you must first enable them in the *CONFIGURATION* column.

To access the hotkey menu from the default display, you press the key directly below the HOTKEY text on the LCD. The following screen will appear.

←User32 STG GP→ HOTKEY MENU EXIT

Use the right cursor keys to enter the SETTING GROUP menu.

←Menu User01→
SETTING GROUP 1
Nxt Grp Select

Select the setting group with *Nxt Grp* and confirm by pressing *Select*. If neither of the cursor keys is pressed within 20 seconds of entering a hotkey sub menu, the device reverts to the default display.

3.9.2 CONTROL INPUTS

The control inputs are user-assignable functions. You can use the *CTRL I/P CONFIG* column to configure the control inputs for the hotkey menu. In order to do this, use the first setting *Hotkey Enabled* cell to enable or disable any of the 32 control inputs. You can then set each control input to latched or pulsed and set its command to On/Off, Set/Reset, In/Out, or Enabled/Disabled.

By default, the hotkey is enabled for all 32 control inputs and they are set to Set/Reset and are Latched.

To access the hotkey menu from the default display, you press the key directly below the HOTKEY text on the LCD. The following screen will appear.

←User32 STG GP→ HOTKEY MENU

Press the right cursor key twice to get to the first control input, or the left cursor key to get to the last control input.

←STP GP User02→ Control Input 1 EXIT SET

Now you can execute the chosen function (Set/Reset in this case).

If neither of the cursor keys is pressed within 20 seconds of entering a hotkey sub menu, the device reverts to the default display.

3.9.3 CIRCUIT BREAKER CONTROL

You can open and close the controlled circuit breaker with the hotkey to the right, if enabled as described above. By default, hotkey access to the circuit breakers is disabled.

If hotkeyaccess to the circuit breakers has been enabled, the bottom right hand part of the display will read "Open or Close" depending on whether the circuit breaker is closed or open respectively:

For example:

Plant Reference
MiCOM
HOTKEY CLOSE

To close the circuit breaker (in this case), press the key directly below CLOSE. You will be given an option to cancel or confirm.

Execute
CB CLOSE
Cancel Confirm

More detailed information on this can be found in the Monitoring and Control chapter.

3.10 FUNCTION KEYS

Most products have a number of function keys for programming control functionality using the programmable scheme logic (PSL).

Each function key has an associated programmable tri-colour LED that can be programmed to give the desired indication on function key activation.

These function keys can be used to trigger any function that they are connected to as part of the PSL. The function key commands are in the *FUNCTION KEYS* column.

The first cell down in the *FUNCTION KEYS* column is the *Fn Key Status* cell. This contains a binary string, which represents the function key commands. Their status can be read from this binary string.

FUNCTION KEYS Fn Key Status 0000000000

The next cell down (*Fn Key 1*) allows you to activate or disable the first function key (1). The *Lock* setting allows a function key to be locked. This allows function keys that are set to Toggled mode and their DDB signal active 'high', to be locked in their active state, preventing any further key presses from deactivating the associated function. Locking a function key that is set to the Normal mode causes the associated DDB signals to be permanently off. This safety feature prevents any inadvertent function key presses from activating or deactivating critical functions.

FUNCTION KEYS
Fn Key 1
Unlocked

The next cell down (*Fn Key 1 Mode*) allows you to set the function key to *Normal* or *Toggled*. In the Toggle mode the function key DDB signal output stays in the set state until a reset command is given, by activating the function key on the next key press. In the Normal mode, the function key DDB signal stays energised for as long as the function key is pressed then resets automatically. If required, a minimum pulse width can be programmed by adding a minimum pulse timer to the function key DDB output signal.

FUNCTION KEYS Fn Key 1 Mode Toggled

The next cell down ($Fn \ Key \ 1 \ Label$) allows you to change the label assigned to the function. The default label is $Function \ key \ 1$ in this case. To change the label you need to press the enter key and then change the text on the bottom line, character by character. This text is displayed when a function key is accessed in the function key menu, or it can be displayed in the PSL.

FUNCTION KEYS Fn Key 1 Label Function Key 1

Subsequent cells allow you to carry out the same procedure as above for the other function keys.

The status of the function keys is stored in non-volatile memory. If the auxiliary supply is interrupted, the status of all the function keys is restored. The IED only recognises a single function key press at a time and a minimum key

press duration of approximately 200 ms is required before the key press is recognised. This feature avoids accidental double presses.

4 DATE AND TIME CONFIGURATION

The date and time setting will normally be updated automatically by the chosen UTC (Universal Time Coordination) time synchronisation mechanism when the device is in service. You can also set the date and time manually using the *Date/Time* cell in the *DATE AND TIME* column.

4.1 USING AN SNTP SIGNAL

When using SNTP to maintain the clock, the IED must first be connected to the SNTP server, which should be energized and functioning.

- 1. In the DATE AND TIME column, check that either the **Primary Source** or **Secondary Source** setting is set to SNTP.
- 2. Ensure that the IED is receiving valid time synchronisation messages by checking that the **SNTP Status** cell reads Server 1 OK or Server 2 OK.
- 3. Check that the **Act. Time Source** cell reads *SNTP*. This indicates that the IED is using PTP as the source for its time. Note that If IRIG-B or PTP have been selected as the Primary Source, these must first be disconnected before the device can switch to SNTP as the active source.
- 4. Once the IED is using SNTP as the active time source, adjust the time offset of the universal coordinated time on the SNTP Server equipment, so that local time is displayed.
- 5. Check that the time, date and month are correct in the **Date/Time** cell.

4.2 USING AN IRIG-B SIGNAL

When using IRIG-B to maintain the clock, the IED must first be connected to the timing source equipment (usually a P594), which should be energized and functioning.

- 1. In the DATE AND TIME column, check that either the **Primary Source** or **Secondary Source** setting is set to IRIG-B.
- 2. Ensure the IED is receiving the IRIG-B signal by checking that *IRIG-B Status* cell reads *Active*
- 3. Check that the **Act. Time Source** cell reads IRIG-B. This indicates that the IED is using IRIG-B as the source for its time. Note that If SNTP or PTP have been selected as the Primary Source, these must first be disconnected before the device can switch to IRIG-B as the active source.
- 4. Once the IED is using IRIG-B as the active time source, adjust the time offset of the universal coordinated time (satellite clock time) on the satellite clock equipment, so that local time is displayed.
- 5. Check that the time, date and month are correct in the *Date/Time* cell. The IRIG-B signal does not contain the current year so this also needs to be set manually in this cell.
- 6. If the auxiliary supply fails, the time and date are maintained by the auxiliary battery. Therefore, when the auxiliary supply is restored, you should not have to set the time and date again. To test this, remove the IRIG-B signal, and then remove the auxiliary supply. Leave the device de-energized for approximately 30 seconds. On re-energization, the time should be correct.
- 7. Reconnect the IRIG-B signal.

4.3 USING AN IEEE 1588 PTP SIGNAL

When using IEEE 1588 PTP to maintain the clock, the IED must first be connected to the PTP Grandmaster, which should be energized and functioning.

- 1. In the *DATE AND TIME* column, check that either the *Primary Source* or *Secondary Source* setting is set to *PTP*.
- 2. Set the *Domain Number* setting. The domain defines which clocks the IED will use for synchronisation. Therefore this number must match the domain used by the other clocks on the network.

- 3. Ensure that the IED is receiving valid time synchronisation messages by checking that the *PTP Status* cell reads *Valid Master*.
- 4. Check that **Act. Time Source** cell reads *PTP*. This indicates that the IED is using PTP as the source for its time. Note that If IRIG-B or SNTP have been selected as the Primary Source, these must first be disconnected before the device can switch to PTP as the active source.
- 5. Once the IED is using PTP as the active time source, adjust the time offset of the universal coordinated time on the Master Clock equipment, so that local time is displayed.
- 6. Check that the time, date and month are correct in the **Date/Time** cell.

4.4 WITHOUT A TIMING SOURCE SIGNAL

If the time and date is not being maintained by an IRIG-B, PTP or SNTP signal, in the *DATE AND TIME* column, ensure that both the *Primary Source* and *Secondary Source* are set to *NONE*.

- 1. Check that **Act. Time Source** cell reads *Free Running*.
- 2. Set the date and time to the correct local time and date using the Date/Time cell or the serial protocol.
- 3. If the auxiliary supply fails, the time and date are maintained by the auxiliary battery. Therefore, when the auxiliary supply is restored, you should not have to set the time and date again. To test this, remove the auxiliary supply. Leave the device de-energized for approximately 30 seconds. On re-energization, the time should be correct.

4.5 TIME ZONE COMPENSATION

The UTC time standard uses Greenwich Mean Time as its standard. Without compensation, the date and time would be displayed on the device irrespective of its location.

You may wish to display the local time corresponding to its geographical location. You can do this with the settings *LocalTime Enable* and *LocalTime Offset*.

The LocalTime Enable has three setting options; Disabled, Fixed, and Flexible.

With Disabled, no local time zone is maintained. Time synchronisation from any interface will be used to directly set the master clock. All times displayed on all interfaces will be based on the master clock with no adjustment.

With Fixed, a local time zone adjustment is defined using the **LocalTime Offset** setting and all non-IEC 61850 interfaces, which uses the Simple Network Time Protocol (SNTP), are compensated to display the local time.

With Flexible, a local time zone adjustment is defined using the **LocalTime Offset** setting. The non-local and non-IEC 61850 interfaces can be set to either the UTC zone or the local time zone. The local interfaces are always set to the local time zone and the Ethernet interface is always set to the UTC zone.

The interfaces where you can select between UTC and Local Time are the serial interfaces RP1, RP2, DNP over Ethernet (if applicable) and Tunnelled Courier (if applicable). This is achieved by means of the following settings, each of which can be set to UTC or Local.:

- RP1 Time Zone
- RP2 Time Zone
- DNPOE Time Zone
- Tunnel Time Zone

The **LocalTime Offset** setting allows you to enter the local time zone compensation from -12 to + 12 hours at 15 minute intervals.

4.6 DAYLIGHT SAVING TIME COMPENSATION

It is possible to compensate for Daylight Saving time using the following settings

- DST Enable
- DST Offset
- DST Start
- DST Start Day
- DST Start Month
- DST Start Mins
- DST End
- DST End Day
- DST End Month
- DST End Mins

These settings are described in the *DATE AND TIME* settings table in the configuration chapter.

5 SETTINGS GROUP SELECTION

You can select the setting group using opto inputs, a menu selection, and for some models the hotkey menu or function keys. You choose which method using the Setting Group setting in the CONFIGURATION column. There are two possibilities; Select via Menu, or Select via PSL. If you choose **Select via Menu**, you set the settings group using the **Active Settings** setting or with the hotkeys. If you choose **Select via PSL**, you set the settings group with DDB signals according to the following table:

SG Select 1X	SG Select X1	Selected Setting Group
0	0	1
0	1	2
1	0	3
1	1	4

Each setting group has its own PSL. Once a PSL configuration has been designed it can be allocated to any one of the 4 setting groups. When downloading or extracting a PSL configuration, you will be prompted to enter the required setting group to which it will allocated.

CHAPTER 6

CURRENT PROTECTION FUNCTIONS

1 CHAPTER OVERVIEW

The P141, P142, P143, P144, P145 provides a wide range of current protection functions. This chapter describes the operation of these functions including the principles, logic diagrams and applications.

This chapter contains the following sections:

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2 OVERCURRENT PROTECTION PRINCIPLES

Most electrical power system faults result in an overcurrent of one kind or another. It is the job of protection devices, formerly known as 'relays' but now known as Intelligent Electronic Devices (IEDs) to protect the power system from faults. The general principle is to isolate the faults as quickly as possible to limit the danger and prevent fault currents flowing through systems, which can cause severe damage to equipment and systems. At the same time, we wish to switch off only the parts of the power grid that are absolutely necessary, to prevent unnecessary blackouts. The protection devices that control the tripping of the power grid's circuit breakers are highly sophisticated electronic units, providing an array of functionality to cover the different fault scenarios for a multitude of applications.

The described products offer a range of overcurrent protection functions including:

- Phase Overcurrent protection
- Earth Fault Overcurrent protection
- Negative Sequence Overcurrent protection
- Sensitive Earth Fault protection

To ensure that only the necessary circuit breakers are tripped and that these are tripped with the smallest possible delay, the IEDs in the protection scheme need to co-ordinate with each other. Various methods are available to achieve correct co-ordination between IEDs in a system. These are:

- By means of time alone
- By means of current alone
- By means of a combination of both time and current.

Grading by means of current alone is only possible where there is an appreciable difference in fault level between the two locations where the devices are situated. Grading by time is used by some utilities but can often lead to excessive fault clearance times at or near source substations where the fault level is highest.

For these reasons the most commonly applied characteristic in co-ordinating overcurrent devices is the IDMT (Inverse Definite Minimum Time) type.

2.1 IDMT CHARACTERISTICS

There are two basic requirements to consider when designing protection schemes:

- All faults should be cleared as quickly as possible to minimise damage to equipment
- Fault clearance should result in minimum disruption to the electrical power grid.

The second requirement means that the protection scheme should be designed such that only the circuit breaker(s) in the protection zone where the fault occurs, should trip.

These two criteria are actually in conflict with one another, because to satisfy (1), we increase the risk of shutting off healthy parts of the grid, and to satisfy (2) we purposely introduce time delays, which increase the amount of time a fault current will flow. With IDMT protection applied to radial feeders, this probem is exacerbated by the nature of faults in that the protection devices nearest the source, where the fault currents are largest, actually need the longest time delay.

IDMT characteristics are described by operating curves. Traditionally, these were defined by the performance of electromechanical relays. In numerical protection, equations are used to replicate these characteristics so that they can be used to grade with older equipment.

The old electromechanical relays countered this problem somewhat due to their natural operate time v. fault current characteristic, whereby the higher the fault current, the quicker the operate time. The characteristic typical of these electromechanical relays is called Inverse Definite Minimum Time or IDMT for short.

2.1.1 IEC 60255 IDMT CURVES

There are four well-known variants of this characteristic:

- Standard Inverse
- Very inverse
- Extremely inverse
- UK Long Time inverse

These equations and corresponding curves governing these characteristics are very well known in the power industry.

Standard Inverse

This characteristic is commonly known as the 3/10 characteristic, i.e. at ten times setting current and TMS of 1 the relay will operate in 3 seconds.

The characteristic curve can be defined by the mathematical expression:

$$t_{op} = T \frac{0.14}{\left(\frac{I}{I_s}\right)^{0.02} - 1}$$

The standard inverse time characteristic is widely applied at all system voltages – as back up protection on EHV systems and as the main protection on HV and MV distribution systems.

In general, the standard inverse characteristics are used when:

- There are no co-ordination requirements with other types of protective equipment further out on the system, e.g. Fuses, thermal characteristics of transformers, motors etc.
- The fault levels at the near and far ends of the system do not vary significantly.
- There is minimal inrush on cold load pick up. Cold load inrush is that current which occurs when a feeder is energised after a prolonged outage. In general the relay cannot be set above this value but the current should decrease below the relay setting before the relay operates.

Very Inverse

This type of characteristic is normally used to obtain greater time selectivity when the limiting overall time factor is very low, and the fault current at any point does not vary too widely with system conditions. It is particularly suitable, if there is a substantial reduction of fault current as the distance from the power source increases. The steeper inverse curve gives longer time grading intervals. Its operating time is approximately doubled for a reduction in setting from 7 to 4 times the relay current setting. This permits the same time multiplier setting for several relays in series.

The characteristic curve can be defined by the mathematical expression:

$$t_{op} = T \frac{13.5}{\left(\frac{I}{I_s}\right) - 1}$$

Extremely Inverse

With this characteristic the operating time is approximately inversely proportional to the square of the current. The long operating time of the relay at peak values of load current make the relay particularly suitable for grading with fuses and also for protection of feeders which are subject to peak currents on switching in, such as feeders supplying refrigerators, pumps, water heaters etc., which remain connected even after a prolonged interruption of supply.

For cases where the generation is practically constant and discrimination with low tripping times is difficult to obtain, because of the low impedance per line section, an extremely inverse relay can be very useful since only a small difference of current is necessary to obtain an adequate time difference.

Another application for this relay is with auto reclosers in low voltage distribution circuits. As the majority of faults are of a transient nature, the relay is set to operate before the normal operating time of the fuse, thus preventing perhaps unnecessary blowing of the fuse.

Upon reclosure, if the fault persists, the recloser locks itself in the closed position and allows the fuse to blow to clear the fault.

This characteristic is also widely used for protecting plant against overheating since overheating is usually an I2t function.

This characteristic curve can be defined by the mathematical expression:

$$t_{op} = T \frac{80}{\left(\frac{I}{I_s}\right)^2 - 1}$$

UK Long Time Inverse

This type of characteristic has a long time characteristic and may be used for protection of neutral earthing resistors (which normally have a 30 second rating). The relay operating time at 5 times current setting is 30 seconds at a TMS of 1.

This can be defined by:

$$t_{op} = T \frac{120}{\left(\frac{I}{I_s}\right) - 1}$$

In the above equations:

- t_{op} is the operating time
- T is the time multiplier setting
- I is the measured current
- I_s is the current threshold setting.

The ratio I/I_s is sometimes defined as 'M' or 'PSM' (Plug Setting Multiplier).

These curves are plotted as follows:

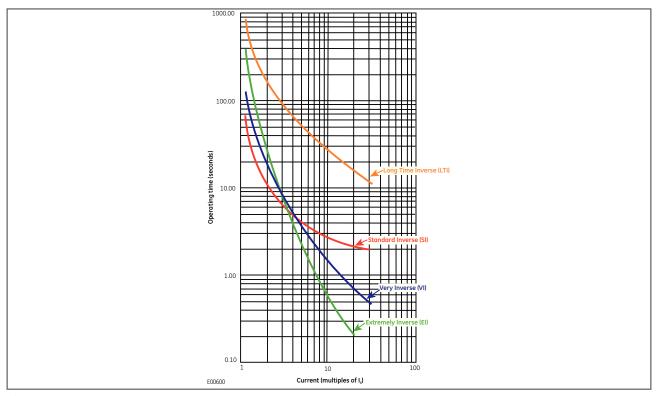


Figure 30: IEC 60255 IDMT curves

2.1.2 EUROPEAN STANDARDS

The IEC 60255 IDMT Operate equation is:

$$t_{op} = T \left(\frac{\beta}{M^{\alpha} - 1} + L \right) + C$$

and the IEC 60255 IDMT Reset equation is:

$$t_r = T \left(\frac{\beta}{1 - M^{\alpha}} \right)$$

where:

- t_{op} is the operating time
- t_r is the reset time
- T is the Time Multiplier setting
- M is the ratio of the measured current divided by the threshold current (I/Is)
- β is a constant, which can be chosen to satisfy the required curve characteristic
- \bullet a is a constant, which can be chosen to satisfy the required curve characteristic
- C is a constant for adding Definite Time (Definite Time adder)
- L is a constant (usually only used for ANSI/IEEE curves)

The constant values for the IEC IDMT curves are as follows:

Curve Description	β constant	α constant	L constant
IEC Standard Inverse Operate	0.14	0.02	0
IEC Standard Inverse Reset	8.2	6.45	0

Curve Description	β constant	α constant	L constant
IEC Very Inverse Operate	13.5	1	0
IEC Very Inverse Reset	50.92	2.4	0
IEC Extremely Inverse Operate	80	2	0
IEC Extremely Inverse Reset	44.1	3.03	0
UK Long Time Inverse Operate*	120	1	0
UK Rectifier Operate*	45900	5.6	0

Rapid Inverse (RI) characteristic

The RI operate curve is represented by the following equation:

$$t_{op} = K \left(\frac{1}{0.339 - \frac{0.236}{M}} \right)$$

where:

- t_{op} is the operating time
- K is the Time Multiplier setting
- M is the ratio of the measured current divided by the threshold current (I/I_S)

Note:

* When using UK Long Time Inverse, UK Rectifier or RI for the Operate characteristic, DT (Definite Time) is always used for the Reset characteristic.

2.1.3 NORTH AMERICAN STANDARDS

The IEEE IDMT Operate equation is:

$$t_{op} = TD\left(\frac{\beta}{M^{\alpha} - 1} + L\right) + C$$

and the IEEE IDMT Reset equation is:

$$t_r = TD\left(\frac{\beta}{1 - M^{\alpha}}\right)$$

where:

- t_{op} is the operating time
- t_r is the reset time
- TD is the Time Dial setting
- M is the ratio of the measured current divided by the threshold current (I/I_s)
- β is a constant, which can be chosen to satisfy the required curve characteristic
- α is a constant, which can be chosen to satisfy the required curve characteristic
- C is a constant for adding Definite Time (Definite Time adder)
- L is a constant (usually only used for ANSI/IEEE curves)

The constant values for the IEEE curves are as follows:

Curve Description	β constant	α constant	L constant
IEEE Moderately Inverse Operate	0.0515	0.02	0.114
IEEE Moderately Inverse Reset	4.85	2	0
IEEE Very Inverse Operate	19.61	2	0.491
IEEE Very Inverse Reset	21.6	2	0
IEEE Extremely Inverse Operate	28.2	2	0.1217
IEEE Extremely Inverse Reset	29.1	2	0
CO8 US Inverse Operate	5.95	2	0.18
CO8 US Inverse Reset	5.95	2	0
CO2 US Short Time Inverse Operate	0.16758	0.02	0.11858
CO2 US Short Time Inverse Reset	2.261	2	0

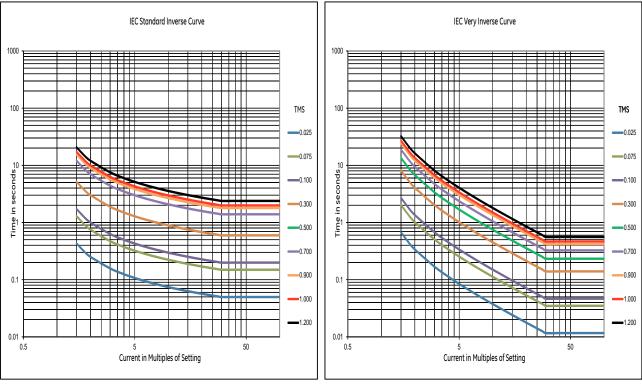
The constant values for the ANSI curves are as follows:

Curve Description	β constant	α constant	L constant
ANSI Normally Inverse Operate	8.9341	2.0938	0.17966
ANSI Normally Inverse Reset	9	2	0
ANSI Short Time Inverse Operate	0.03393	1.2969	0.2663
ANSI Short Time Inverse Reset	0.5	2	0
ANSI Long Time Inverse Operate	2.18592	1	5.6143
ANSI Long Time Inverse Reset	15.75	2	0

Note

^{*} When using UK Long Time Inverse or UK Rectifier for the Operate characteristic, DT is always used for the Reset characteristic.

2.1.4 IEC AND IEEE INVERSE CURVES



E00757

Figure 31: IEC standard and very inverse curves

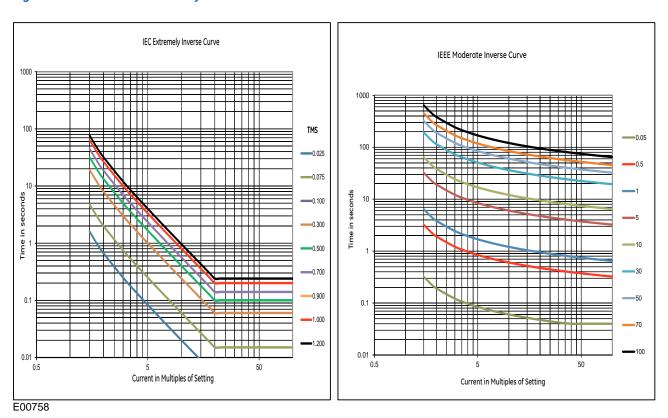
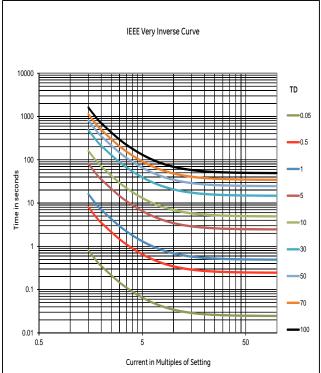
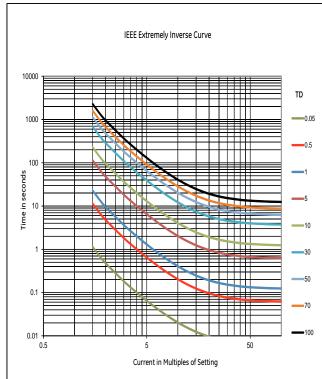


Figure 32: IEC Extremely inverse and IEEE moderate inverse curves





E00759

Figure 33: IEEE very and extremely inverse curves

2.1.5 DIFFERENCES BETWEEN THE NORTH AMERICAN AND EUROPEAN STANDARDS

The IEEE and US curves are set differently to the IEC/UK curves, with regard to the time setting. A time multiplier setting (TMS) is used to adjust the operating time of the IEC curves, whereas a time dial setting is used for the IEEE/US curves. The menu is arranged such that if an IEC/UK curve is selected, the *I> Time Dial* cell is not visible and vice versa for the TMS setting. For both IEC and IEEE/US type curves, a definite time adder setting is available, which will increase the operating time of the curves by the set value.

2.1.6 PROGRAMMABLE CURVES

As well as the standard curves as defined by various countries and standardising bodies, it is possible to program custom curves using the User Programmable Curve Tool, described in the Settings Application Software chapter. This is a user-friendly tool by which you can create curves either by formula or by entering data points. Programmable curves help you to match more closely the withstand characteristics of the electrical equipment than standard curves.

2.2 PRINCIPLES OF IMPLEMENTATION

The range of protection products provides a very wide range of protection functionality. Despite the diverse range of functionality provided, there is some commonality between the way many of the protection functions are implemented. It is important to describe some of these basic principles before going deeper into the individual protection functions.

A simple representation of protection functionality is shown in the following diagram:

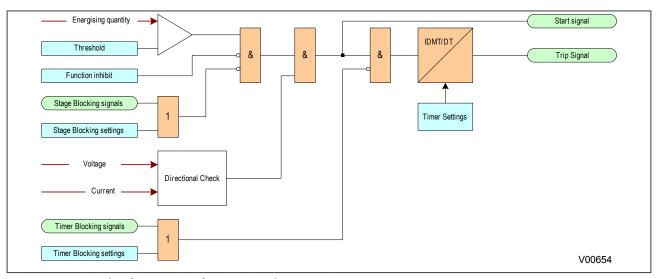


Figure 34: Principle of protection function implementation

An energising quantity is either a voltage input from a system voltage transformer, a current input from a system current transformer or another quantity derived from one or both of these. The energising quantities are extracted from the power system. The signals are converted to digital quantities where they can be processed by the IEDs internal processor.

In general, an energising quantity, be it a current, voltage, power, frequency, or phase quantity, is compared with a threshold value, which may be settable, or hard-coded depending on the function. If the quantity exceeds (for overvalues) or falls short of (for undervalues) the threshold, a signal is produced, which when gated with the various inhibit and blocking functions becomes the Start signal for that protection function. This Start signal is generally made available to Fixed Scheme Logic (FSL) and Programmable Scheme Logic (PSL) for further processing. It is also passed through a timer function to produce the Trip signal. The timer function may be an IDMT curve, or a Definite Time delay, depending on the function. This timer may also be blocked with timer blocking signals and settings. The timer can be configured by a range of settings to define such parameters as the type of curve, The Time Multiplier Setting, the IDMT constants, the Definite Time delay etc.

In General Electric products, there are usually several independent stages for each of the functions, and for three-phase functions, there are usually independent stages for each of the three phases.

Typically some stages use an Inverse Definite Minumum time (IDMT) timer function, and others use a Definite Time timer (DT) function. If the DT time delay is set to '0', then the function is known to be "instantaneous". In many instances, the term 'instantaneous protection" is used loosely to describe Definite Time protection stages, even when the stage may not theoretically be instantaneous.

Many protection functions require a direction-dependent decision. Such functions can only be implemented where both current and voltage inputs are available. For such functions, a directional check is required, whose output can block the Start signal should the direction of the fault be wrong.

Note:

In the logic diagrams and descriptive text, it is usually sufficient to show only the first stage, as the design principles for subsequent stages are usually the same (or at least very similar). Where there are differences between the functionality of different stages, this is clearly indicated.

2.2.1 TIMER HOLD FACILITY

The Timer Hold facility is available for stages with IDMT functionality, and is controlled by the timer reset settings for the relevant stages (e.g. *I>1 tReset*, *I>2 tReset*). These cells are not visible for the IEEE/US curves if an inverse time reset characteristic has been selected, because in this case the reset time is determined by the time dial setting (TDS).

This feature may be useful in certain applications, such as when grading with upstream electromechanical overcurrent relays, which have inherent reset time delays. If you set the hold timer to a value other than zero, the resetting of the protection element timers will be delayed for this period. This allows the element to behave in a similar way to an electromechanical relay. If you set the hold timer to zero, the overcurrent timer for that stage will reset instantaneously as soon as the current falls below a specified percentage of the current setting (typically 95%).

Another situation where the timer hold facility may be used to reduce fault clearance times is for intermittent faults. An example of this may occur in a plastic insulated cable. In this application it is possible that the fault energy melts and reseals the cable insulation, thereby extinguishing the fault. This process repeats to give a succession of fault current pulses, each of increasing duration with reducing intervals between the pulses, until the fault becomes permanent.

When the reset time is instantaneous, the device will repeatedly reset and not be able to trip until the fault becomes permanent. By using the Timer Hold facility the device will integrate the fault current pulses, thereby reducing fault clearance time.

3 PHASE OVERCURRENT PROTECTION

Phase current faults are faults where fault current flows between two or more phases of a power system. The fault current may be between the phase conductors only or, between two or more phase conductors and earth.

Although not as common as earth faults (single phase to earth), phase faults are typically more severe.

3.1 PHASE OVERCURRENT PROTECTION IMPLEMENTATION

Phase Overcurrent Protection is configured in the OVERCURRENT column of the relevant settings group.

The product provides six stages of segregated three-phase overcurrent protection, each with independent time delay characteristics. The settings are independent for each stage, but for each stage, the settings apply to all phases.

Stages 1, 2 and 5 provide a choice of operate and reset characteristics, where you can select between:

- A range of IDMT (Inverse Definite Minimum Time) curves based on IEC and IEEE standards
- A range of programmable user-defined curves
- DT (Definite Time) characteristic

For stage 1, this is achieved using the following settings:

- *I>1 Function* for the overcurrent operate characteristic
- I>1 Reset Char for the overcurrent reset characteristic
- I>1 Usr Rst Char for the reset characteristic for user-defined curves

The setting names for other stages follow the same principles.

The IDMT-equipped stages, (1,2 and 5) also provide a Timer Hold facility. Stage 1 for example, is configured using the cells *I>1 tReset*. This setting does not apply to IEEE curves.

Stages 3, 4 and 6 have definite time characteristics only.

I>1 Start A I>1 Current Set I>1 Trip A IA2H Start Timer Settings I> Blocking 2H Blocks I>1 2H 1PH Block I>1 Start B I>1 Current Set I>1 Trip B IB2H Start & Timer Settings I> Blocking 2H Blocks I>1 2H 1PH Block I>1 Start C & I>1 Current Set I>1 Trip C IC2H Start & Timer Settings I>1 Start I> Blocking 2H Blocks I>1 2H 1PH Block I>1 Trip I2H Any Start Notes: This diagram does not show all stages. Other stages follow similar I> Blocking 2H Blocks I>1 AR blocking is only available for stages 3, 4 and 6 2H 1PH Block I>1 Timer Block AR Blk Main Prot I> Blocking AR Blocks I>3 AR blocking available for DT-only stages V00601

3.2 NON-DIRECTIONAL OVERCURRENT LOGIC

Figure 35: Non-directional Overcurrent Logic diagram

Phase Overcurrent Modules are level detectors that detect when the current magnitude exceeds a set threshold. When this happens, a Start signal is generated unless it is inhibited by a blocking signal. This Start signal initiates the timer module, which can be configured as an IDMT timer or DT timer, depending on the stage number. The Start signal is also available for use in the PSL. For each stage, there are three Phase Overcurrent Modules, one for each phase. The three Start signals from each of these phases are combined to form a 3-phase Start signal.

The Start signals can be blocked by the Second Harmonic blocking function; on a per phase basis (single-phase blocking) or for all three phases at once (three-phase blocking). The relevant bits are set in the *I*> *Blocking* cell and this is combined with the relevant second harmonic blocking DDBs.

The timer can be configured with several settings depening on which type of timer is selected. Taking stage 1 as an example:

The setting *I>1 Time Delay* sets the DT time delay

The setting *I>1 TMS* sets the Time Multiplier setting for IEC IDMT curves

The setting *I>1 Time Dial* sets the Time Multiplier setting for IEEE/US IDMT curves

The setting *I>1 DT Adder* adds a fixed time delay to the IDMT operate characteristic

The setting I>1 tRESET determines the reset time for the DT characteristic

The outputs of the timer modules are the single-phase trip signals. These trip signals are combined to form a 3-phase Trip signal.

The timer modules can be blocked by a Phase Overcurrent Timer Block (for example I>1 Timer Block).

For DT-only stages, the DT timer can be blocked by the Autoreclose function. An Autoreclose blocking signal is produced by the DDB signal **AR Blk Main Prot** and the relevant settings in the **I> Blocking** cell.

3.3 DIRECTIONAL ELEMENT

If fault current can flow in both directions through a protected location, you will need to use a directional overcurrent element to determine the direction of the fault. Once the direction has been determined the device can decide whether to allow tripping or to block tripping. To determine the direction of a phase overcurrent fault, the device must compare the phase angle of the fault current with that of a known reference quantity. The phase angle of this known reference quantity must be independent of the faulted phase. Typically this will be the line voltage between the other two phases.

The phase fault elements of the IEDs are internally polarized by the quadrature phase-phase voltages, as shown in the table below:

Phase of protection	Operate current	Polarizing voltage
A Phase	IA	VBC
B Phase	IB	VCA
C Phase	IC	VAB

Under system fault conditions, the fault current vector lags its nominal phase voltage by an angle depending on the system X/R ratio. The IED must therefore operate with maximum sensitivity for currents lying in this region. This is achieved by using the IED characteristic angle (RCA). This is the angle by which the current applied to the IED must be displaced from the voltage applied to the IED to obtain maximum sensitivity.

The device provides a setting *I*> *Char Angle*, which is set globally for all overcurrent stages. It is possible to set characteristic angles anywhere in the range -95° to $+95^{\circ}$.

A directional check is performed based on the following criteria:

Directional forward

-90° < (angle(I) - angle(V) - RCA) < 90°

Directional reverse

-90° > (angle(I) - angle(V) - RCA) > 90°

For close up three-phase faults, all three voltages will collapse to zero and no healthy phase voltages will be present. For this reason, the device includes a synchronous polarisation feature that stores the pre-fault voltage information and continues to apply this to the directional overcurrent elements for a time period of 3.2 seconds. This ensures that either instantaneous or time-delayed directional overcurrent elements will be allowed to operate, even with a three-phase voltage collapse.

3.3.1 DIRECTIONAL OVERCURRENT LOGIC

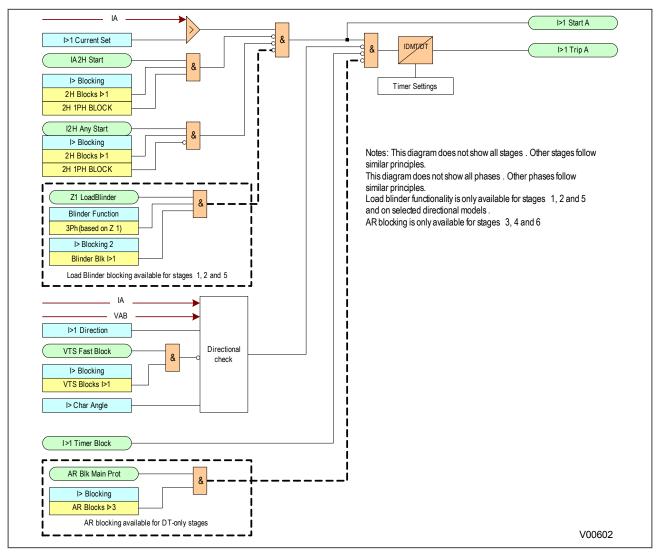


Figure 36: Directional Overcurrent Logic diagram (Phase A shown only)

Voltage Transformer Supervision (VTS) can be used to block operation of directional overcurrent elements.

This is achieved using the *I>Blocking* cell. When the relevant bit is set to 1, operation of the VTS will block the stage if directionalised. When set to 0, the stage will revert to non-directional upon operation of the VTS.

3.4 RECONSTRUCTION OF MISSING PHASE CURRENT

The P144 relay is designed to function with inputs from only 2 phase CTs and one core balance CT (CBCT). Since only two phases are presented to the relay, the relay must derive the missing phase current using the available phase and earth currents. The missing phase current is selectable in the CT AND VT RATIO column with the I Derived Phase setting. This setting may have a value of, IA, IB, IC or None, with IB being the default value.

The missing phase is calculated using one of the following equations:

$$Current \ IA = \left(\frac{ISEF \ x \ ISEF \ CT \ Ratio}{PHASE \ CT \ Ratio}\right) - (IB + IC)$$

$$Current \ IB = \left(\frac{ISEF \ x \ ISEF \ CT \ Ratio}{PHASE \ CT \ Ratio}\right) - (IA + IC)$$

$$Current \ IC = \left(\frac{ISEF \ x \ ISEF \ CT \ Ratio}{PHASE \ CT \ Ratio}\right) - (IA + IB)$$

The dynamic range of SEF current input is limited to 2In in order to give greater accuracy for small earth fault currents. However, in the event of a cross country fault the earth fault current may exceed 2In, which may limit the effectiveness of the earth fault protection. To improve the relay's dynamic range, it is recommended that the standard earth fault input (EF1) be wired in series with the SEF input. The dynamic range of the EF1 input is limited to 64In. This then allows the EF1 protection to provide the high set protection instead of the SEF input.

Although the equations above indicate that the missing phase current is derived from the ISEF input, the relay actually selects the highest of either ISEF or EF1. In the event of a cross country fault, the ISEF input is likely to saturate, thus the highest current will be EF1. In order for this technique to function correctly it is essential that the E/F and SEF CT ratios are set the same.

3.5 APPLICATION NOTES

3.5.1 PARALLEL FEEDERS

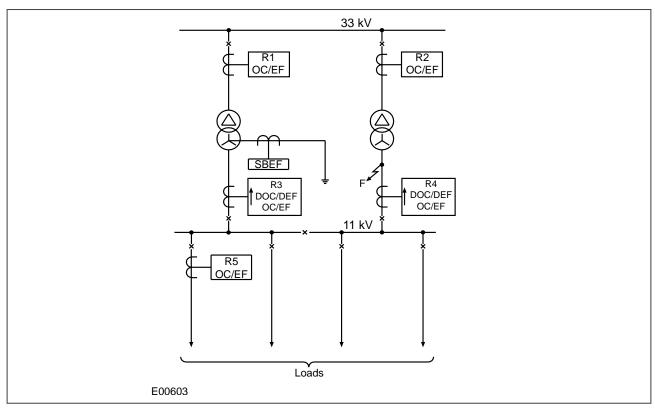


Figure 37: Typical distribution system using parallel transformers

In the application shown in the diagram, a fault at 'F' could result in the operation of both R3 and R4 resulting in the loss of supply to the 11 kV busbar. Hence, with this system configuration, it is necessary to apply directional protection devices at these locations set to 'look into' their respective transformers. These devices should co-

ordinate with the non-directional devices, R1 and R2, to ensure discriminative operation during such fault conditions.

In such an application, R3 and R4 may commonly require non-directional overcurrent protection elements to provide protection to the 11 kV busbar, in addition to providing a back-up function to the overcurrent devices on the outgoing feeders (R5).

For this application, stage 1 of the R3 and R4 overcurrent protection would be set to non-directional and time graded with R5, using an appropriate time delay characteristic. Stage 2 could then be set to directional (looking back into the transformer) and also have a characteristic which provides correct co-ordination with R1 and R2. Directionality for each of the applicable overcurrent stages can be set in the directionality cells (*I>1 Direction*).

Note:

The principles outlined for the parallel transformer application are equally applicable for plain feeders that are operating in parallel.

3.5.2 RING MAIN ARRANGEMENTS

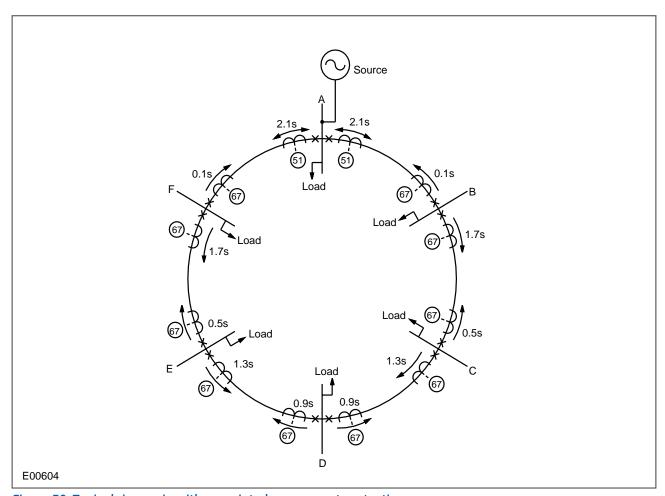


Figure 38: Typical ring main with associated overcurrent protection

In a ring main arrangement, current may flow in either direction through the various device locations, therefore directional overcurrent devices are needed to achieve correct discrimination.

The normal grading procedure for overcurrent devices protecting a ring main circuit is to consider the ring open at the supply point and to grade the devices first clockwise and then anti-clockwise. The arrows shown at the various device locations depict the direction for forward operation of the respective devices (i.e. the directional devices are set to look into the feeder that they are protecting).

The diagram shows typical time settings (assuming definite time co-ordination is used), from which it can be seen that any faults on the interconnections between stations are cleared discriminatively by the devices at each end of the feeder.

Any of the overcurrent stages may be configured to be directional and co-ordinated, but bear in mind that IDMT characteristics are not selectable on all the stages.

3.5.3 SETTING GUIDELINES

Standard principles should be applied in calculating the necessary current and time settings. The example detailed below shows a typical setting calculation and describes how the settings are applied.

This example is for a device feeding a LV switchboard and makes the following assumptions:

- CT Ratio = 500/1
- Full load current of circuit = 450A
- Slowest downstream protection = 100A Fuse

The current setting on the device must account for both the maximum load current and the reset ratio, therefore:

I> must be greater than: 450/drop-off = 450/0.95 = 474A.

The device allows the current settings to be applied in either primary or secondary quantities. This is done by setting the *Setting Values* cell of the *CONFIGURATION* column. When this cell is set to primary, all phase overcurrent setting values are scaled by the programmed CT ratio.

In this example, assuming primary currents are to be used, the ratio should be programmed as 500/1.

The required setting is therefore 0.95A in terms of secondary current or 475A in terms of primary.

A suitable time delayed characteristic will now need to be chosen. When co-ordinating with downstream fuses, the applied characteristic should be closely matched to the fuse characteristic. Therefore, assuming IDMT co-ordination is to be used, an Extremely Inverse (EI) characteristic would normally be chosen. This is found under the *I>1 Function* cell as *IEC E Inverse*.

Finally, a suitable time multiplier setting (TMS) must be calculated and entered in cell I>1 TMS.

3.5.4 SETTING GUIDELINES (DIRECTIONAL ELEMENT)

The applied current settings for directional overcurrent devices are dependent upon the application in question. In a parallel feeder arrangement, load current is always flowing in the non-operate direction. Hence, the current setting may be less than the full load rating of the circuit.

You need to observe some setting constraints when applying directional overcurrent protection at the receivingend of parallel feeders. These minimum safe settings are designed to ensure that there is no possibility of undesired tripping during clearance of a source fault. For a linear system load, these settings are as follows:

We recommend the following settings to ensure that there is no possibility of malaoperation:

- Parallel plain feeders: Set to 50% pre-fault load current
- Parallel transformer feeders: Set to 87% pre-fault load current

In a ring main application, the load current can flow in either direction. The current setting must be above the maximum load current.

The required characteristic angle settings for directional devices depend on the application. We recommend the following settings:

- Plain feeders, or applications with an earthing point behind the device location, should use a +30° RCA setting
- Transformer feeders, or applications with a zero sequence source in front of the device location, should use a +45° RCA setting

Although it is possible to set the RCA to exactly match the system fault angle, we recommend that you adhere to the above guidelines, as these settings provide satisfactory performance and stability under a wide range of system conditions.

4 VOLTAGE DEPENDENT OVERCURRENT ELEMENT

An overcurrent protection scheme is co-ordinated throughout a system such that cascaded operation is achieved. This means that if for some reason a downstream circuit breaker fails to trip for a fault condition, the next upstream circuit breaker should trip.

However, where long feeders are protected by overcurrent protection, the detection of remote phase-to-phase faults may prove difficult due to the fact that the current pick-up of phase overcurrent elements must be set above the maximum load current, thereby limiting the minimum sensitivity.

If the current seen by a local device for a remote fault condition is below its overcurrent setting, a voltage dependent element may be used to increase the sensitivity to such faults. As a reduction in system voltage will occur during overcurrent conditions, this may be used to enhance the sensitivity of the overcurrent protection by reducing the pick up level.

Voltage dependent overcurrent devices are often applied in generator protection applications in order to give adequate sensitivity for close up fault conditions. The fault characteristic of this protection must then co-ordinate with any of the downstream overcurrent devices that are responsive to the current decrement condition. It therefore follows that if the device is to be applied to an outgoing feeder from a generator station, the use of voltage dependent overcurrent protection in the feeder device may allow better co-ordination with the Voltage Dependent device on the generator.

4.1 VOLTAGE DEPENDENT OVERCURRENT PROTECTION IMPLEMENTATION

Voltage Dependent Overcurrent Protection (VDep OC) is set in the *OVERCURRENT* column of the relevant settings group, under the sub-heading *V DEPENDANT O/C*.

The function is available for stages 1, 2 and 5 of the main overcurrent element. When VDep OC is enabled, the overcurrent threshold setting is modified when the voltage falls below a set threshold.

If voltage dependant overcurrent operation is selected, the element can be set in one of two modes, voltage controlled overcurrent or voltage restrained overcurrent.

4.1.1 VOLTAGE CONTROLLED OVERCURRENT PROTECTION

In Voltage Controlled Operation (VCO) mode of operation, the under voltage detector is used to produce a step change in the current setting, when the voltage falls below the voltage setting **V Dep OC V<1 Set**. The operating characteristic of the current setting when voltage controlled mode is selected is as follows:

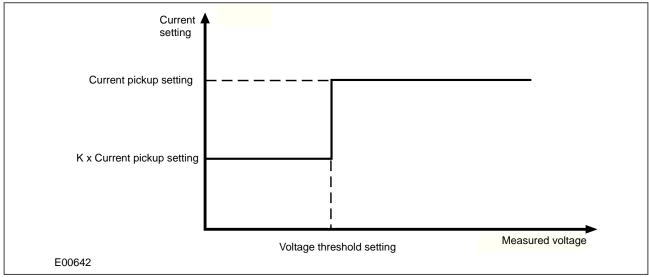


Figure 39: Modification of current pickup level for voltage controlled overcurrent protection

4.1.2 VOLTAGE RESTRAINED OVERCURRENT PROTECTION

In Voltage Restrained Operation (VRO) mode the effective operating current of the protection element is continuously variable as the applied voltage varies between two voltage thresholds. This protection mode is considered to be better suited to applications where the generator is connected to the system via a generator transformer.

With indirect connection of the generator, a solid phase-phase fault on the local busbar will result in only a partial phase-phase voltage collapse at the generator terminals.

The voltage-restrained current setting is related to measured voltage as follows:

- If V is greater than V<1, the current setting (Is) = I>
- If V is greater than V<2 but less than V<1, the current setting (Is) =

$$KI > +(I > -KI)\frac{V - V < 2}{V < 1 - V < 2}$$

• If V is less than **V<2**, the current setting (Is) = K.I>

where:

- I> = Over current stage setting
- Is = Current setting at voltage V
- V = Voltage applied to relay element
- V<1 = V Dep OC V<1 Set
- V<2 = V Dep OC V<2 Set

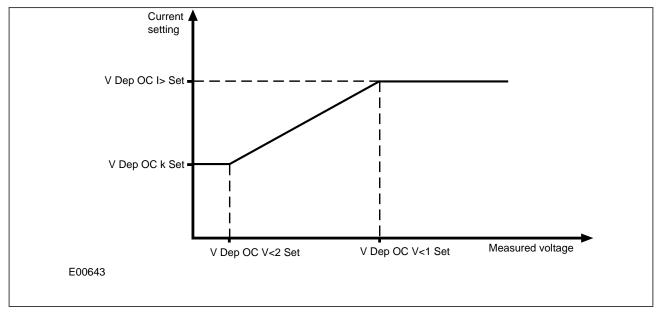


Figure 40: Modification of current pickup level for voltage restrained overcurrent protection

V Dep OC Status VCO I>1 & Vdep OC Start AB VRO I>1 V Dep OC V<1 Set I>1 Current Set Applied Current Threshold V Dep OC k Set VAB V Dep OC V<1 Set I>1 Current Set VAB V Dep OC V<2 Set I>1 Current Set V Dep OC k Set VAB V Dep OC V<2 Set VAB Note: This diagram does not show all stages. Other stages follow V Dep OC V<1 Set similar principles. V Dep OC k Set Function al I>1 Current Set Operator V00644

4.2 VOLTAGE DEPENDENT OVERCURRENT LOGIC

Figure 41: Voltage dependant overcurrent logic (Phase A to phase B)

The current threshold setting for the Overcurrent function is determined by the voltage.

If the voltage is greater than **V Dep OC V<1 Set**, the normal overcurrent setting **I>1 current set** is used. this applies to both VCO and VRO modes.

If the voltage is less than **V Dep OC V<1 Set** AND it is in VCO mode, the overcurrent setting **I>1 current set** is multiplied by the factor set by **V Dep OC k set**.

If the voltage is less than **V Dep OC V<2 Set** AND it is in VRO mode, the overcurrent setting **I>1 current set** is multiplied by the factor set by **V Dep OC k set**.

If the voltage is between **V Dep OC V<1 Set** and **V Dep OC V<2 Set** AND it is in VRO mode, the overcurrent setting is multiplied by a functional operator to determine the setting.

4.3 APPLICATION NOTES

4.3.1 SETTING GUIDELINES

The **V Dep OC k set** setting should be set low enough to allow operation for remote phase-to-phase faults, typically:

$$k = \frac{I_F}{1.2I} >$$

where:

- $I_F = Minimum fault current expected for the remote fault$
- I> = Phase current setting for the element to have VCO control

Example

If the overcurrent device has a setting of 160% In, but the minimum fault current for the remote fault condition is only 80% In, then the required k factor is given by:

$$k = \frac{0.8}{1.6 \times 1.2} = 0.42$$

The voltage threshold, **V Dep OC V<(n) Set** setting would be set below the lowest system voltage that may occur under normal system operating conditions, whilst ensuring correct detection of the remote fault.

5 CURRENT SETTING THRESHOLD SELECTION

The Phase Overcurrent protection threshold setting can be influenced by the Cold Load Pickup (CLP)and the Voltage Dependent Overcurrent (V DepOC) functions, should this functionality be used.

The Overcurrent function selects the threshold setting according to the following diagram:

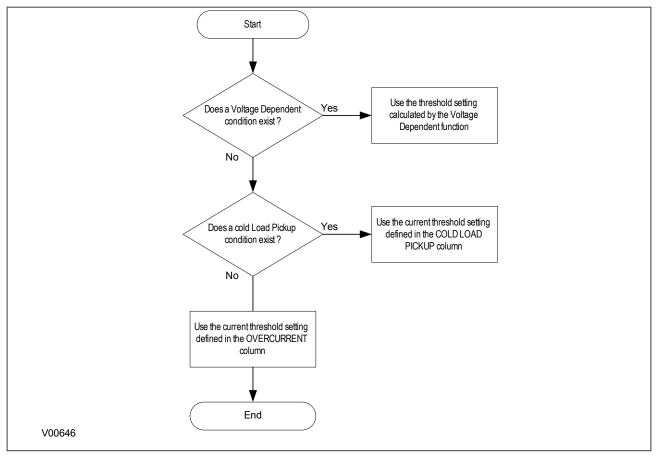


Figure 42: Selecting the current threshold setting

6 COLD LOAD PICKUP

When a feeder circuit breaker is closed in order to energise a load, the current levels that flow for a period of time following energisation may be far greater than the normal load levels. Consequently, overcurrent settings that have been applied to provide overcurrent protection may not be suitable during this period of energisation (cold load), as they may initiate undesired tripping of the circuit breaker. This scenario can be prevented with Cold Load Pickup (CLP) functionality.

The Cold Load Pick-Up (CLP) logic works by either:

- Blocking one or more stages of the overcurrent protection for a set duration
- Raising the overcurrent settings of selected stages, for the cold loading period.

The CLP logic therefore provides stability, whilst maintaining protection during the start-up.

6.1 IMPLEMENTATION

Cold Load Pickup Protection is configured in the COLD LOAD PICKUP column of the relevant settings group.

This function acts upon the following protection functions:

- All overcurrent stages (both non-directional and directional if applicable)
- The first stage of Earth Fault 1 (both non-directional and directional if applicable)
- The first stage of Earth Fault 2 (both non-directional and directional if applicable)

The principle of operation is identical for the 3-phase overcurrent protection and the first stages of Earth Fault overcurrent protection for both EF1 and EF2.

CLP operation occurs when the circuit breaker remains open for a time greater than **tcold** and is subsequently closed. CLP operation is applied after **tcold** and remains for a set time delay of **tclp** following closure of the circuit breaker. The status of the circuit breaker is provided either by means of the CB auxiliary contacts or by means of an external device via logic inputs. Whilst CLP operation is in force, the CLP settings are enabled After the time delay **tclp** has elapsed, the normal overcurrent settings are applied and the CLP settings are disabled.

If desired, instead of applying different current setting thresholds for the cold load time, it is also possible to completely block the overcurrent operation during this time, for any of the overcurrent stages.

Voltage-dependent operation can also affect the overcurrent settings. If a Voltage Dependent condition arises, this takes precedence over the CLP function. If the CLP condition prevails and the Voltage Dependent function resets, the device will operate using the CLP settings. Time-delayed elements are reset to zero if they are disabled during the transitions between normal settings and CLP settings.

6.2 CLP LOGIC

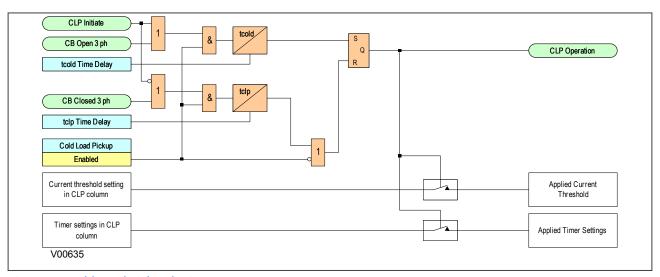


Figure 43: Cold Load Pickup logic

The CLP Operation signal indicates that CLP logic is in operation. This only happens when CLP is enabled AND CLP is initiated either externally or from a CB Open condition after the *tcold* period has elapsed. The CLP Operation indicator goes low when CLP is disabled or when the external CLP trigger is removed or when there is a CB closed condition.

tcold and **tclp** are initiated via the CB open and CB closed signals generated within the device. These signals are produced by connecting auxiliary contacts from the circuit breaker or starting device to the IED's opto-inputs

If dual CB contacts are not available (one for Open (52a) and for Close (52b)) you can configure the device to be driven from a single contact (either 52a or 52b). The device would then simply invert one signal to provide the other. This option is available using the *CB status input* cell in the *CB CONTROL* column. The setting can be set to *None*, 52a, 52b or 52a and 52b.

6.3 APPLICATION NOTES

6.3.1 CLP FOR RESISTIVE LOADS

A typical example of where CLP logic may be used is for resistive heating loads such as such as air conditioning systems. Resistive loads typically offer less resistance when cold than when warm, hence the start-up current will be higher.

To set up the CLP, you need to select Enable from the I> status option to enable the settings of the temporary current and time settings. These settings should be chosen in accordance with the expected load profile. Where it is not necessary to alter the setting of a particular stage, the CLP settings should be set to the same level as the standard overcurrent settings.

It may not be necessary to alter the protection settings following a short supply interruption. In this case a suitable *tcold* timer setting can be used.

6.3.2 CLP FOR MOTOR FEEDERS

In general, a dedicated motor protection device would protect feeders supplying motor loads. However, if CLP logic is available in a feeder device, this may be used to modify the overcurrent settings during start-up.

Depending on the magnitude and duration of the motor starting current, it may be sufficient to simply block operation of instantaneous elements. If the start duration is long, the time-delayed protection settings may also need to be raised. A combination of both blocking and raising of the overcurrent settings may be adopted. The CLP overcurrent settings in this case must be chosen with regard to the motor starting characteristic.

This may be useful where instantaneous earth fault protection needs to be applied to the motor. During motor start-up conditions, it is likely that incorrect operation of the earth fault element would occur due to asymmetric CT saturation. This is due to the high level of starting current causing saturation of one or more of the line CTs feeding the overcurrent/earth fault protection. The resultant transient imbalance in the secondary line current quantities is therefore detected by the residually connected earth fault element. For this reason, it is normal to either apply a nominal time delay to the element, or to use a series stabilising resistor.

The CLP logic may be used to allow reduced operating times or current settings to be applied to the earth fault element under normal running conditions. These settings could then be raised prior to motor starting, by means of the logic.

6.3.3 CLP FOR SWITCH ONTO FAULT CONDITIONS

In some feeder applications, fast tripping may be required if a fault is already present on the feeder when it is energised. Such faults may be due to a fault condition not having been removed from the feeder, or due to earthing clamps having been left on following maintenance. In either case, it is desirable to clear the fault condition quickly, rather than waiting for the time delay imposed by IDMT overcurrent protection.

The CLP logic can cater for this situation. Selected overcurrent/earth fault stages could be set to instantaneous operation for a defined period following circuit breaker closure (typically 200 ms). Therefore, instantaneous fault clearance would be achieved for a switch onto fault (SOTF) condition.

7 SELECTIVE LOGIC

With Selective Logic you can use the Start signals to control the time delays of upstream IEDs, as an alternative to simply blocking them. This provides an alternative approach to achieving non-cascading types of overcurrent scheme.

7.1 SELECTIVE LOGIC IMPLEMENTATION

Selective Logic is set in the SELECTIVE LOGIC column of the relevant settings group.

The Selective Logic function works by temporarily increasing the time delay settings of the chosen overcurrent elements. This logic is initiated by issuing signals to an upstream IED.

This function acts on the following protection functions:

- Non-Directional/Directional phase overcurrent (3rd, 4th and 6th stages)
- Non-Directional/Directional earth fault 1 (3rd and 4th stages)
- Non-Directional/Directional earth fault 2 (3rd and 4th stages)
- Non-Directional/Directional sensitive earth fault (3rd and 4th stages)

Note:

In the event of a conflict between Selective Logic and CLP, Selective Logic takes precedence.

7.2 SELECTIVE LOGIC DIAGRAM

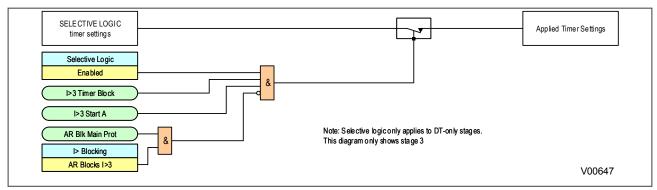


Figure 44: Selective Logic

The logic diagram is shown for overcurrent phase A, but is valid for all three phases for each of the stages. The principle of operation is also identical for earth fault protection.

When the selective logic function is enabled, the action of the blocking input is as follows:

No block applied

In the event of a fault condition that continuously asserts the start output, the function will assert a trip signal after the normal time delay has elapsed.

Logic input block applied

In the event of a fault condition that continuously asserts the start output, the function will assert a trip signal after the selective logic time delay has elapsed.

Auto-reclose input block applied

In the event of a fault condition that continuously asserts the start output, when an auto-reclose block is applied the function will not trip. The auto-reclose block also overrides the logic input block and will block the selective logic timer.

Note:

The Auto-reclose function outputs two signals that block protection, namely; AR BIk Main Prot and AR BIk SEF Prot.

AR Blk Main Prot is common to Phase Overcurrent, Earth Fault 1 and Earth Fault 2, whereas **AR Blk SEF Prot** is used for SEF protection.

8 TIMER SETTING SELECTION

The timer settings used depend on whether there is a Selective Overcurrent condition or a Cold Load Pickup condition (if this functionality is used). The protection function selects the settings according to the following flow diagram:

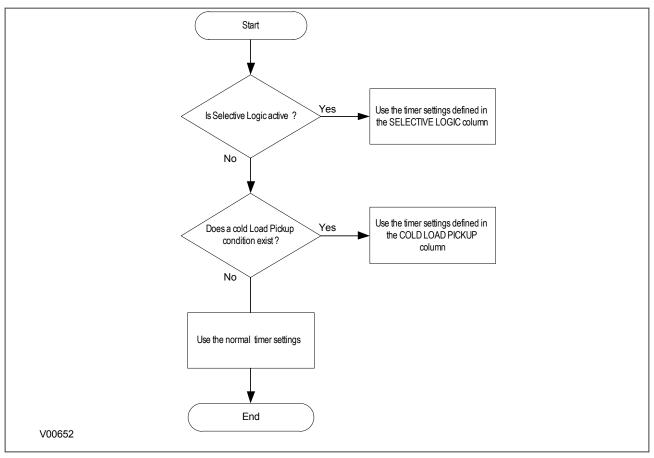


Figure 45: Selecting the timer settings

9 NEGATIVE SEQUENCE OVERCURRENT PROTECTION

When applying standard phase overcurrent protection, the overcurrent elements must be set significantly higher than the maximum load current. This limits the element's sensitivity. Most protection schemes also use an earth fault element operating from residual current, which improves sensitivity for earth faults. However, certain faults may arise which can remain undetected by such schemes. Negative Phase Sequence Overcurrent elements can help in such cases.

Any unbalanced fault condition will produce a negative sequence current component. Therefore, a negative phase sequence overcurrent element can be used for both phase-to-phase and phase-to-earth faults. Negative Phase Sequence Overcurrent protection offers the following advantages:

- Negative phase sequence overcurrent elements are more sensitive to resistive phase-to-phase faults, where phase overcurrent elements may not operate.
- In certain applications, residual current may not be detected by an earth fault element due to the system
 configuration. For example, an earth fault element applied on the delta side of a delta-star transformer is
 unable to detect earth faults on the star side. However, negative sequence current will be present on both
 sides of the transformer for any fault condition, irrespective of the transformer configuration. Therefore, a
 negative phase sequence overcurrent element may be used to provide time-delayed back-up protection for
 any uncleared asymmetrical faults downstream.

9.1 NEGATIVE SEQUENCE OVERCURRENT PROTECTION IMPLEMENTATION

Negative Sequence Overcurrent Protection is implemented in the *NEG SEQ O/C* column of the relevant settings group.

The product provides four stages of negative sequence overcurrent protection with independent time delay characteristics.

Stages 1, 2 provide a choice of operate and reset characteristics, where you can select between:

- A range of standard IDMT (Inverse Definite Minimum Time) curves
- A range of User-defined curves
- DT (Definite Time)

For stage 1, this is achieved using the following settings:

- *I2>1 Function* for the overcurrent operate characteristic
- 12>1 Reset Char for the overcurrent reset characteristic
- I2>1 Usr RstChar for the reset characteristic for user-defined curves

The setting names for other stages follow the same principles.

The IDMT-equipped stages, (1 and 2) also provide a Timer Hold facility. Stage 1, for example, is configured using the cells *I2>1 tRESET*. This setting is not applicable for curves based on the IEEE standard.

Stages 3 and 4 have definite time characteristics only.

9.2 NON-DIRECTIONAL NEGATIVE SEQUENCE OVERCURRENT LOGIC

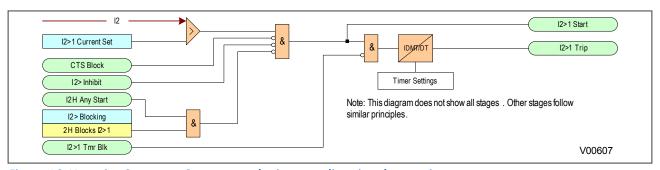


Figure 46: Negative Sequence Overcurrent logic - non-directional operation

For Negative Phase Sequence Overcurrent Protection, the energising quantitity *I2>* is compared with the threshold voltage *I2>1 Current Set*. If the value exceeds this setting a Start signal (*I2>1 Start*) is generated, provided there are no blocks.

The function can be blocked if a CTS or second harmonic condition is detected.

The *I2>1 Start* signal is fed into a timer to produce the *I2>1 trip* signal. The timer can be blocked by the timer block signal *I2>1 Tmr Blk*.

This diagram and description applies to each stage.

9.3 COMPOSITE EARTH FAULT START LOGIC

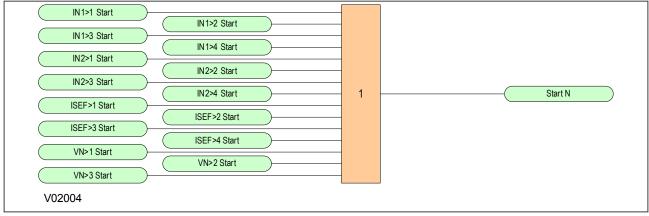


Figure 47: Composite Earth Fault Start Logic

9.4 DIRECTIONAL ELEMENT

Where negative phase sequence current may flow in either direction, directional control should be used.

Directionality is achieved by comparing the angle between the negative phase sequence voltage and the negative phase sequence current. A directional element is available for all of the negative sequence overcurrent stages. This is found in the *I2> Direction* cell for the relevant stage. It can be set to non-directional, directional forward, or directional reverse.

A suitable characteristic angle setting (*I2> Char Angle*) is chosen to provide optimum performance. This setting should be set equal to the phase angle of the negative sequence current with respect to the inverted negative sequence voltage (–**V2**), in order to be at the centre of the directional characteristic.

12 I2>1 Start 12>1 Current Set IDM7/DT 12>1 Trip CTS Block I2> Inhibit Timer Settings I2H Any Start I2> Blocking 2H Blocks I2>1 Note: This diagram does not show all stages. Other stages follow I2>1 Direction I2> V2pol Set Directional VTS Slow Block check I2> Blocking & VTS Blocks I2>1 I2> Char Angle I2>1 Tmr Blk V00608

9.4.1 DIRECTIONAL NEGATIVE SEQUENCE OVERCURRENT LOGIC

Figure 48: Negative Sequence Overcurrent logic - directional operation

Directionality is achieved by comparing the angle between the negative phase sequence voltage and the negative phase sequence current. The element may be selected to operate in either the forward or reverse direction. A suitable characteristic angle setting (*I2> Char Angle*) is chosen to provide optimum performance. This setting should be set equal to the phase angle of the negative sequence current with respect to the inverted negative sequence voltage (–V2), in order to be at the centre of the directional characteristic.

For the negative phase sequence directional elements to operate, the device must detect a polarising voltage above a minimum threshold, *I2> V2pol Set*. This must be set in excess of any steady state negative phase sequence voltage. This may be determined during the commissioning stage by viewing the negative phase sequence measurements in the device.

When the element is selected as directional (directional devices only), a VTS Block option is available. When the relevant bit is set to 1, operation of the Voltage Transformer Supervision (VTS) will block the stage. When set to 0, the stage will revert to non-directional.

9.5 APPLICATION NOTES

9.5.1 SETTING GUIDELINES (CURRENT THRESHOLD)

A negative phase sequence element can be connected in the primary supply to the transformer and set as sensitively as required to protect for secondary phase-to-earth or phase-to-phase faults. This function will also provide better protection than the phase overcurrent function for internal transformer faults. The NPS overcurrent protection should be set to coordinate with the low-side phase and earth elements for phase-to-earth and phase-to-phase faults.

The current pick-up threshold must be set higher than the negative phase sequence current due to the maximum normal load imbalance. This can be set practically at the commissioning stage, making use of the measurement function to display the standing negative phase sequence current. The setting should be at least 20% above this figure.

Where the negative phase sequence element needs to operate for specific uncleared asymmetric faults, a precise threshold setting would have to be based on an individual fault analysis for that particular system due to the complexities involved. However, to ensure operation of the protection, the current pick-up setting must be set approximately 20% below the lowest calculated negative phase sequence fault current contribution to a specific remote fault condition.

9.5.2 SETTING GUIDELINES (TIME DELAY)

Correct setting of the time delay for this function is vital. You should also be very aware that this element is applied primarily to provide back-up protection to other protection devices or to provide an alarm. It would therefore normally have a long time delay.

The time delay set must be greater than the operating time of any other protection device (at minimum fault level) that may respond to unbalanced faults such as phase overcurrent elements and earth fault elements.

9.5.3 SETTING GUIDELINES (DIRECTIONAL ELEMENT)

Where negative phase sequence current may flow in either direction through an IED location, such as parallel lines or ring main systems, directional control of the element should be employed (VT models only).

Directionality is achieved by comparing the angle between the negative phase sequence voltage and the negative phase sequence current and the element may be selected to operate in either the forward or reverse direction. A suitable relay characteristic angle setting (*I2> Char Angle*) is chosen to provide optimum performance. This setting should be set equal to the phase angle of the negative sequence current with respect to the inverted negative sequence voltage (–V2), in order to be at the centre of the directional characteristic.

The angle that occurs between V2 and I2 under fault conditions is directly dependent on the negative sequence source impedance of the system. However, typical settings for the element are as follows:

- For a transmission system the relay characteristic angle (RCA) should be set equal to -60°
- For a distribution system the relay characteristic angle (RCA) should be set equal to -45°

For the negative phase sequence directional elements to operate, the device must detect a polarising voltage above a minimum threshold, *I2> V2pol Set*. This must be set in excess of any steady state negative phase sequence voltage. This may be determined during the commissioning stage by viewing the negative phase sequence measurements in the device.

10 EARTH FAULT PROTECTION

Earth faults are overcurrent faults where the fault current flows to earth. Earth faults are the most common type of fault.

Earth faults can be measured directly from the system by means of:

- A separate current Transformer (CT) located in a power system earth connection
- A separate Core Balance Current Transformer (CBCT), usually connected to the SEF transformer input
- A residual connection of the three line CTs, where the Earth faults can be derived mathematically by summing the three measured phase currents.

Depending on the device model, it will provide one or more of the above means for Earth fault protection.

10.1 EARTH FAULT PROTECTION ELEMENTS

Earth fault protection is implemented in the columns EARTH FAULT 1 and EARTH FAULT 2 of the relevant settings group.

Each column contains an identical set of elements. *EARTH FAULT 1* (EF1) is used for earth fault current that is measured directly from the system (measured). *EARTH FAULT 2* (EF2) uses quantities derived internally from summing the three-phase currents.

The product provides four stages of Earth Fault protection with independent time delay characteristics, for each *EARTH FAULT* column.

Stages 1 and 2 provide a choice of operate and reset characteristics, where you can select between:

- A range of IDMT (Inverse Definite Minimum Time) curves
- A range of User-defined curves
- DT (Definite Time)

For the EF1 column, this is achieved using the cells:

- IN1>(n) Function for the overcurrent operate characteristics
- IN1>(n) Reset Char for the overcurrent reset characteristic
- IN1>(n) Usr RstChar for the reset characteristic for user-defined curves

For the EF2 column, this is achieved using the cells:

- IN2>(n) Function for the overcurrent operate characteristics
- IN2>(n) Reset Char for the overcurrent reset characteristic
- IN2>(n) Usr RstChar for the reset characteristic for user-defined curves

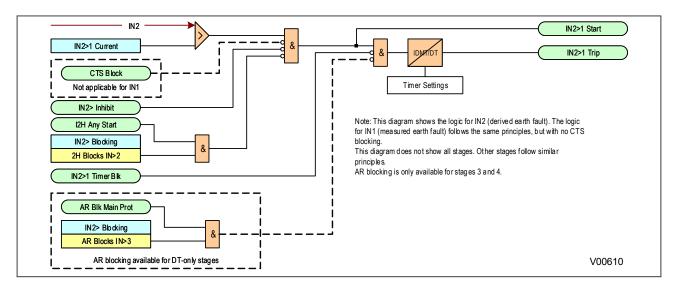
where (n) is the number of the stage.

Stages 1 and 2 provide a Timer Hold facility. This is configured using the cells **IN1>(n)** tReset for EF1 and **IN2>(n)** tReset for EF2.

Stages 3 and 4 can have definite time characteristics only.

The fact that both EF1 and EF2 elements may be enabled at the same time leads to a number of applications advantages. For example, some applications may require directional earth fault protection for upstream equipment and backup earth fault protection for downstream equipment. This can be achieved with a single IED, rather than two.

10.2 NON-DIRECTIONAL EARTH FAULT LOGIC



Note

- *1 If a CLP condition exists, the I>(n) Current Set threshold is taken from the COLD LOAD PICKUP column
- *2 Autoreclose blocking is only available for stages 3,4 and 6 and on selected models
- *3 The CTS blocking is not applicable for IN1, however this can be achieved using the PSL

Figure 49: Non-directional EF logic (single stage)

The Earth Fault current is compared with a set threshold (*IN1>(n) Current*) for each stage. If it exceeds this threshold, a Start signal is triggered, providing it is not blocked. This can be blocked by the second harmonic blocking function, or an Inhibit Earth Fault DDB signal.

The autoreclose logic can be set to block the Earth Fault trip after a prescribed number of shots (set in *AUTORECLOSE* column). This is achieved using the *AR Blk Main Prot* setting. this can also be blocked by the relevant timer block signal *IN1>(n)TimerBlk* DDB signal.

Earth Fault protection can follow the same IDMT characteristics as described in the Overcurrent Protection Principles section. Please refer to that section for details of IDMT characteristics.

The diagram and description also applies to the Earth Fault 2 element (IN2).

10.3 IDG CURVE

The IDG curve is commonly used for time delayed earth fault protection in the Swedish market. This curve is available in stage 1 of the Earth Fault protection.

The IDG curve is represented by the following equation:

$$t_{op} = 5.8 - 1.35 \log_e \left(\frac{I}{IN > Setting}\right)$$

where:

t_{op} is the operating time

I is the measured current

IN> Setting is an adjustable setting, which defines the start point of the characteristic

Note:

Although the start point of the characteristic is defined by the "IN>" setting, the actual current threshold is a different setting called "IDG Is". The "IDG Is" setting is set as a multiple of "IN>".

Note:

When using an IDG Operate characteristic, DT is always used with a value of zero for the Rest characteristic.

An additional setting "IDG Time" is also used to set the minimum operating time at high levels of fault current.

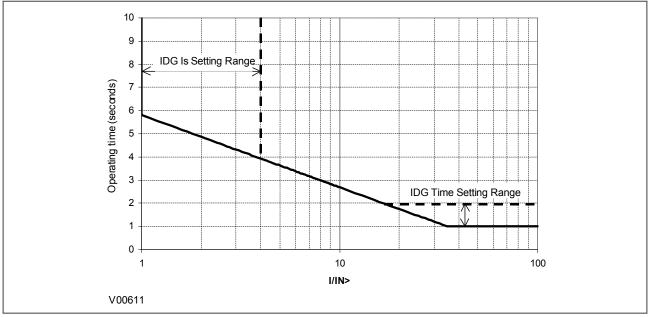


Figure 50: IDG Characteristic

10.4 DIRECTIONAL ELEMENT

If Earth fault current can flow in both directions through a protected location, you will need to use a directional overcurrent element to determine the direction of the fault. Typical systems that require such protection are parallel feeders and ring main systems.

A directional element is available for all of the Earth Fault stages. These are found in the direction setting cells for the relevant stage. They can be set to non-directional, directional forward, or directional reverse.

Directional control can be blocked by the VTS element if required.

For standard earth fault protection, two options are available for polarisation; Residual Voltage (zero sequence) or Negative Sequence.

10.4.1 RESIDUAL VOLTAGE POLARISATION

With earth fault protection, the polarising signal needs to be representative of the earth fault condition. As residual voltage is generated during earth fault conditions, this quantity is commonly used to polarise directional earth fault elements. This is known as Zero Sequence Voltage polarisation, Residual Voltage polarisation or Neutral Displacement Voltage (NVD) polarisation.

Small levels of residual voltage could be present under normal system conditions due to system imbalances, VT inaccuracies, device tolerances etc. For this reason, the device includes a user settable threshold (*IN*> *VNPol set*), which must be exceeded in order for the DEF function to become operational. The residual voltage measurement provided in the *MEASUREMENTS 1* column of the menu may assist in determining the required threshold setting during the commissioning stage, as this will indicate the level of standing residual voltage present.

Note:

Residual voltage is nominally 180° out of phase with residual current. Consequently, the DEF elements are polarised from the "-Vres" quantity. This 180° phase shift is automatically introduced within the device.

The directional criteria with residual voltage polarisation is given below:

- Directional forward: -90° < (angle(IN) angle(VN + 180°) RCA) < 90°
- Directional reverse: -90° > (angle(IN) angle(VN + 180°) RCA) > 90°

Most of the models derive the Residual Voltage quantity internally, from the 3-phase voltage input supplied from either a 5-limb VT or three single-phase VTs.

The P144, however, measures this voltage from the residual voltage input which must be supplied from a suitable broken delta VT. This type of VT allows the passage of residual flux and consequently allows the device to derive the required residual voltage. The primary star point of the VT must be earthed. A three-limb VT has no path for residual flux and is therefore unsuitable to supply the device.

10.4.1.1 DIRECTIONAL EARTH FAULT LOGIC WITH RESIDUAL VOLTAGE POLARISATION

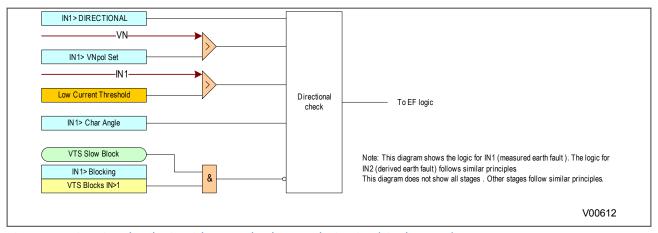


Figure 51: Directional EF logic with neutral voltage polarization (single stage)

Voltage Transformer Supervision (VTS) selectively blocks the directional protection or causes it to revert to non-directional operation. When selected to block the directional protection, VTS blocking is applied to the directional checking which effectively blocks the Start outputs as well.

10.4.2 NEGATIVE SEQUENCE POLARISATION

In some applications, the use of residual voltage polarisation may be not possible to achieve, or at the very least, problematic. For example, a suitable type of VT may be unavailable, or an HV/EHV parallel line application may present problems with zero sequence mutual coupling.

In such situations, the problem may be solved by using Negative Phase Sequence (NPS) quantities for polarisation. This method determines the fault direction by comparing the NPS voltage with the NPS current. The operating quantity, however, is still residual current.

This can be used for both the derived and measured standard earth fault elements. It requires a suitable voltage and current threshold to be set in cells *IN*> *V2pol set* and *IN*> *I2pol set* respectively.

Negative phase sequence polarising is not recommended for impedance earthed systems regardless of the type of VT feeding the relay. This is due to the reduced earth fault current limiting the voltage drop across the negative sequence source impedance to negligible levels. If this voltage is less than 0.5 volts the device will stop providing directionalisation.

The directional criteria with negative sequence polarisation is given below:

- Directional forward: -90° < (angle(I2) angle(V2 + 180°) RCA) < 90°
- Directional reverse: -90° > (angle(I2) angle(V2 + 180°) RCA) > 90°

10.4.2.1 DIRECTIONAL EARTH FAULT LOGIC WITH NPS POLARISATION

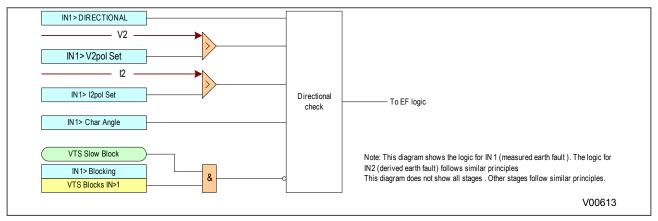


Figure 52: Directional Earth Fault logic with negative sequence polarisation (single stage)

Voltage Transformer Supervision (VTS) selectively blocks the directional protection or causes it to revert to non-directional operation. When selected to block the directional protection, VTS blocking is applied to the directional checking which effectively blocks the Start outputs as well.

10.5 APPLICATION NOTES

10.5.1 SETTING GUIDELINES (DIRECTIONAL ELEMENT)

With directional earth faults, the residual current under fault conditions lies at an angle lagging the polarising voltage. Hence, negative RCA settings are required for DEF applications. This is set in the cell *I* > *Char Angle* in the relevant earth fault menu.

We recommend the following RCA settings:

- Resistance earthed systems: 0°
- Distribution systems (solidly earthed): -45°
- Transmission systems (solidly earthed): -60°

10.5.2 PETERSON COIL EARTHED SYSTEMS

A Petersen Coil earthing system is used in compensated earthing systems, as well as being used in cases of high impedance earthing. Petersen Coil earthed systems (also called compensated or resonant systems) are commonly found in areas where the system consists mainly of rural overhead lines. They are particularly beneficial in locations which are subject to a high incidence of transient faults. In a Petersen Coil earthed system, the network is earthed via a reactor, whose reactance is tuned to be nominally equal to the total system capacitance to earth. Similar to insulated systems, if a single-phase to earth fault is applied to a Petersen Coil earthed system, under steady state conditions no earth fault current flows. The effectiveness of the method in reducing the current to zero is dependent on the accuracy of the tuning of the reactance value and any changes in system capacitance (for example due to system configuration changes) require changes to the coil reactance. In practice, perfect matching of the coil reactance to the system capacitance is difficult to achieve, so that a small earth fault current will flow.

In isolated and compensated earthed systems, if an earth fault current is below a certain level, then the fault will self-extinguish due to the low current magnitude. It therefore appears as a transient phenomenon. The figure below shows earth fault current levels, below which they self-extinguish on these types of system. Statistics

demonstrate that around 80% of earth faults in Petersen Coil earthed systems self-extinguish. This, in part, explains their popularity.

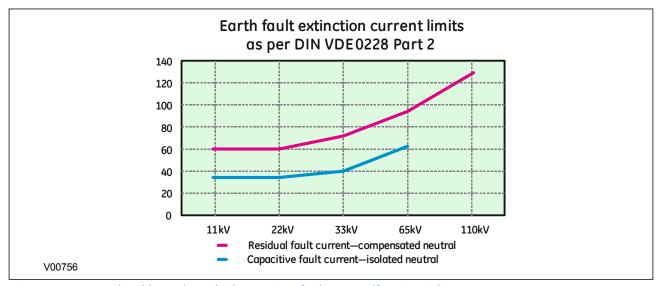


Figure 53: Current level (amps) at which transient faults are self-extinguishing

The following figure depicts a simple network earthed through a Petersen Coil reactance. It can be shown that if the reactor is correctly tuned, theoretically no earth fault current will flow.

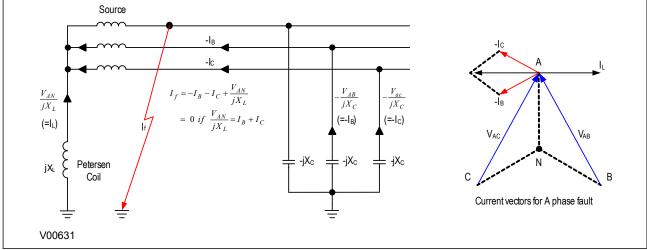


Figure 54: Earth fault in Petersen Coil earthed system

Consider a radial distribution system earthed using a Petersen Coil with a phase to earth fault on phase C, shown in the figure below:

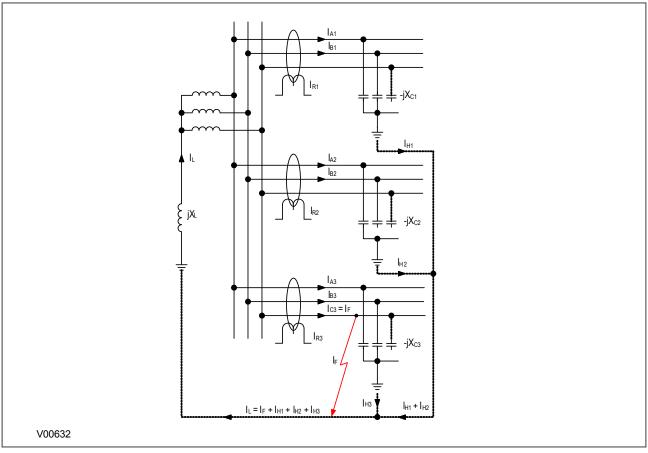


Figure 55: Distribution of currents during a Phase C fault

Assuming that no resistance is present in X_L or X_C , the resulting phasor diagrams will be as shown in the figure below:

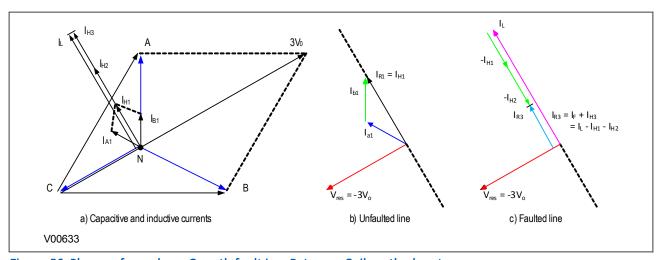


Figure 56: Phasors for a phase C earth fault in a Petersen Coil earthed system

It can be seen that:

- The voltage in the faulty phase reduces to almost 0V
- The healthy phases raise their phase to earth voltages by a factor of $\sqrt{3}$
- The triangle of voltages remains balanced
- The charging currents lead the voltages by 90°

Using a core-balance current transformer (CBCT), the current imbalances on the healthy feeders can be measured. They correspond to simple vector addition of I_{A1} and I_{B1} , I_{A2} and I_{B2} , I_{A3} and I_{B3} , and they lag the residual voltage by exactly 90°.

The magnitude of the residual current I_{R1} is equal to three times the steady-state charging current per phase. On the faulted feeder, the residual current is equal to $I_L - I_{H1} - I_{H2}$ (C). This is shown in the zero sequence network shown in the following figure:

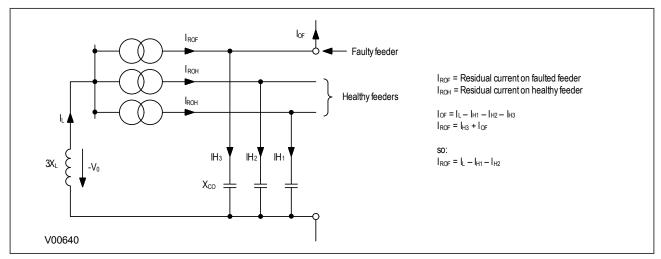


Figure 57: Zero sequence network showing residual currents

In practical cases, however, resistance is present, resulting in the following phasor diagrams:

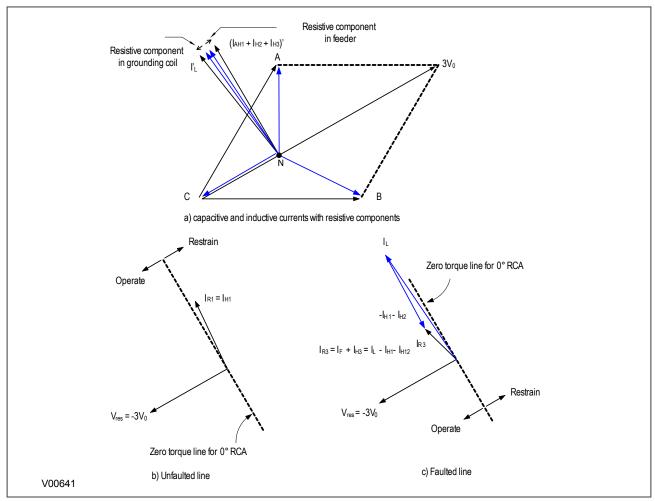


Figure 58: Phase C earth fault in Petersen Coil earthed system: practical case with resistance present

If the residual voltage is used as the polarising voltage, the residual current is phase shifted by an angle less than 90° on the faulted feeder, and greater than 90° on the healthy feeders. With an RCA of 0°, the healthy feeder residual current will fall in the 'restrain' area of the characteristic while the faulted feeder residual current falls in the 'operate' area.

Often, a resistance is deliberately inserted in parallel with the Petersen Coil to ensure a measurable earth fault current and increase the angular difference between the residual signals to reinforce the directional decision.

Directionality is usually implemented using a Wattmetric function, or a transient earth fault detection function (TEFD), rather than a simple directional function, since they are more sensitive. For further information about TEFD, refer to Transient Earth Fault Detection in the Current Protection Functions chapter.

10.5.3 SETTING GUIDELINES (COMPENSATED NETWORKS)

The directional setting should be such that the forward direction is looking down into the protected feeder (away from the busbar), with a 0° RCA setting.

For a fully compensated system, the residual current detected by the relay on the faulted feeder is equal to the coil current minus the sum of the charging currents flowing from the rest of the system. Further, the addition of the two healthy phase charging currents on each feeder gives a total charging current which has a magnitude of three times the steady state per phase value. Therefore, for a fully compensated system, the detected unbalanced current is equal to three times the per phase charging current of the faulted circuit. A typical setting may therefore be in the order of 30% of this value, i.e. equal to the per phase charging current of the faulted circuit. In practise, the exact settings may well be determined on site, where system faults can be applied and suitable settings can be adopted based on practically obtained results.

In most situations, the system will not be fully compensated and consequently a small level of steady state fault current will be allowed to flow. The residual current seen by the protection on the faulted feeder may therefore be a larger value, which further emphasises the fact that the protection settings should be based upon practical current levels, wherever possible.

The above also holds true for the RCA setting. As has been shown, a nominal RCA setting of 0° is required. However, fine-tuning of this setting on-site may be necessary in order to obtain the optimum setting in accordance with the levels of coil and feeder resistances present. The loading and performance of the CT will also have an effect in this regard. The effect of CT magnetising current will be to create phase lead of current. Whilst this would assist with operation of faulted feeder IEDs, it would reduce the stability margin of healthy feeder IEDs. A compromise can therefore be reached through fine adjustment of the RCA. This is adjustable in 1° steps.

11 SENSITIVE EARTH FAULT PROTECTION

With some earth faults, the fault current flowing to earth is limited by either intentional resistance (as is the case with some HV systems) or unintentional resistance (e.g. in very dry conditions and where the substrate is high resistance, such as sand or rock).

To provide protection in such cases, it is necessary to provide an earth fault protection system with a setting that is considerably lower than for normal line protection. Such sensitivity cannot be provided with conventional CTs, therefore the SEF input would normally be fed from a core balance current transformer (CBCT) mounted around the three phases of the feeder cable. The SEF transformer should be a special measurement class transformer.

11.1 SEF PROTECTION IMPLEMENTATION

The product provides four stages of SEF protection with independent time delay characteristics.

Stages 1, 2 provide a choice of operate and reset characteristics, where you can select between:

- A range of IDMT (Inverse Definite Minimum Time) curves
- A range of User-defined curves
- DT (Definite Time)

This is achieved using the cells

- ISEF>(n) Function for the overcurrent operate characteristic
- ISEF>(n) Reset Char for the overcurrent reset characteristic
- ISEF>(n) Usr RstChar for the reset characteristic for user -defined curves

where (n) is the number of the stage.

Stages 1 and 2 also provide a Timer Hold facility. This is configured using the cells *ISEF>(n)* tReset.

Stages 3 and 4 have definite time characteristics only.

11.2 NON-DIRECTIONAL SEF LOGIC

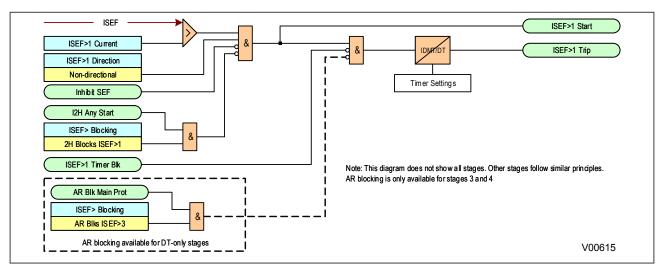


Figure 59: Non-directional SEF logic

The SEF current is compared with a set threshold (*ISEF>(n) Current*) for each stage. If it exceeds this threshold, a Start signal is triggered, providing it is not blocked. This can be blocked by the second harmonic blocking function, or an Inhibit SEF DDB signal.

The autoreclose logic can be set to block the SEF trip after a prescribed number of shots (set in AUTORECLOSE column). This is achieved using the **AR Blk Main Prot** setting. This can also be blocked by the relevant timer block signal **ISEF>(n)TimerBlk** DDB signal.

SEF protection can follow the same IDMT characteristics as described in the Overcurrent Protection Principles section. Please refer to this section for details of IDMT characteristics.

11.3 SEF ANY START LOGIC

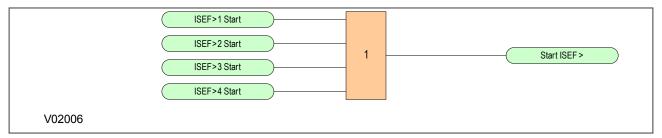


Figure 60: SEF Any Start Logic

11.4 EPATR B CURVE

The EPATR B curve is commonly used for time-delayed Sensitive Earth Fault protection in certain markets. This curve is only available in the Sensitive Earth Fault protection stages 1 and 2. It is based on primary current settings, employing a SEF CT ratio of 100:1 A.

The EPATR_B curve has 3 separate segments defined in terms of the primary current. It is defined as follows:

Segment	Primary Current Range Based on 100A:1A CT Ratio	Current/Time Characteristic
1	ISEF = 0.5A to 6.0A	t = 432 x TMS/ISEF 0.655 secs
2	ISEF = 6.0A to 200A	t = 800 x TMS/ISEF secs
3	ISEF above 200A	t = 4 x TMS secs

where TMS (time multiplier setting) is 0.025 - 1.2 in steps of 0.025.

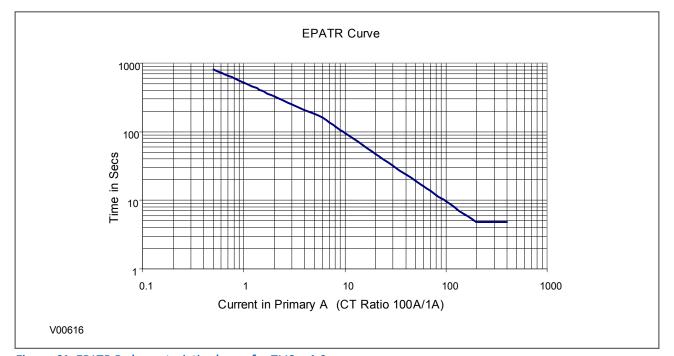


Figure 61: EPATR B characteristic shown for TMS = 1.0

11.5 DIRECTIONAL ELEMENT

Where current may flow in either direction, directional control should be used.

A directional element is available for all of the SEF overcurrent stages. This is found in the *ISEF>(n) Direction* cell for the relevant stage. It can be set to non-directional, directional forward, or directional reverse.

Directionality is achieved by using different techniques depending on the application. With reference to the figure below, you can see that directional SEF can be used for:

- Solidly earthed systems
- Unearthed systems (insulated systems)
- Compensated systems
- Resistance earthed systems

The following diagram shows which type of directional control can be used for which systems.

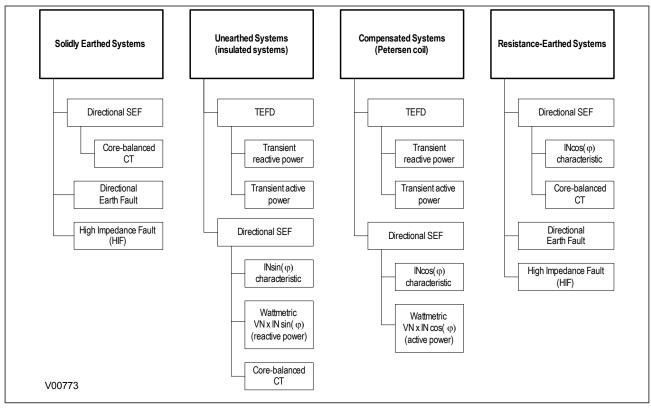


Figure 62: Types of directional control

The device supports standard core-balanced directional control as well as $Isin(\phi)$, $Icos(\phi)$ and Wattmetric characteristics.

If you are using directional SEF protection, you select the required polarisation using the **SEF/REF Options** setting in the SEF/REF PROT'N column.

11.5.1 WATTMETRIC CHARACTERISTIC

Analysis has shown that a small angular difference exists between the spill current on healthy and faulted feeders for earth faults on compensated networks. This angular difference gives rise to active components of current which are in anti-phase to one another.

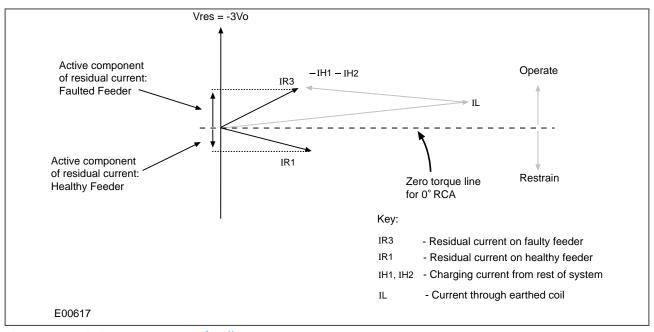


Figure 63: Resistive components of spill current

Consequently, the active components of zero sequence power will also lie in similar planes, meaning an IED capable of detecting active power can make discriminatory decisions. If the Wattmetric component of zero sequence power is detected in the forward direction, then this would indicate fault on that feeder. If power is detected in the reverse direction, then the fault must be present on an adjacent feeder or at the source.

For operation of the directional earth fault element, all three of the settable thresholds must be exceeded; namely the current ISEF>, the voltage *ISEF>VNpol Set* and the power *PN> Setting*.

The power setting is called PN> and is calculated using residual quantities. The formula for operation is as follows:

The PN> setting corresponds to:

$$V_{res}I_{res}\cos(\phi - \phi_c) = 9V_0I_0\cos(\phi - \phi_c)$$

where:

- ϕ = Angle between the Polarising Voltage (**-Vres**) and the Residual Current
- ϕ_C = Relay Characteristic Angle (RCA) Setting (*ISEF* > *Char Angle*)
- V_{res} = Residual Voltage
- I_{res} = Residual Current
- V_o = Zero Sequence Voltage
- I_o = Zero Sequence Current

The action of setting the PN> threshold to zero would effectively disable the wattmetric function and the device would operate as a basic, sensitive directional earth fault element. However, if this is required, then the SEF option can be selected from the **SEF/REF Options** cell in the menu.

Note:

The residual power setting, PN>, is scaled by the programmed Transformer ratios.

A further point to note is that when a power threshold other than zero is selected, a slight alteration is made to the angular boundaries of the directional characteristic. Rather than being $\pm 90^{\circ}$ from the RCA, they are made slightly narrower at $\pm 85^{\circ}$.

The directional check criteria is as follows:

Directional forward: -85° < (angle(IN) - angle(VN + 180°) - RCA) < 85°

Directional reverse: -85° > (angle(IN) - angle(VN + 180°) - RCA) > 85°

11.5.2 ICOS PHI / ISIN PHI CHARACTERISTIC

In some applications, the residual current on the healthy feeder can lie just inside the operating boundary following a fault condition. The residual current for the faulted feeder lies close to the operating boundary.

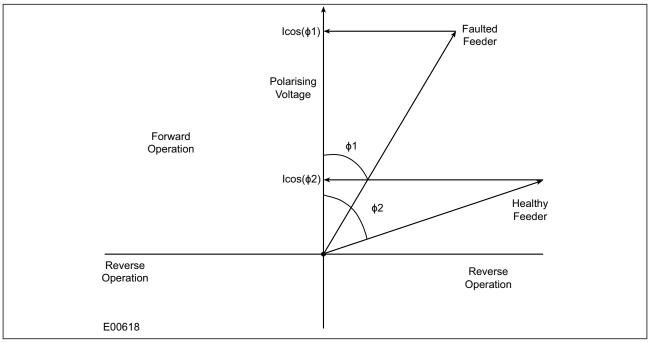


Figure 64: Operating characteristic for Icos

The diagram illustrates the method of discrimination when the real ($\cos\phi$) component is considered. Faults close to the polarising voltage will have a higher magnitude than those close to the operating boundary. In the diagram, we assume that the current magnitude I is in both the faulted and non-faulted feeders.

- For the active component Icos, the criterion for operation is: $I\cos\phi > ISEF > (n)$ current
- For the reactive component Isin, the criterion for operation is: $lsin\phi > ISEF > (n)$ current

Where *ISEF>(n)* current is the sensitive earth fault current setting for the stage in question

If any stage is set to non-directional, the element reverts back to normal operation based on current magnitude I with no directional decision. In this case, correct discrimination is achieved by means of an Icos characteristic as the faulted feeder will have a large active component of residual current, whilst the healthy feeder will have a small value.

For insulated earth applications, it is common to use the Isin characteristic.

All of the relevant settings can be found under the SEF PROTECTION column.

11.5.3 DIRECTIONAL SEF LOGIC

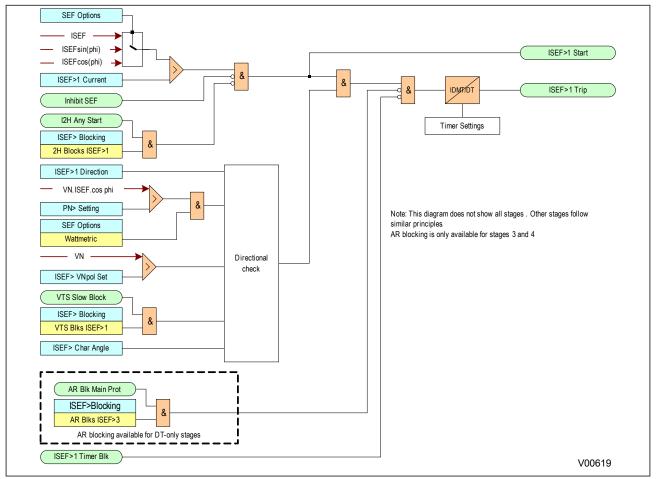


Figure 65: Directional SEF with VN polarisation (single stage)

The sensitive earth fault protection can be set IN/OUT of service using the appropriate DDB inhibit signal, which can be operated from an opto-input or control command. VT Supervision (VTS) selectively blocks the directional protection or causes it to revert to non-directional operation. When selected to block the directional protection, VTS blocking is applied to the directional checking which effectively blocks the start outputs as well.

The directional check criteria are given below for the standard directional sensitive earth fault element:

- Directional forward: -90° < (angle(IN) angle(VN + 180°) RCA) < 90°
- Directional reverse: -90° > (angle(IN) angle(VN + 180°) RCA) > 90°

Three possibilities exist for the type of protection element that you can use for sensitive earth fault detection:

- A suitably sensitive directional earth fault protection element having a characteristic angle setting (RCA) of zero degrees, with the possibility of fine adjustment about this threshold.
- A sensitive directional zero sequence wattmetric protection element having a characteristic angle setting (RCA) of zero degrees, with the possibility of fine adjustment about this threshold.
- A sensitive directional earth fault protection element having $lcos\phi$ and $lsin\phi$ characteristics.

All stages of the sensitive earth fault element can be set down to 0.5% of rated current.

11.6 APPLICATION NOTES

11.6.1 INSULATED SYSTEMS

When insulated systems are used, it is not possible to detect faults using standard earth fault protection. It is possible to use a residual overvoltage device to achieve this, but even with this method full discrimination is not possible. Fully discriminative earth fault protection on this type of system can only be achieved by using a SEF (Sensitive Earth Fault) element. This type of protection detects the resultant imbalance in the system charging currents that occurs under earth fault conditions. A core balanced CT must be used for this application. This eliminates the possibility of spill current that may arise from slight mismatches between residually connected line CTs. It also enables a much lower CT ratio to be applied, thereby allowing the required protection sensitivity to be more easily achieved.

The following diagram shows an insulated system with a C-phase fault.

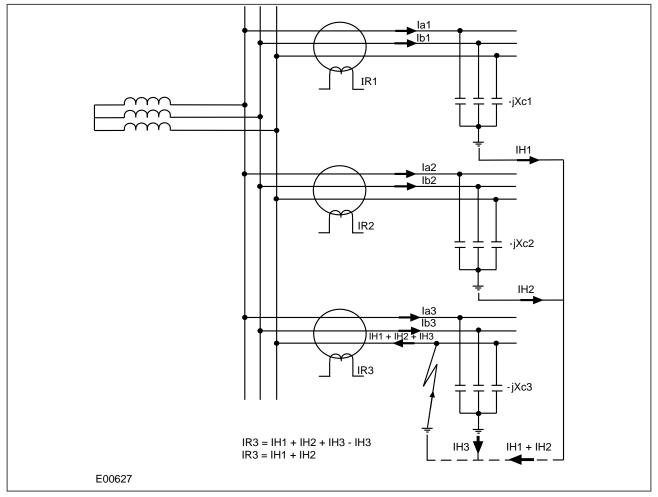


Figure 66: Current distribution in an insulated system with C phase fault

The protection elements on the healthy feeder see the charging current imbalance for their own feeder. The protection element on the faulted feeder, however, sees the charging current from the rest of the system (IH1 and IH2 in this case). Its own feeder's charging current (IH3) is cancelled out.

With reference to the associated vector diagram, it can be seen that the C-phase to earth fault causes the voltages on the healthy phases to rise by a factor of $\sqrt{3}$. The A-phase charging current (Ia1), leads the resultant A phase voltage by 90°. Likewise, the B-phase charging current leads the resultant Vb by 90°.

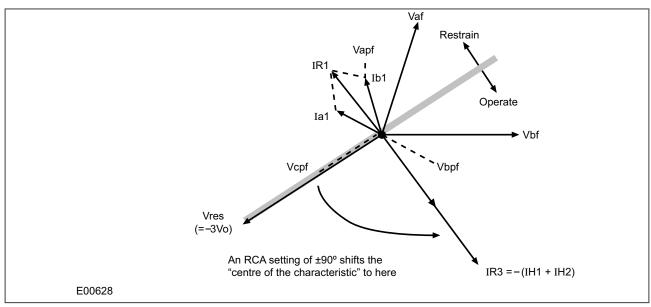


Figure 67: Phasor diagrams for insulated system with C phase fault

The current imbalance detected by a core balanced current transformer on the healthy feeders is the vector addition of Ia1 and Ib1. This gives a residual current which lags the polariing voltage (–3Vo) by 90°. As the healthy phase voltages have risen by a factor of $\sqrt{3}$, the charging currents on these phases are also $\sqrt{3}$ times larger than their steady state values. Therefore, the magnitude of the residual current IR1, is equal to 3 times the steady state per phase charging current.

The phasor diagram indicates that the residual currents on the healthy and faulted feeders (IR1 and IR3 respectively) are in anti-phase. A directional element (if available) could therefore be used to provide discriminative earth fault protection.

If the polarising is shifted through $+90^{\circ}$, the residual current seen by the relay on the faulted feeder will lie within the operate region of the directional characteristic and the current on the healthy feeders will fall within the restrain region.

The required characteristic angle setting for the SEF element when applied to insulated systems, is $+90^{\circ}$. This is for the case when the protection is connected such that its direction of current flow for operation is from the source busbar towards the feeder. If the forward direction for operation were set such that it is from the feeder into the busbar, then a -90° RCA would be required.

Note

Discrimination can be provided without the need for directional control. This can only be achieved, however, if it is possible to set the IED in excess of the charging current of the protected feeder and below the charging current for the rest of the system.

11.6.2 SETTING GUIDELINES (INSULATED SYSTEMS)

The residual current on the faulted feeder is equal to the sum of the charging currents flowing from the rest of the system. Further, the addition of the two healthy phase charging currents on each feeder gives a total charging current which has a magnitude of three times the per phase value. Therefore, the total imbalance current is equal to three times the per phase charging current of the system. A typical setting may therefore be in the order of 30% of this value, i.e. equal to the per phase charging current of the remaining system. Practically though, the required setting may well be determined on site, where suitable settings can be adopted based on practically obtained results.

When using a core-balanced transformer, care must be taken in the positioning of the CT with respect to the earthing of the cable sheath:

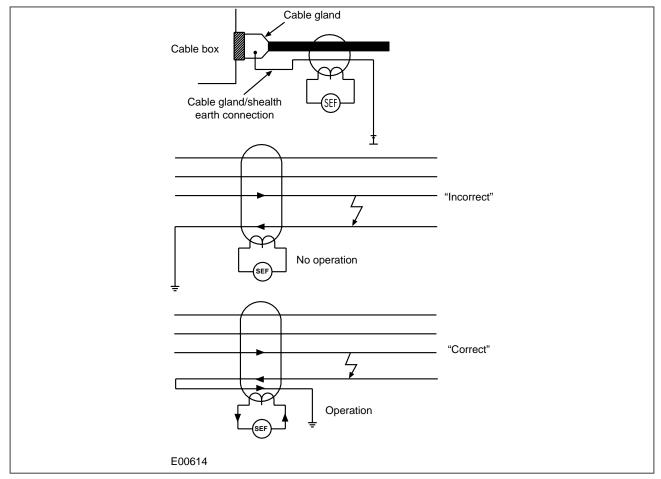


Figure 68: Positioning of core balance current transformers

If the cable sheath is terminated at the cable gland and directly earthed at that point, a cable fault (from phase to sheath) will not result in any unbalanced current in the core balance CT. Therefore, prior to earthing, the connection must be brought back through the CBCT and earthed on the feeder side. This then ensures correct relay operation during earth fault conditions.

12 THERMAL OVERLOAD PROTECTION

The heat generated within an item of plant is the resistive loss. The thermal time characteristic is therefore based on the equation I²Rt. Over-temperature conditions occur when currents in excess of their maximum rating are allowed to flow for a period of time.

Temperature changes during heating follow exponential time constants. The device provides two characteristics for thermal overload protection; a single time constant characteristic and a dual time constant characteristic. You select these according to the application.

12.1 SINGLE TIME CONSTANT CHARACTERISTIC

This characteristic is used to protect cables, dry type transformers and capacitor banks.

The single constant thermal characteristic is given by the equation:

$$t = -\tau \log \left[\frac{I^2 - (KI_{FLC})^2}{I^2 - I_p^2} \right]$$

where:

- t = time to trip, following application of the overload current I
- τ = heating and cooling time constant of the protected plant
- I = largest phase current
- I_{FLC} full load current rating (the Thermal Trip setting)
- K = a constant with the value of 1.05
- I_D = steady state pre-loading before application of the overload

12.2 DUAL TIME CONSTANT CHARACTERISTIC

This characteristic is used to protect equipment such as oil-filled transformers with natural air cooling. The thermal model is similar to that with the single time constant, except that two timer constants must be set.

For marginal overloading, heat will flow from the windings into the bulk of the insulating oil. Therefore, at low current, the replica curve is dominated by the long time constant for the oil. This provides protection against a general rise in oil temperature.

For severe overloading, heat accumulates in the transformer windings, with little opportunity for dissipation into the surrounding insulating oil. Therefore at high current levels, the replica curve is dominated by the short time constant for the windings. This provides protection against hot spots developing within the transformer windings.

Overall, the dual time constant characteristic serves to protect the winding insulation from ageing and to minimise gas production by overheated oil. Note however that the thermal model does not compensate for the effects of ambient temperature change.

The dual time constant thermal characteristic is given by the equation:

$$0.4e^{(-t/\tau_1)} + 0.6e^{(-t/\tau_2)} = \left[\frac{I^2 - (KI_{FLC})^2}{I^2 - I_p^2}\right]$$

where:

- τ_1 = heating and cooling time constant of the transformer windings
- τ_2 = heating and cooling time constant of the insulating oil

12.3 THERMAL OVERLOAD PROTECTION IMPLEMENTATION

The device incorporates a current-based thermal characteristic, using RMS load current to model heating and cooling of the protected plant. The element can be set with both alarm and trip stages.

Thermal Overload Protection is implemented in the THERMAL OVERLOAD column of the relevant settings group.

This column contains the settings for the characteristic type, the alarm and trip thresholds and the time constants.

12.4 THERMAL OVERLOAD PROTECTION LOGIC

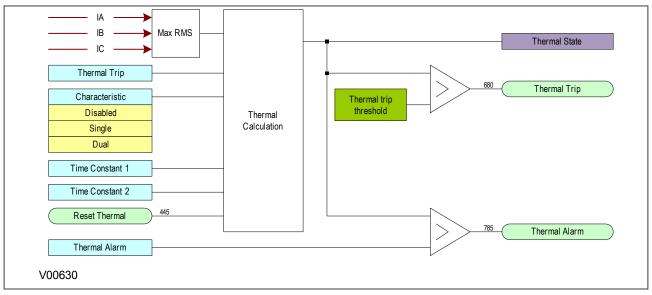


Figure 69: Thermal overload protection logic diagram

The magnitudes of the three phase input currents are compared and the largest magnitude is taken as the input to the thermal overload function. If this current exceeds the thermal trip threshold setting a start condition is asserted.

The Start signal is applied to the chosen thermal characteristic module, which has three outputs signals; alarm trip and thermal state measurement. The thermal state measurement is made available in one of the MEASUREMENTS columns.

The thermal state can be reset by either an opto-input (if assigned to this function using the programmable scheme logic) or the HMI panel menu.

12.5 APPLICATION NOTES

12.5.1 SETTING GUIDELINES FOR DUAL TIME CONSTANT CHARACTERISTIC

The easiest way of solving the dual time constant thermal equation is to express the current in terms of time and to use a spreadsheet to calculate the current for a series of increasing operating times using the following equation, then plotting a graph.

$$I = \sqrt{\frac{0.4I_p^2.e^{(-t/\tau 1)} + 0.6I_p^2.e^{(-t/\tau 2)} - k^2.I_{FLC}^2}{0.4e^{(-t/\tau 1)} + 0.6e^{(-t/\tau 2)} - 1}}$$

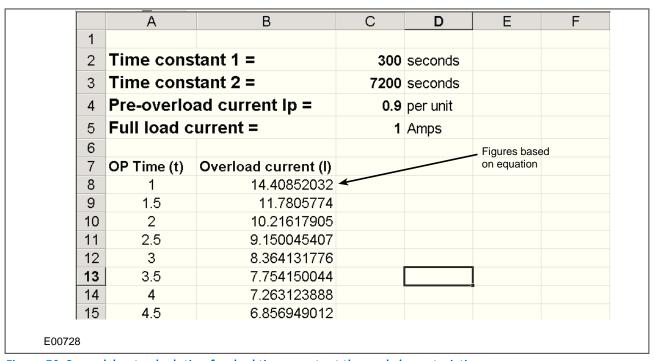


Figure 70: Spreadsheet calculation for dual time constant thermal characteristic

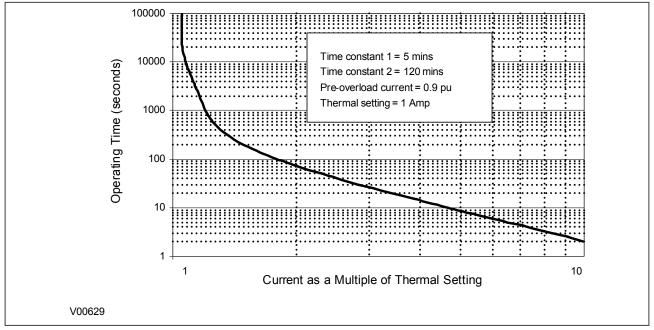


Figure 71: Dual time constant thermal characteristic

The current setting is calculated as:

Thermal Trip = Permissible continuous loading of the transformer item/CT ratio.

For an oil-filled transformer with rating 400 to 1600 kVA, the approximate time constants are:

- $\tau_1 = 5$ minutes
- $\tau_2 = 120$ minutes

An alarm can be raised on reaching a thermal state corresponding to a percentage of the trip threshold. A typical setting might be "Thermal Alarm" = 70% of thermal capacity.

Note:

The thermal time constants given in the above tables are typical only. Reference should always be made to the plant manufacturer for accurate information.

12.5.2 SETTING GUIDELINES FOR SINGLE TIME CONSTANT CHARACTERISTIC

The time to trip varies depending on the load current carried before application of the overload, i.e. whether the overload was applied from hot or cold.

The thermal time constant characteristic may be rewritten as:

$$e^{(-t/\tau)} = \left[\frac{\theta - \theta_p}{\theta - 1}\right]$$

where:

- $\theta = \text{thermal state} = I^2/K^2I_{FLC}^2$
- θ_p = pre-fault thermal state = $I_p^2/K^2I_{FLC}^2$
- I_p is the pre-fault thermal state
- IFLC is the full load current

Note:

A current of 105%ls (KI_{FLC}) has to be applied for several time constants to cause a thermal state measurement of 100%.

The current setting is calculated as:

Thermal Trip = Permissible continuous loading of the plant item/CT ratio.

The following tables show the approximate time constant in minutes, for different cable rated voltages with various conductor cross-sectional areas, and other plant equipment.

Area mm ²	6 - 11 kV	22 kV	33 kV	66 kV
25 – 50	10 minutes	15 minutes	40 minutes	-
70 – 120	15 minutes	25 minutes	40 minutes	60 minutes
150	25 minutes	40 minutes	40 minutes	60 minutes
185	25 minutes	40 minutes	60 minutes	60 minutes
240	40 minutes	40 minutes	60 minutes	60 minutes
300	40 minutes	60 minutes	60 minutes	90 minutes

Plant type	Time Constant (Minutes)
Dry-type transformer <400 kVA	40
Dry-type transformers 400 – 800 kVA	60 - 90
Air-core Reactors	40
Capacitor Banks	10
Overhead Lines with cross section > 100 mm ²	10
Overhead Lines	10
Busbars	60

13 BROKEN CONDUCTOR PROTECTION

One type of unbalanced fault is the 'Series' or 'Open Circuit' fault. This type of fault can arise from, among other things, broken conductors. Series faults do not cause an increase in phase current and so cannot be detected by overcurrent protection. However, they do produce an imbalance, resulting in negative phase sequence current, which can be detected.

It is possible to apply a negative phase sequence overcurrent element to detect broken conductors. However, on a lightly loaded line, the negative sequence current resulting from a series fault condition may be very close to, or less than, the full load steady state imbalance arising from CT errors and load imbalances, making it very difficult to distinguish. A regular negative sequence element would therefore not work at low load levels. To overcome this, the device incorporates a special Broken Conductor protection element.

The Broken Conductor element measures the ratio of negative to positive phase sequence current (I2/I1). This ratio is approximately constant with variations in load current, therefore making it more sensitive to series faults than standard negative sequence protection.

13.1 BROKEN CONDUCTOR PROTECTION IMPLEMENTATION

Broken Conductor protection is implemented in the *BROKEN CONDUCTOR* column of the relevant settings group. This column contains the settings to enable the function, for the pickup threshold and the time delay.

13.2 BROKEN CONDUCTOR PROTECTION LOGIC

The ratio of I_2/I_1 is calculated and compared with the threshold setting. If the threshold is exceeded, the delay timer is initiated. The CTS block signal is used to block the operation of the delay timer.

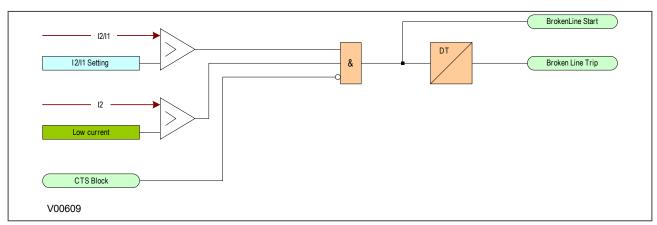


Figure 72: Broken conductor logic

13.3 APPLICATION NOTES

13.3.1 SETTING GUIDELINES

For a broken conductor affecting a single point earthed power system, there will be little zero sequence current flow and the ratio of I_2/I_1 that flows in the protected circuit will approach 100%. In the case of a multiple earthed power system (assuming equal impedance's in each sequence network), the ratio I_2/I_1 will be 50%.

In practise, the levels of standing negative phase sequence current present on the system govern this minimum setting. This can be determined from a system study, or by making use of the measurement facilities at the commissioning stage. If the latter method is adopted, it is important to take the measurements during maximum system load conditions, to ensure that all single-phase loads are accounted for.

Note:

A minimum value of 8% negative phase sequence current is required for successful operation.

Since sensitive settings have been employed, we can expect that the element will operate for any unbalanced condition occurring on the system (for example, during a single pole autoreclose cycle). For this reason, a long time delay is necessary to ensure co-ordination with other protection devices. A 60 second time delay setting may be typical.

The following example was recorded by an IED during commissioning:

$$I_{\text{full load}} = 500A$$

$$I_2 = 50A$$

therefore the quiescent I_2/I_1 ratio = 0.1

To allow for tolerances and load variations a setting of 20% of this value may be typical: Therefore set:

$$I_2/I_1 = 0.2$$

In a double circuit (parallel line) application, using a 40% setting will ensure that the broken conductor protection will operate only for the circuit that is affected. A setting of 0.4 results in no pick-up for the parallel healthy circuit.

Set I_2/I_1 Time Delay = 60 s to allow adequate time for short circuit fault clearance by time delayed protections.

14 BLOCKED OVERCURRENT PROTECTION

With Blocked Overcurrent schemes, you connect the start contacts from downstream IEDs to the timer blocking inputs of upstream IEDs. This allows identical current and time settings to be used on each of the IEDs in the scheme, as the device nearest to the fault does not receive a blocking signal and so trips discriminatively. This type of scheme therefore reduces the number of required grading stages, and consequently fault clearance times.

The principle of Blocked Overcurrent protection may be extended by setting fast-acting overcurrent elements on the incoming feeders to a substation, which are then arranged to be blocked by start contacts from the devices protecting the outgoing feeders. The fast-acting element is thus allowed to trip for a fault condition on the busbar, but is stable for external feeder faults due to the blocking signal.

This type of scheme provides much reduced fault clearance times for busbar faults than would be the case with conventional time-graded overcurrent protection. The availability of multiple overcurrent and earth fault stages in the General Electric IEDs allows additional time-graded overcurrent protection for back-up purposes.

14.1 BLOCKED OVERCURRENT IMPLEMENTATION

Blocked Overcurrent schemes are implemented using the PSL. The start outputs, available from each stage of the overcurrent and earth fault elements (including the sensitive earth fault element) can be mapped to output relay contacts. These outputs can then be connected to the relevant timer block inputs of the upstream IEDs via optoinputs.

14.2 BLOCKED OVERCURRENT LOGIC

To facilitate the implementation of blocked overcurrent schemes, the device provides the following logic to provide a Blocked Overcurrent Start signal *I> BlockStart*:

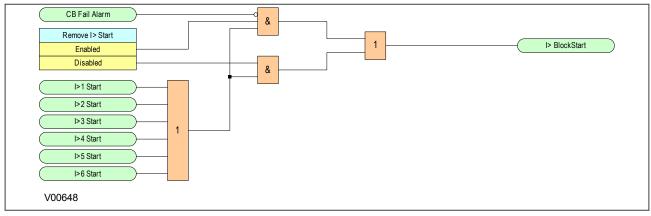


Figure 73: Blocked Overcurrent logic

The *I*> *BlockStart* signal is derived from the logical OR of the phase overcurrent start outputs. This output is then gated with the *CB Fail Alarm* DDB signal and the setting *Remove I*> *Start* setting.

14.3 BLOCKED EARTH FAULT LOGIC

To facilitate the implementation of blocked overcurrent schemes, the device provides the following logic to provide the Blocked Earth Fault signal *IN/SEF>Blk Start*:

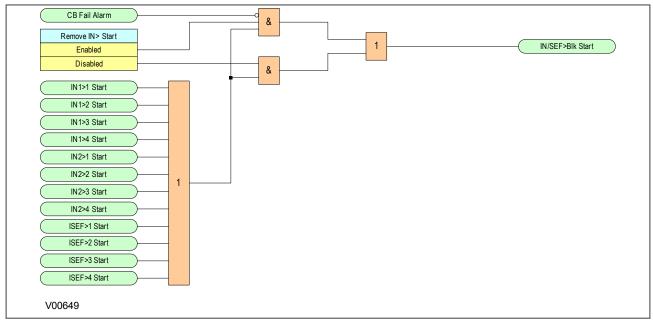


Figure 74: Blocked Earth Fault logic

The *IN/SEF>Blk Start* signal is derived from the logical OR of the phase overcurrent start outputs. This output is then gated with the *CB Fail Alarm* DDB signal and the *Remove IN> Start* setting.

14.4 APPLICATION NOTES

14.4.1 BUSBAR BLOCKING SCHEME

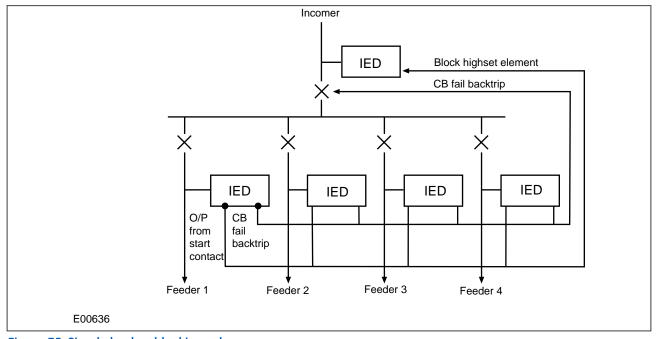


Figure 75: Simple busbar blocking scheme

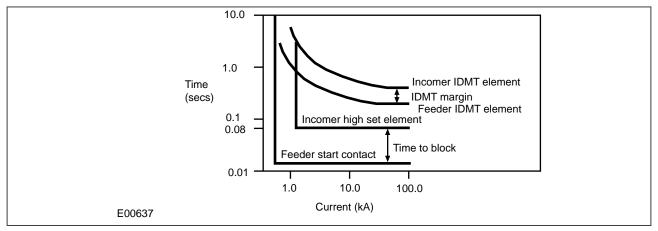


Figure 76: Simple busbar blocking scheme characteristics

For further guidance on the use of blocked busbar schemes, refer to General Electric.

15 SECOND HARMONIC BLOCKING

When a transformer is initially connected to a source of AC voltage, there may be a substantial surge of current through the primary winding called inrush current.

Inrush current is a regularly occurring phenomenon and should not be considered a fault, as we do not wish the protection device to issue a trip command whenever a transformer, or machine is switched on. This presents a problem to the protection device, because it should always trip on an internal fault. The problem is that typical internal transformer faults may produce overcurrents which are not necessarily greater than the inrush current. Furthermore faults tend to manifest themselves on switch on, due to the high inrush currents. For this reason, we need to find a mechanism that can distinguish between fault current and inrush current. Fortunately this is possible due to the different natures of the respective currents. An inrush current waveform is rich in harmonics (particularly the second), whereas an internal fault current consists only of the fundamental. We can thus develop a restraining method based on the harmonic content of the inrush current. The mechanism by which this is achieved is called second harmonic blocking.

15.1 SECOND HARMONIC BLOCKING IMPLEMENTATION

Second harmonic blocking can be applied to the following overcurrent protection types:

- Phase Overcurrent protection (POC)
- Earth Fault protection (derived and measured) (EF1 and EF2)
- Sensitive Earth Fault protection (SEF)
- Negative Phase Sequence Overcurrent protection (NPSOC)

Second harmonic blocking is implemented in the SECURITY CONFIG column of the relevant setting group.

Second harmonic blocking is applicable to all stages of each of the elements. Each protection element has a relevant blocking setting with which the type of blocking is defined.

For phase overcurrent, 2nd harmonic blocking can be applied to each phase individually (phase segregated), or to all three phases at once (cross-block). This is determined by the *I*> *Blocking* setting.

& IA fundamental I2H Any Start I>Lift 2H IA2H Start Low current (hard-coded) IB2H Start IA 2nd harm / IA fund IA 2ndHarm IC2H Start 2ndHarm Thresh IA fundamental I>Lift 2H Low current (hard-coded) IB 2nd harm / IB fund IB 2ndHarm 2ndHarm Thresh IC 2ndHarm I>Lift 2H Low current (hard-coded) IC 2nd harm / IC fund IC 2ndHarm 2ndHarm Thresh V00626

15.2 SECOND HARMONIC BLOCKING LOGIC (POC INPUT)

Figure 77: 2nd Harmonic Blocking Logic (POC Input)

The function works by identifying and measuring the inrush currents present in the phase currents at switch on. It does this by comparing the value of the second harmonic current components to the value of the fundamental component. If this ratio exceeds the set thresholds, then the blocking signal is generated. The threshold is defined by the *2ndHarm Thresh* setting.

We only want the function to block the protection if the fundamental current component is within the normal range. If this exceeds the normal range, then this is indicative of a fault, which must be protected. For this reason there is another settable trigger *I>lift 2H*, which when exceeded, stops the 2nd harmonic blocking function.

15.3 SECOND HARMONIC BLOCKING LOGIC (SEF INPUT)

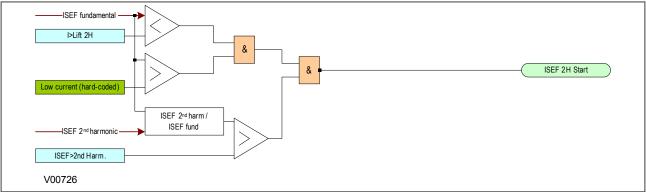


Figure 78: 2nd Harmonic Blocking Logic (SEF Input)

The function measures the current present at the SEF CT input and determines the ratio of the second harmonic component to the fundamental. If this ratio exceeds the set threshold, then the SEF second harmonic blocking signal is generated. The threshold is defined by the *ISEF>2nd Harm*. setting.

We only want the function to block the protection if the fundamental current component is within the normal range. If this exceeds the normal range, then this is indicative of a fault, which must be protected. For this reason there is another settable trigger *I*> *lift 2H*, which when exceeded, stops the 2nd harmonic blocking function.

The minimum detection level is 4 mA rms. The maximum detection level is 1.8 A rms in any sample over the previous cycle. There is no delay on pick-up but there is a 1 cycle delay on drop-off.

15.4 APPLICATION NOTES

15.4.1 SETTING GUIDELINES

During the energization period, the second harmonic component of the inrush current may be as high as 70%. The second harmonic level may be different for each phase, which is why phase segregated blocking is available.

If the setting is too low, the 2nd harmonic blocking may prevent tripping during some internal transformer faults. If the setting is too high, the blocking may not operate for low levels of inrush current which could result in undesired tripping of the overcurrent element during the energization period. In general, a setting of 15% to 20% is suitable.

16 LOAD BLINDERS

Load blinding is a mechanism, where protection elements are prevented from tripping under heavy load, but healthy conditions. In the past this mechanism was mainly used for transmission systems and was rarely needed at distribution voltage levels. In the last few years, however, distribution networks have become more subject to periods of sustained heavy loads. This is due to a number of reasons, one of which is the increase of distributed generation. For this reason, it has become very desirable to equip overcurrent protection, normally targeted at distribution networks, with load blinding functionality.

Load blinders work by measuring, not only the system current levels, but also the system voltage levels and making tripping decisions based on analysis of both of these measurements. This is known as Impedance measurement.

When the measured current is higher than normal, this can be caused by one of two things; either a fault or a heavy load. If the cause is a fault, the system voltage level will reduce significantly. However, if the cause is a heavy, but healthy load, the voltage will not decrease significantly. Therefore, by measuring the both the system voltage and currents, the protection can make a decision not to trip under heavy load conditions.

The principle of a load blinder is to configure a blinder envelope, which surrounds the expected worst case load limits, and to block tripping for any impedance measured within this blinder region. Only fault impedance outside the load area is allowed to cause a trip. It is possible to set the impedance and angle setting independently for the forward and reverse regions in the Z plane.

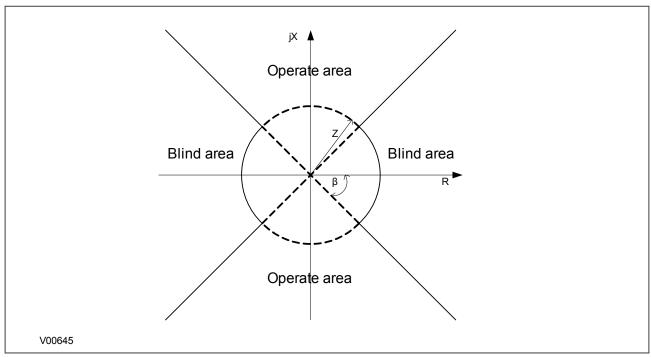


Figure 79: Load blinder and angle

16.1 LOAD BLINDER IMPLEMENTATION

The Load blinder function is implemented in the *OVERCURRENT* column of the relevant settings group, under the sub-heading *LOAD BLINDER*.

The settings allow you to set the impedance and angle limits for both reverse and forward directions, the undervoltage and negative sequence current thresholds for blocking the function, and the operation mode.

There are two modes of operation; single phase and three phase;

The single phase mode uses the normal impedance (Z) of each phase. When single phase mode is selected, the overcurrent blocking is phase segregated and is dependant on the individual overcurrent settings per phase. In single phase mode, only the undervoltage threshold (*Blinder V < Block*) can block the function.

The three phase mode uses positive sequence impedance (Z1). The three phase mode uses both the negative sequence overcurrent threshold (**Blinder I2>Block**) and the undervoltage threshold (**Blinder V< Block**) to block the function.

16.2 LOAD BLINDER LOGIC

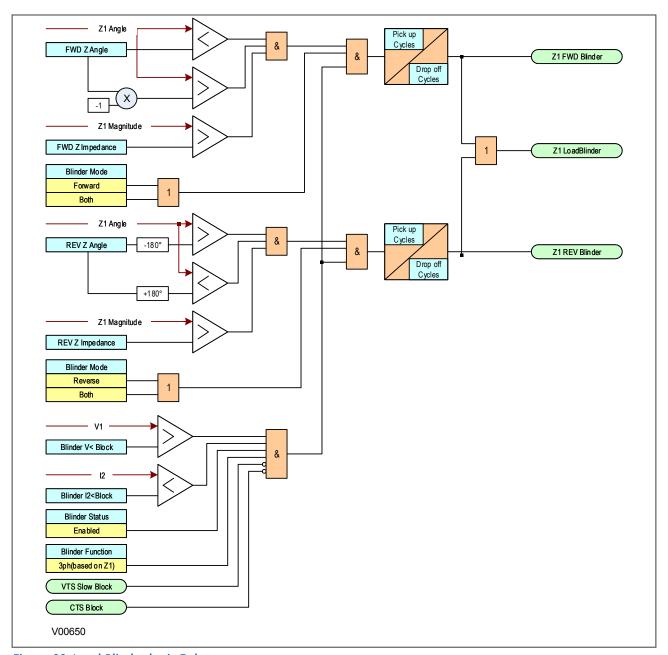


Figure 80: Load Blinder logic 3phase

For the forward direction, the positive sequence impedance magnitude is compared with a set value, and the positive sequence impedance angle is compared with two values, which define the angular range. If the criteria are satisfied and the Blinder mode is in the direction Forward or Both, the blinder signals **Z1 FWD Blinder** and **Z1 LoadBlinder** are produced.

For the reverse direction, the positive sequence impedance magnitude is compared with a set value, and the positive sequence impedance angle is compared with two values, which define the angular range. If the criteria are satisfied and the Blinder mode is in the direction Forward or Both, the blinder signals **Z1 REV Blinder** and **Z1 LoadBlinder** are produced.

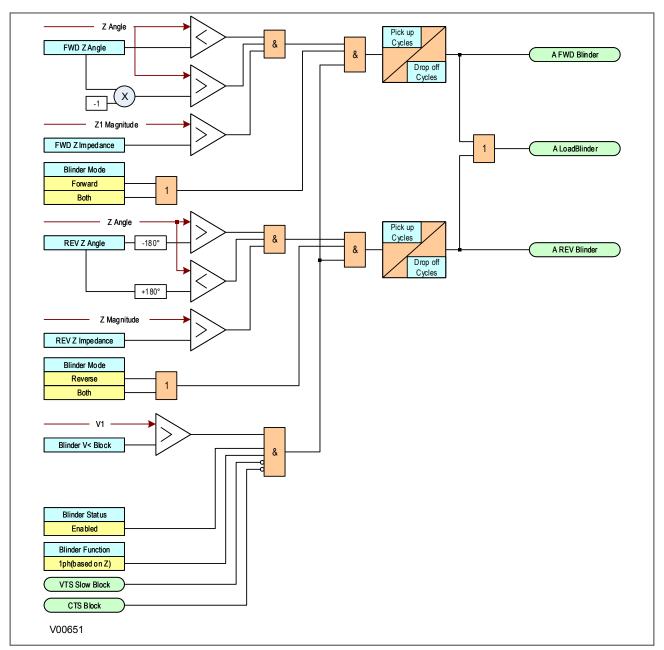


Figure 81: Load Blinder logic phase A

The diagram shows the single-phase Load Blinder logic for phase A. The same principle applies to phases B and C. The single phase Load Blinder logic is very similar to the three-phase Load Blinder logic. The main differences are:

The single-phase function does not use positive sequence impedance, it uses normal impedance measurment. It also does not use negative sequence overcurrent to block the function.

17 NEUTRAL ADMITTANCE PROTECTION

Neutral admittance protection works by calculating the neutral admittance from the neutral input current and voltage (I_N/V_N). The neutral current input is measured with an earth fault or sensitive earth fault current transformer and the neutral voltage is based on the internally derived quantity VN.

Three single stage elements are provided:

- Overadmittance YN>: This is non-directional, providing both start and time delayed trip outputs. The trip may be blocked by a logic input
- Overconductance GN>: This is non-directional or directional, providing both start and time delayed trip outputs. The trip may be blocked by a logic input
- Oversusceptance BN>: This is is non-directional or directional, providing both start and time delayed trip outputs. The trip may be blocked by a logic input

The overadmittance elements YN>, GN> and BN> will operate providing the neutral voltage remains above the set level for the set operating time of the element. They are blocked by operation of the fast VTS block signal from the VT supervision function.

The overadmittance elements provide measurements of admittance, conductance and susceptance that also appear in the fault record.

The overadmittance elements are capable of initiating auto-reclose by means of YN>, GN> and BN> settings in the AUTO-RECLOSE menu column.

17.1 NEUTRAL ADMITTANCE OPERATION

The admittance protection is non-directional. Hence, provided the magnitude of admittance exceeds the set value **YN>** Set and the magnitude of neutral voltage exceeds the set value VN Threshold, the device will operate.

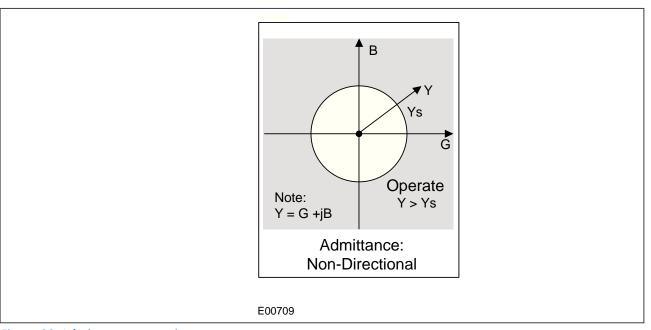


Figure 82: Admittance protection

17.2 CONDUCTANCE OPERATION

The conductance protection may be set non-directional, directional forward or directional reverse. Hence, provided the magnitude and the directional criteria are met for conductance and the magnitude of neutral voltage exceeds the set value VN Threshold, the device will operate. The correction angle causes rotation of the directional boundary for conductance through the set correction angle.

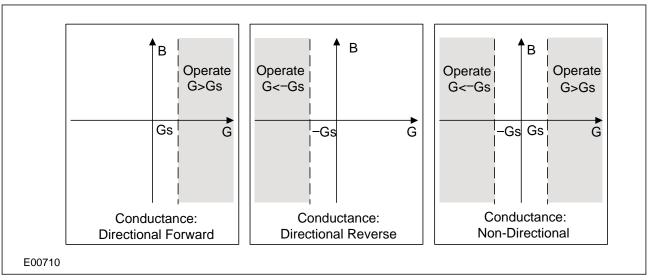


Figure 83: Conductance operation

Note:

For forward operation, the centre of characteristic occurs when IN is in phase with VN.

Note

If the correction angle is set to $+30^\circ$, this rotates the boundary from 90° - 270° to 60° - 240° . It is assumed that the direction of the G axis indicates 0° .

17.3 SUSCEPTANCE OPERATION

The susceptance protection may be set non-directional, directional forward or directional reverse. Hence, provided the magnitude and the directional criteria are met for susceptance and the magnitude of neutral voltage exceeds the set value VN Threshold, the relay will operate. The correction angle causes rotation of the directional boundary for susceptance through the set correction angle.

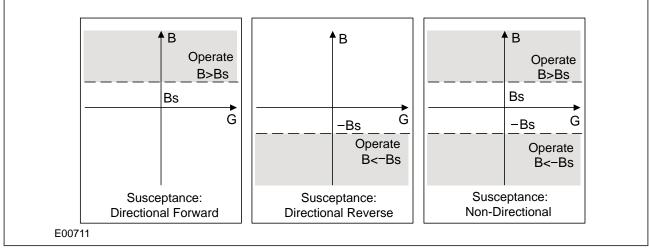


Figure 84: Susceptance operation

Note:

For forward operation, the centre of characteristic occurs when IN leads VN by 90°.

Note:

If the correction angle is set to $+30^\circ$, this rotates the boundary from 0° - 180° to 330° - 150° . It is assumed that the direction of the G axis indicates 0° .

18 BUSBAR PROTECTION

Busbars are the nerve centers of the power system. This is where power lines are connected together in a substation. Essentially a bus bar is a robust and highly conductive metal framework, onto which power lines are connected.

Busbars can pass current from a large number of lines, so a fault on the busbar could result in an extremely large fault current resulting in enormous damage. Faults on busbars are generally rare, but because of the extreme consequence in the event of failure, it is generally wise to provide dedicated protection for them.

Because the connections to busbars are close together, differential protection offers a convenient solution for busbar protection. Using the principle of Kirchoff's law, we need only to compare the sum of the incoming currents with the sum of the outgoing current and establish the difference. If there is a significant difference, then this indicates a fault on the busbar.

The following figure shows a simplified busbar with two input lines and three output lines.

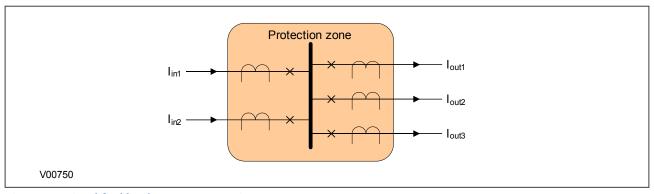


Figure 85: Simplified busbar representation

In this example, if the vector sum of lin1, lin2, lout1, lout2 and lout3 = 0, there is no fault. If the vector sum is not equal to zero, then there is a fault.

There are various protection techniques for busbars, but the technique which is most commonly used is high impedance differential protection. A standard overcurrent protection element can be used for this purpose.

For high impedance differential protection, we need to connect the secondary windings of identical current transformers in parallel, then measure the summed current as follows:

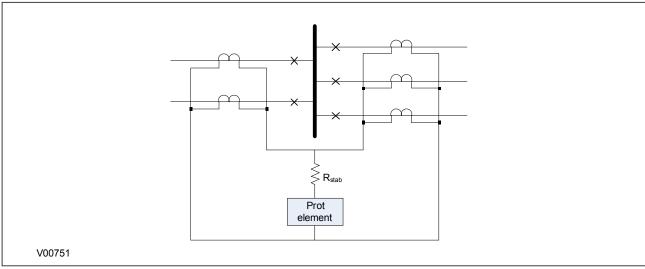


Figure 86: High Impedance differential protection for busbars

The stabilising resistor R_{stab} is the reason why the protection type is high impedance. This resistor reduces the value of the spill current caused by CT discrepancies, thereby reducing the chance of maloperation caused by external faults.

18.1 BUSWIRE SUPERVISION

The P14x range of feeder protection devices can use their overcurrent elements for high impedance busbar protection applications. With any high impedance busbar application, it is essential to provide a special type of CT supervision called Buswire Supervision. This is to prevent overvoltages on the CTs in case of CT open circuits and to prevent overheating of the protection devices.

This buswire supervision can be achieved using a dedicated device called an MVTP relay. But this functionality can now be achieved numerically with any P14x device from software versions 52 and 61 via the Sensitive Overvoltage Protection (SOV)function. The unique characteristic in SOV function extends the relay's capability to mimic the buswire supervision function in a high impedance busbar protection scheme. It is therefore now possible to provide a single box solution for high impedance busbar protection with integrated buswire supervision. Buswire supervision uses the Sensitive Overvoltage Protection function as described in the Voltage Protection section of this manual. The Sensitive Overvoltage protection function allows the possibility of low pickup voltages (down to 2 V) making it ideal for monitoring the voltages apparent on the Busbar protection CTs. The start and trip outputs can be used for creating alarms and for short circuiting the Busbar protection CT secondary windings.

18.2 APPLICATION NOTES

18.2.1 BUSBAR PROTECTION

A typical 132kV double bus generating station is made up of two 100MVA generators and associated step-up transformers, providing power to the high voltage system, by means of four overhead transmission lines, shown below. The main and reserve busbars are sectionalised with bus section circuit breakers. The application for a high impedance circulating current scheme having 4 zones and an overall check feature, is as follows:

The switchgear rating is 3500MVA, the system voltage is 132kV solidly earthed and the maximum loop lead resistance is 2 ohms. The current transformers are of ratio 500/1 amp and have a secondary resistance of 0.7 ohms. The system has an X/R ratio of 20.

18.2.1. STABILITY VOLTAGE

The stability level of the busbar protection is governed by the maximum through fault level which is assumed to be the switchgear rating. Using the switchgear rating allows for any future system expansion.

$$= \frac{3500 \times 10^6}{\sqrt{3} \times 132 \times 10^3} = 15300A$$

Required relay stability voltage (assuming one CT is saturated)

$$= K I_f (R_{CT} + 2_{RL})$$

$$= \frac{1.2 \times 15300}{500} (0.7 + 2)$$

$$= 99V$$

18.2.1. CURRENT SETTING

The primary operating current of busbar protection is normally set to less than 30% of the minimum fault level. It is also considered good practice by some utilities to set the minimum primary operating current in excess of the rated load. Therefore, if one of the CTs becomes open circuit the high impedance relay does not maloperate.

The primary operating current should be made less than 30% of the minimum fault current and more than the full load current of one of the incomers. Therefore, if one of the incomer CTs becomes open circuit the differential

protection will not maloperate. It is assumed that 30% of the minimum fault current is more than the full load current of the largest circuit.

Full load current

$$= \frac{100 \times 10^3}{\sqrt{3} \times 132} = 438A$$

18.2.1. DISCRIMINATING ZONE

Magnetising current taken by each CT at 99V = 0.072A

Maximum number of CTs per zone = 5

Relay current setting, Ir(I>) = 400A = 0.8In

Relay primary operating current,

$$I_{op}$$
 = CT ratio x (I_r + n I_e)
= 500 x (0.8 + (5 x 0.072))
= 500 x 1.16
= 580A (132% full load current)

18.2.1. CHECK ZONE

Magnetising current taken by each CT at 99V = 0.072A

Maximum number of circuits = 6

Relay current setting, $I_r(I>) = 0.8A$

Relay primary operating current,

$$I_{op} = 500 \ x \ (0.8 + (6 \ x \ 0.072))$$

= 500 x 1.232
= 616A (141%-full load current)

Therefore, by setting Ir (I>) = 0.8A, the primary operating current of the busbar protection meets the requirements stated earlier.

18.2.1. STABILISING RESISTOR

The required value of the stabilising resistor is:

$$R_{ST} = \frac{V_S}{I_r}$$
$$= \frac{99}{0.8}$$
$$= 124\Omega$$

Therefore the standard 220Ω variable resistor can be used.

Current transformer requirements

To ensure that internal faults are cleared in the shortest possible time the knee point voltage of the current transformers should be at least 5 times the stability voltage, Vs.

$$V_k/V_S = 4$$

$$V_k = 396V$$

18.2.1. METROSIL NON-LINEAR RESISTOR REQUIREMENTS

If the peak voltage appearing across the relay circuit under maximum internal fault conditions exceeds 3000V peak then a suitable non-linear resistor (Metrosil), externally mounted, should be connected across the relay and stabilising resistor, in order to protect the insulation of the current transformers, relay and interconnecting leads. In the present case the peak voltage can be estimated by the formula:

$$V_{\rm p} = 2\sqrt{2V_{\rm K}(V_{\rm f}-V_{\rm K})}$$

where VK = 396V (In practice this should be the actual current transformer kneepoint voltage, obtained from the current transformer magnetisation curve).

$$V_{r} = If(R_{CT} + 2_{RL} + R_{ST} + R_{r})$$

$$= 15300 \times \frac{1}{500} \times (0.7 + 2 + 124)$$

$$= 30.6 \times 126.7$$

$$= 3877V$$

Therefore substituting these values for VK and Vf into the main formula, it can be seen that the peak voltage developed by the current transformer is:

$$V_{P} = 2\sqrt{2V_{K}(V_{f}-V_{K})}$$

$$= 2\sqrt{2 \times 396 \times (3877 - 396)}$$

$$= 3320V$$

This value is above the maximum of 3000V peak and therefore a non-linear resistor (Metrosil) would have to be connected across the relay and the stabilising resistor. The recommended non-linear resistor type would have to be chosen in accordance with the maximum secondary internal fault current and voltage setting.

18.2.1. BUSBAR SUPERVISION

Whenever possible the supervision primary operating current should not be more than 25 amps or 10% of the smallest circuit, whichever is the greater.

The IN>1 earth fault element in the P140 with its low current settings can be used for busbar supervision.

Assuming that 25A is greater than 10% of the smallest circuit current.

$$IN>1 = 25/500 = 0.05In$$

Using the I>3 element for 3 phase busbar supervision.

The time delay setting of the $I_N>1$ and I>3 elements, used for busbar supervision, is 3s.

Any elements not used should be disabled.

18.2.1. ADVANCED BUSBAR APPLICATION REQUIREMENTS FOR THROUGH FAULT STABILITY

The previous busbar protection example is used here to demonstrate the use of the advanced application requirements for through stability.

To ensure through fault stability with a transient offset in the fault current the required voltage setting is given by:

$$V_S = (0.005 X/R + 0.78) x If (2RL + RCT)$$

To be used when X/R is less or equal to 80. The standard equation should be used for X/R ratios greater than 80. If the calculated value is lower than that given by equation 1 (with K = 1.2) then it should be used instead.

18.2.1. TRANSIENT STABILITY LIMIT

$$V_{s} = 0.005 \text{ X/R} + 0.78 \text{ x } \frac{15300}{500} \text{ x } (0.7 + 2)$$

$$V_{s} = 0.88 \text{ x } 30.6 \text{ x } 2.7$$

$$V_{s} = 73 \text{ V}$$

The relay current setting, Ir = 0.8In

$$R_{ST} = \frac{V_S}{I_r}$$

$$R_{ST} = \frac{73}{0.8} = 91\Omega$$

Assuming $V_K = 4Vs$

$$V_K = 4Vs = 292V$$

Using the advanced application method the knee point voltage requirement has been reduced to 292V compared to the conventional method where the knee point voltage was calculated to be 396V.

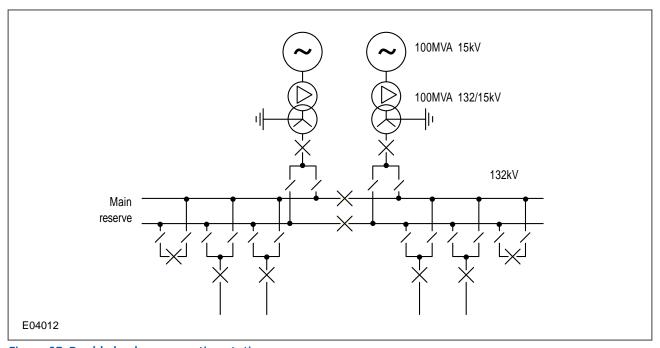


Figure 87: Double busbar generating station

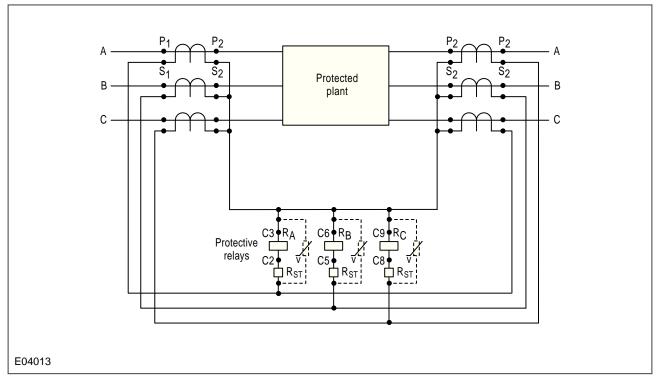


Figure 88: Phase and earth fault differential protection for generators, motors or reactors

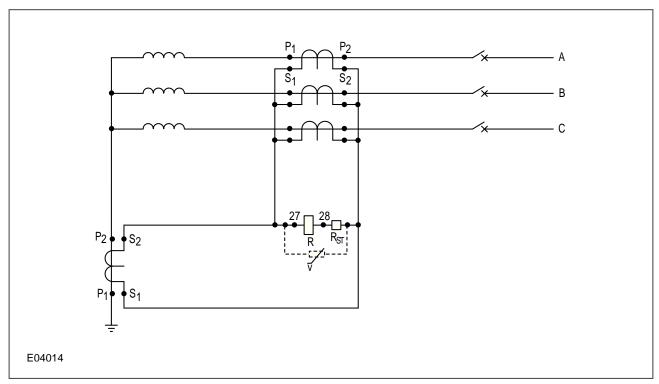


Figure 89: Restricted earth fault protection for 3 phase, 3 wire system-applicable to star connected generators or power transformer windings

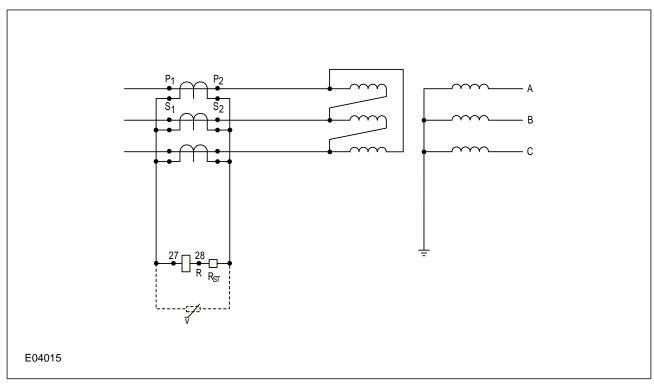


Figure 90: Balanced or restricted earth fault protection for delta winding of a power transformer with supply system earthed

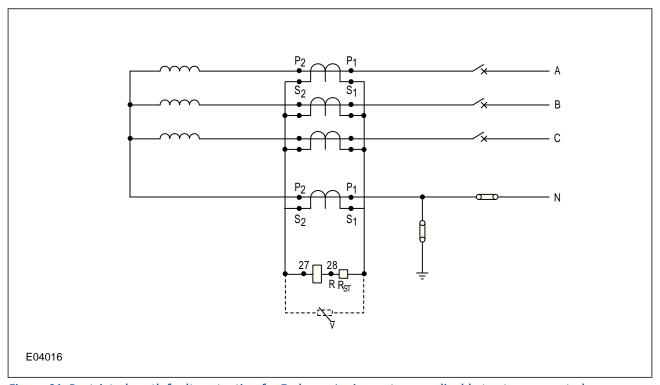


Figure 91: Restricted earth fault protection for 3 phase, 4 wire system-applicable to star connected generators or power transformer windings with neutral earthed at switchgear

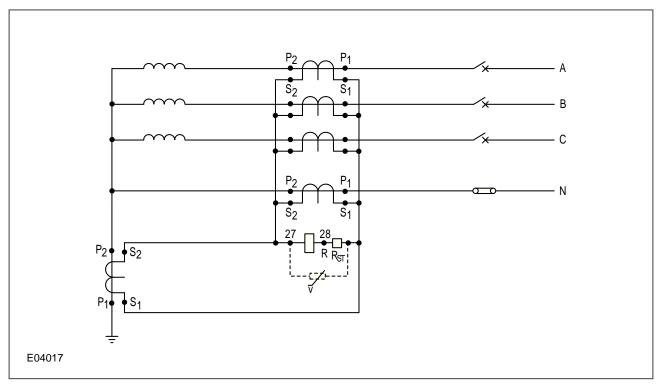


Figure 92: Restricted earth fault protection for 3 phase, 4 wire system-applicable to star connected generators or power transformer windings earthed directly at the star point

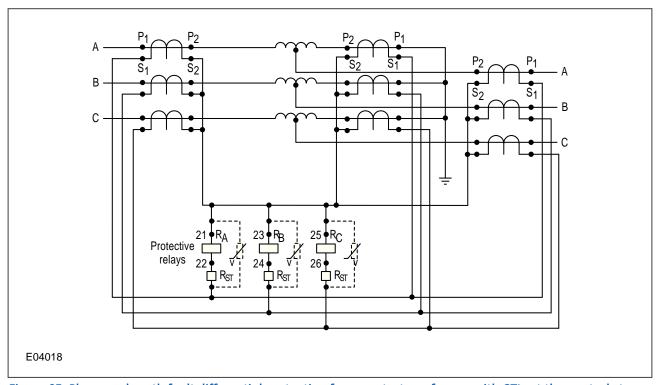


Figure 93: Phase and earth fault differential protection for an auto-transformer with CT's at the neutral star point

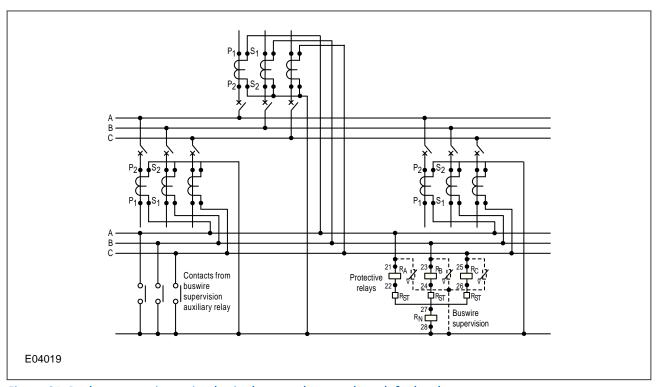


Figure 94: Busbar protection – simple single zone phase and earth fault scheme

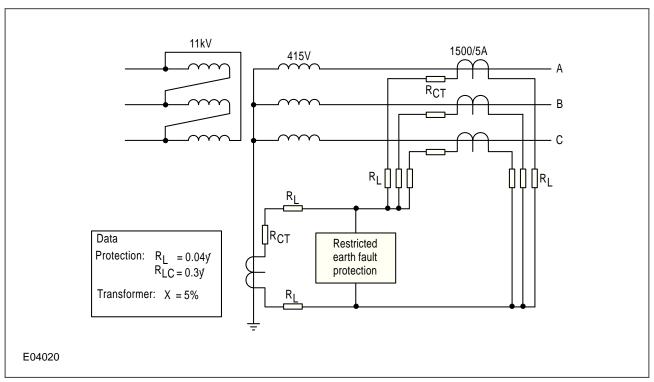


Figure 95: Restricted earth fault protection on a power transformer LV winding

CHAPTER 7

RESTRICTED EARTH FAULT PROTECTION

1 CHAPTER OVERVIEW

The device provides extensive Restricted Earth Fault functionality. This chapter describes the operation of this function including the principles of operation, logic diagrams and applications.

This chapter contains the following sections:

Chapter Overview	171
REF Protection Principles	172
Restricted Earth Fault Protection Implementation	180
Application Notes	183

2 REF PROTECTION PRINCIPLES

Winding-to-core faults in a transformer can be caused by insulation breakdown. Such faults can have very low fault currents, but they still need to be picked up. If such faults are not identified, this could result in extreme damage to very expensive equipment.

Often the associated fault currents are lower than the nominal load current. Neither overcurrent nor percentage differential protection is sufficiently sensitive in this case. We therefore require a different type of protection arrangement. Not only should the protection arrangement be sensitive, but it must create a protection zone, which is limited to each transformer winding. Restricted Earth Fault protection (REF) is the protection mechanism used to protect individual transformer winding sets.

The following figure shows a REF protection arrangement for protecting the delta side of a delta-star transformer.

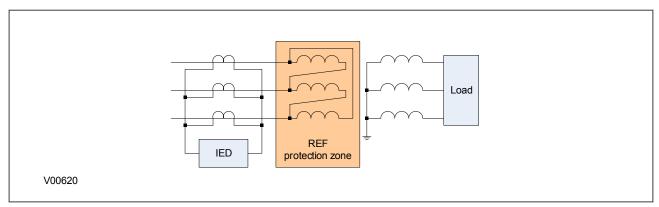


Figure 96: REF protection for delta side

The current transformers measuring the currents in each phase are connected in parallel. The currents from all three phases are summed to form a differential current, sometimes known as a spill current. Under normal operating conditions the currents of the three phases add up to zero resulting in zero spill current. A fault on the star side will also not result in a spill current, as the fault current would simply circulate in the delta windings. However, if any of the three delta windings were to develop a fault, the impedance of the faulty winding would change and that would result in a mismatch between the phase currents, resulting in a spill current. If the spill current is large enough, it will trigger a trip command.

The following figure shows a REF protection arrangement for the star side of a delta-star transformer.

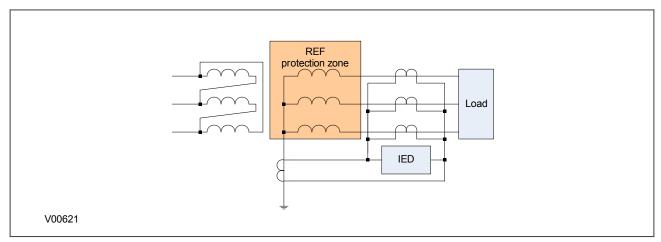


Figure 97: REF protection for star side

Here we have a similar arrangement of current transformers connected in parallel. The difference is that we need to measure the zero sequence current in the neutral line as well. An external unbalanced fault causes zero sequence current to flow through the neutral line, resulting in uneven currents in the phases, which could cause

the protection to maloperate. By measuring this zero sequence current and placing it in parallel with the other three, the currents are balanced, resulting in stable operation. Now only a fault inside the star winding can create an imbalance sufficient to cause a trip.

2.1 RESISTANCE-EARTHED STAR WINDINGS

Most distribution systems use resistance-earthed systems to limit the fault current. Consider the diagram below, which depicts an earth fault on the star winding of a resistance-earthed Dyn transformer (Dyn = Delta-Star with star-point neutral connection).

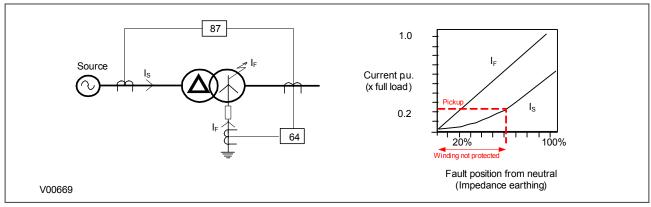


Figure 98: REF Protection for resistance-earthed systems

The value of fault current (I_F) depends on two factors:

- The value of earthing resistance (which makes the fault path impedance negligible)
- The fault point voltage (which is governed by the fault location).

Because the fault current (I_F) is governed by the resistance, its value is directly proportional to the location of the fault.

A restricted earth fault element is connected to measure I_F directly. This provides very sensitive earth fault protection. The overall differential protection is less sensitive, since it only measures the HV current I_S . The value of I_S is limited by the number of faulty secondary turns in relation to the HV turns.

2.2 SOLIDLY-EARTHED STAR WINDINGS

Most transmission systems use solidly-earthed systems. Consider the diagram below, which depicts an earth fault on the star winding of a solidly-earthed Dyn transformer.

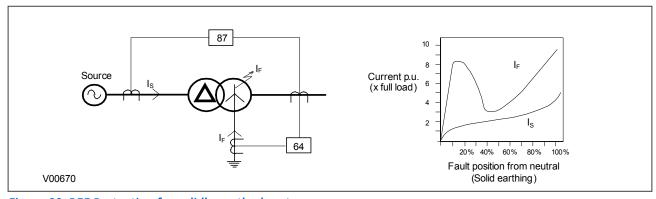


Figure 99: REF Protection for solidly earthed system

In this case, the fault current I_F is dependent on:

- The leakage reactance of the winding
- The impedance in the fault path
- The fault point voltage (which is governed by the fault location)

In this case, the value of fault current (I_F) varies with the fault location in a complex manner.

A restricted earth fault element is connected to measure I_F directly. This provides very sensitive earth fault protection.

For solidly earthed systems, the operating current for the transformer differential protection is still significant for faults over most of the winding. For this reason, independent REF protection may not have been previously considered, especially where an additional device would have been needed. But with this product, it can be applied without extra cost.

2.3 THROUGH FAULT STABILITY

In an ideal world, the CTs either side of a differentially protected system would be identical with identical characteristics to avoid creating a differential current. However, in reality CTs can never be identical, therefore a certain amount of differential current is inevitable. As the through-fault current in the primary increases, the discrepancies introduced by imperfectly matched CTs is magnified, causing the differential current to build up. Eventually, the value of the differential current reaches the pickup current threshold, causing the protection element to trip. In such cases, the differential scheme is said to have lost stability. To specify a differential scheme's ability to restrain from tripping on external faults, we define a parameter called 'through-fault stability limit', which is the maximum through-fault current a system can handle without losing stability.

2.4 RESTRICTED EARTH FAULT TYPES

There are two different types of Restricted Earth Fault; Low Impedance REF (also known as Biased REF) and High Impedance REF. Each method compensates for the effect of through-fault errors in a different manner.

With Low Impedance REF, the through-fault current is measured and this is used to alter the sensitivity of the REF element accordingly by applying a bias characteristic. So the higher the through fault current, the higher the differential current must be for the device to issue a trip signal, Often a transient bias component is added to improve stability during external faults.

Low impedance protection used to be considered less secure than high impedance protection. This is no longer true as numerical IEDs apply sophisticated algorithms to match the performance of high-impedance schemes. Some advantages of using Low Impedance REF are listed below:

- There is no need for dedicated CTs. As a result CT cost is substantially reduced.
- The wiring is simpler as it does not require an external resistor or Metrosil.
- Common phase current inputs can be used.
- It provides internal CT ratio mismatch compensation. It can match CT ratios up to 1:40 resulting flexibility in substation design and reduced cost.
- Advanced algorithms make the protection secure.

With High Impedance REF, there is no bias characteristic, and the trip threshold is set to a constant level. However, the High Impedance differential technique ensures that the impedance of the circuit is sufficiently high such that the differential voltage under external fault conditions is lower than the voltage needed to drive differential current through the device. This ensures stability against external fault conditions so the device will operate only for faults occurring inside the protected zone.

High Impedance REF protection responds to a voltage across the differential junction points. During external faults, even with severe saturation of some of the CTs, the voltage does not rise above certain level, because the other

CTs will provide a lower-impedance path compared with the device input impedance. The principle has been used for more than half a century. Some advantages of using High Impedance REF are listed below:

- It provides a simple proven algorithm, which is fast, robust and secure.
- It is less sensitive to CT saturation.

2.4.1 RESTRICTED EARTH FAULT PROTECTION

The REF protection in the P14x relays may be configured to operate as either a high impedance or low impedance element and the following sections describe the application of the relay in each mode.

The high impedance REF element of the relay shares the same CT input as the SEF protection hence, only one of these elements may be selected. However, the low impedance REF element does not use the SEF input and so may be selected at the same time.

Note:

REF protection is not available in the P144 relay model.

2.4.2 BIASED DIFFERENTIAL PROTECTION

In a biased differential relay, the through current is measured and used to increase the setting of the differential element. For heavy through faults, one CT in the scheme can be expected to become more saturated than the other and hence differential current can be produced. However, biasing will increase the relay setting such that the resulting differential current is insufficient to cause operation of the relay.

The figures below show the operating characteristic for the P14x relay applied for biased REF protection.

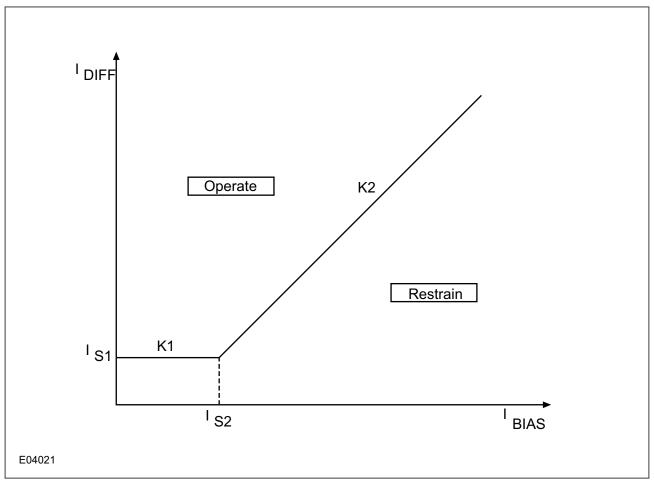


Figure 100: REF bias characteristic

The actual operating characteristic of the element is shown in the figure above.

The formulae used by the relay to calculate the required bias quantity is therefore as follows:

Ibias = ${(Highest of Ia, Ib or Ic) + (Ineutral \times Scaling Factor)}/2$

The reason for the scaling factor included on the neutral current is explained by referring to the figure above.

For IBIAS < IS2

Operate when IDIFF > IS1 + K1.IBIAS

For IBIAS = IS2

Operate when IDIFF > IS1 + K1.IS2

For IBIAS > IS2

Operate when IDIFF > IS1 + K1.IS2 + K2.(IBIAS-IS2)

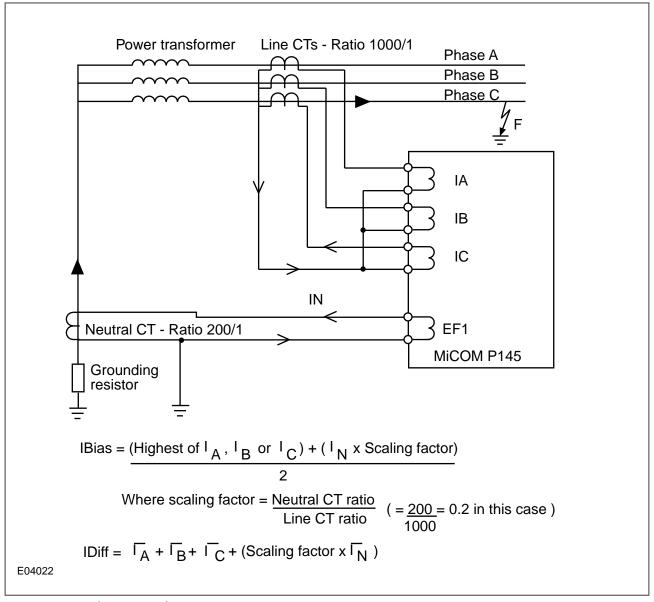


Figure 101: REF bias principle

Where it is required that the neutral CT also drives the EF1 protection element to provide standby earth fault protection, it may be a requirement that the neutral CT has a lower ratio than the line CTs in order to provide better earth fault sensitivity. If this were not accounted for in the REF protection, the neutral current value used would be incorrect. For this reason, the relay automatically scales the level of neutral current used in the bias calculation by a factor equal to the ratio of the neutral to line CT primary ratings. The use of this scaling factor is shown in the figure above, where the formulae for bias and differential currents are given.

2.4.3 HIGH IMPEDANCE REF PRINCIPLE

This scheme is very sensitive and can protect against low levels of fault current, typical of winding faults.

High Impedance REF protection is based on the differential principle. It works on the circulating current principle as shown in the following diagram.

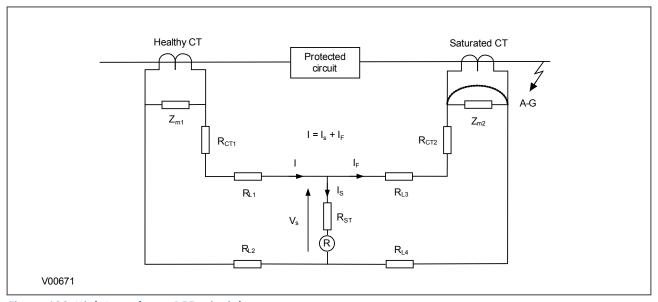


Figure 102: High Impedance REF principle

When subjected to heavy through faults the line current transformer may enter saturation unevenly, resulting in imbalance. To ensure stability under these conditions a series connected external resistor is required, so that most of the unbalanced current will flow through the saturated CT. As a result, the current flowing through the device will be less than the setting, therefore maintaining stability during external faults.

Voltage across REF element $V_S = I_F (R_{CT2} + R_{L3} + R_{L4})$

Stabilising resistor $R_{ST} = V_s/I_s - R_R$

where:

- $I_F = maximum secondary through fault current$
- R_R = device burden
- $R_{CT} = CT$ secondary winding resistance
- R_{L2} and R_{L3} = Resistances of leads from the device to the current transformer
- R_{ST} = Stabilising resistor

High Impedance REF can be used for either delta windings or star windings in both solidly grounded and resistance grounded systems. The connection to a modern IED are as follows:

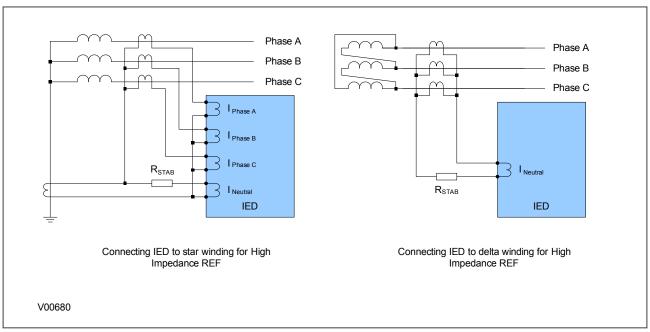


Figure 103: High Impedance REF Connection

3 RESTRICTED EARTH FAULT PROTECTION IMPLEMENTATION

3.1 RESTRICTED EARTH FAULT PROTECTION SETTINGS

Restricted Earth Fault Protection is implemented in the Restricted E/F column of the relevant settings group. It is here that the constants and bias currents are set.

The REF protection may be configured to operate as either a high impedance or biased element.

3.2 LOW IMPEDANCE REF

3.2.1 SETTING THE BIAS CHARACTERISTIC

Low impedance REF uses a bias charactersitic for increasing sensitivity and stabilising for through faults. The current required to trip the differential IED is called the Operate current. This Operate current is a function of the differential current and the bias current according to the bias characteristic.

The differential current is defined as follows:

$$I_{diff} = (\overline{I}_A + \overline{I}_B + \overline{I}_C) + K\overline{I}_N$$

The bias current is as follows:

$$I_{bias} = \frac{1}{2} \left\{ \max \left[|I_A|, |I_B|, |I_C| \right] + K |I_N| \right\}$$

where:

- K = Neutral CT ratio / Line CT ratio
- IN = current measured by the neutral CT

The allowable range for K is:

0.05 < K < 15 for standard CTs

0.05 < K < 20 for sensitive CTs

The operate current is calculated according to the following characteristic:

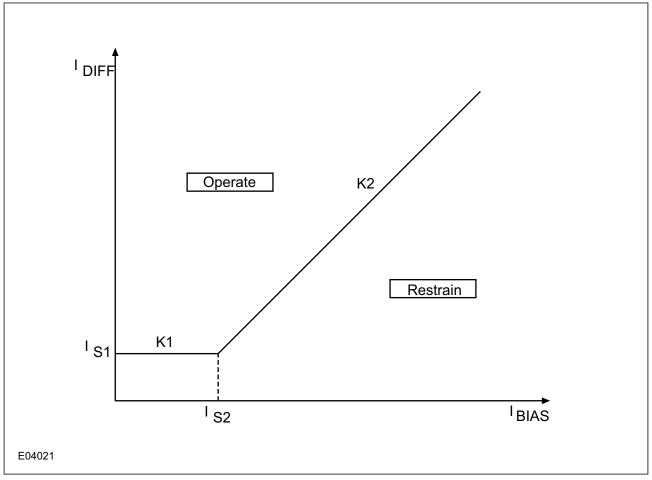


Figure 104: REF bias characteristic

The following settings are provided to define this bias characteristic:

- IREF> Is1: sets the minimum trip threshold
- IREF> Is2: sets the bias current kneepoint whereby the required trip current starts increasing
- IREF> k1: defines the first slope (often set to 0%)
- IREF> k2: defines the second slope

Note:

Is1 and Is2 are relative to the line CT, which is always the reference CT.

3.2.2 DELAYED BIAS

The bias quantity used is actually delayed by one cycle. It is the maximum value of the mean bias quantities calculated within the previous cycle, where the mean bias is the fundamental bias current. This means the bias level, and thus through-fault stability is maintained after an external fault has been cleared.

The algorithm, shown below, is executed eight times per cycle.

 $I_{bias} = Maximum [I_{bias} (n), I_{bias} (n-1), ...I_{bias}, (n-(K-1))]$

It is this delayed bias that is used to calculate the operating current.

3.2.3 TRANSIENT BIAS

If there is a sudden increase in the mean-bias measurement, an additional bias quantity is introduced in the bias calculation. Transient Bias provides stability for external faults where CT saturation might occur.

The transient bias function enhances the stability of the differential element during external faults and allows for the time delay in CT saturation caused by small external fault currents and high X/R ratios.

No transient bias is produced under load switching conditions, or when the CT comes out of saturation.

3.3 HIGH IMPEDANCE REF

The device provides a high impedance restricted earth fault protection function. An external resistor is required to provide stability in the presence of saturated line current transformers. Current transformer supervision signals do not block the high impedance REF protection. The appropriate logic must be configured in PSL to block the high impedance REF when any of the above signals is asserted.

3.3.1 HIGH IMPEDANCE REF CALCULATION PRINCIPLES

The primary operating current (Iop) is a function of the current transformer ratio, the device operate current (*IREF>Is*), the number of current transformers in parallel with a REF element (n) and the magnetizing current of each current transformer (Ie) at the stability voltage (Vs). This relationship can be expressed in three ways:

1. The maximum current transformer magnetizing current to achieve a specific primary operating current with a particular operating current:

$$I_e < \frac{1}{n} \left(\frac{I_{op}}{CT\ ratio} - [IREF > Is] \right)$$

2. The maximum current setting to achieve a specific primary operating current with a given current transformer magnetizing current:

$$[IREF > Is] < \left(\frac{I_{op}}{CT\ ratio} - nI_{e}\right)$$

3. The protection primary operating current for a particular operating current with a particular level of magnetizing current:

$$I_{op} = (CT \ ratio)([IREF > Is] + nI_e)$$

To achieve the required primary operating current with the current transformers that are used, you must select a current setting for the high impedance element, as shown in item 2 above. You can calculate the value of the stabilising resistor (R_{ST}) in the following manner.

$$R_{st} = \frac{Vs}{\left[IREF > Is\right]} = \frac{I_F \left(R_{CT} + 2R_L\right)}{\left[IREF > Is\right]}$$

where:

- R_{CT} = the resistance of the CT winding
- R_L = the resistance of the lead from the CT to the IED.

Note:

The above formula assumes negligible relay burden.

We recommend a stabilizing resistor, which is continuously adjustable up to its maximum declared resistance.

4 APPLICATION NOTES

4.1 STAR WINDING RESISTANCE EARTHED

Consider the following resistance earthed star winding below.

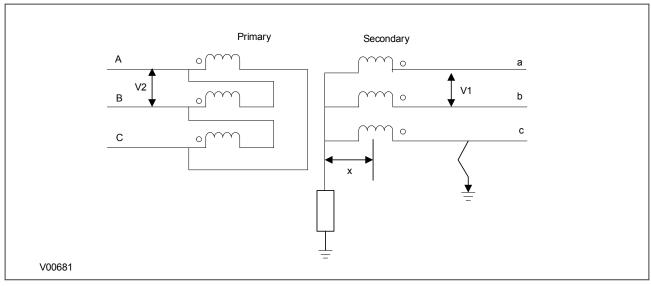


Figure 105: Star winding, resistance earthed

An earth fault on such a winding causes a current which is dependent on the value of earthing impedance. This earth fault current is proportional to the distance of the fault from the neutral point since the fault voltage is directly proportional to this distance.

The ratio of transformation between the primary winding and the short circuited turns also varies with the position of the fault. Therefore the current that flows through the transformer terminals is proportional to the square of the fraction of the winding which is short circuited.

The earthing resistor is rated to pass the full load current $I_{FLC} = V1/\sqrt{3}R$

Assuming that V1 = V2 then T2 = $\sqrt{3}$ T1

For a fault at x PU distance from the neutral, the fault current If = $xV1/\sqrt{3}R$

Therefore the secondary fault current referred to the primary is $I_{primary} = x^2 I_{FLC} / \sqrt{3}$

If the fault is a single end fed fault, the primary current should be greater than 0.2 pu (Is1 default setting) for the differential protection to operate. Therefore $x^2/\sqrt{3} > 20\%$

The following diagram shows that 41% of the winding is protected by the differential element.

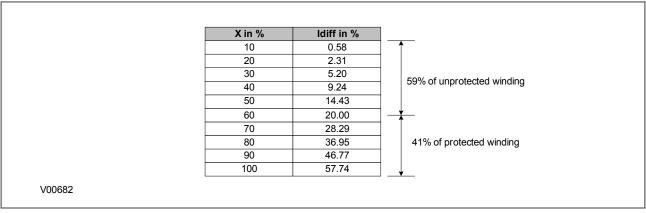


Figure 106: Percentage of winding protected

4.2 LOW IMPEDANCE REF PROTECTION APPLICATION

4.2.1 SETTING GUIDELINES FOR BIASED OPERATION

Two bias settings are provided in the REF characteristic. The K1 level of bias is applied up to through currents of Is2, which is normally set to the rated current of the transformer. K1 is normally be set to 0% to give optimum sensitivity for internal faults. However, if any CT mismatch is present under normal conditions, then K1 may be increased accordingly, to compensate. We recommend a setting of 20% in this case.

K2 bias is applied for through currents above Is2 and would typically be set to 150%.

According to ESI 48-3 1977, typical settings for the Is1 thresholds are 10-60% of the winding rated current when solidly earthed and 10-25% of the minimum earth fault current for a fault at the transformer terminals when resistance earthed.

4.2.2 LOW IMPEDANCE REF SCALING FACTOR

The three line CTs are connected to the three-phase CTs, and the neutral CT is connected to the neutral CT input. These currents are then used internally to derive both a bias and a differential current quantity for use by the low impedance REF protection. The advantage of this mode of connection is that the line and neutral CTs are not differentially connected, so the neutral CT can also be used to provide the measurement for the Standby Earth Fault Protection. Also, no external components such as stabilizing resistors or Metrosils are required.

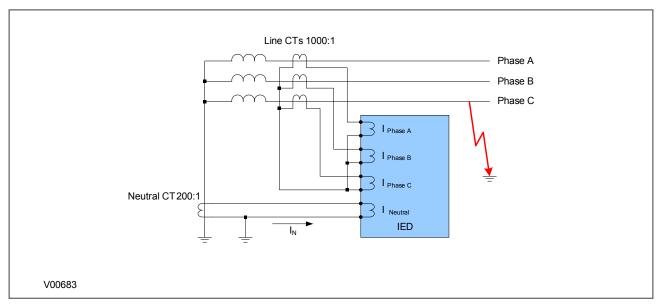


Figure 107: Low Impedance REF Scaling Factor

Another advantage of Low Impedance REF protection is that you can use a neutral CT with a lower ratio than the line CTs in order to provide better earth fault sensitivity. In the bias calculation, the device applies a scaling factor to the neutral current. This scaling factor is as follows:

Scaling factor = K = Neutral CT ratio / Line CT ratio

This results in the following differential and bias current equations:

$$I_{diff} = (\overline{I}_A + \overline{I}_B + \overline{I}_C) + K\overline{I}_N$$

$$I_{bias} = \frac{1}{2} \left\{ \max \left[\left| I_A \right|, \left| I_B \right|, \left| I_C \right| \right] + K \left| I_N \right| \right\}$$

4.2.3 PARAMETER CALCULATIONS

Consider a solidly earthed 90 MVA 132 kV transformer with a REF-protected star winding. Assume line CTS with a ratio of 400:1.

Is1 is set to 10% of the winding nominal current:

- $= (0.1 \times 90 \times 10^6) / (\sqrt{3} \times 132 \times 10^3)$
- = 39 Amps primary
- = 39/400 = 0.0975 Amps secondary (approx 0.1 A)

Is2 is set to the rated current of the transformer:

- $= 90 \times 10^6 / (\sqrt{3} \times 132 \times 10^3)$
- = 390 Amps primary
- = 390/400 = 0.975 Amps secondary (approx 1 A)

Set **K1** to 0% and **K2** to 150%

4.3 HIGH IMPEDANCE REF PROTECTION APPLICATION

4.3.1 HIGH IMPEDANCE REF OPERATING MODES

In the examples below, the respective Line CTS and measurement CTs must have the same CT ratios and similar magnetising characteristics.

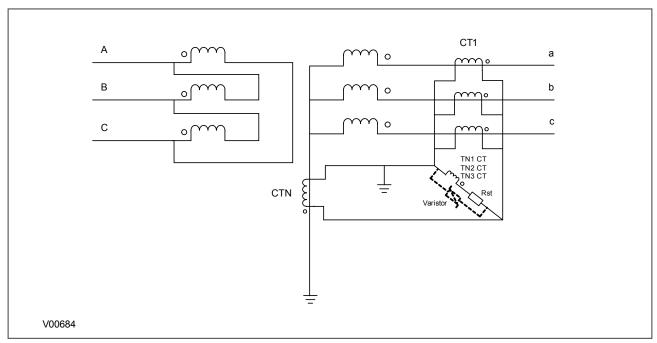


Figure 108: Hi-Z REF protection for a grounded star winding

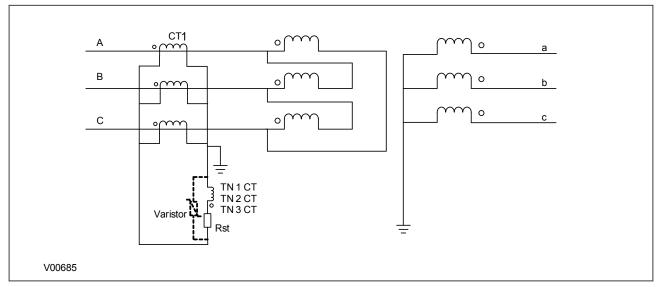


Figure 109: Hi-Z REF protection for a delta winding

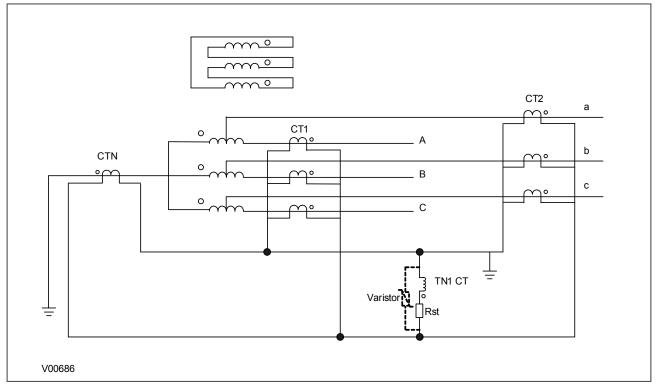


Figure 110: Hi-Z REF Protection for autotransformer configuration

4.3.2 SETTING GUIDELINES FOR HIGH IMPEDANCE OPERATION

This scheme is very sensitive and can protect against low levels of fault current in resistance grounded systems. In this application, the *IREF>Is* settings should be chosen to provide a primary operating current less than 10-25% of the minimum earth fault level.

This scheme can also be used in a solidly grounded system. In this application, the *IREF>Is* settings should be chosen to provide a primary operating current between 10% and 60 % of the winding rated current.

The following diagram shows the application of a high impedance REF element to protect the LV winding of a power transformer.

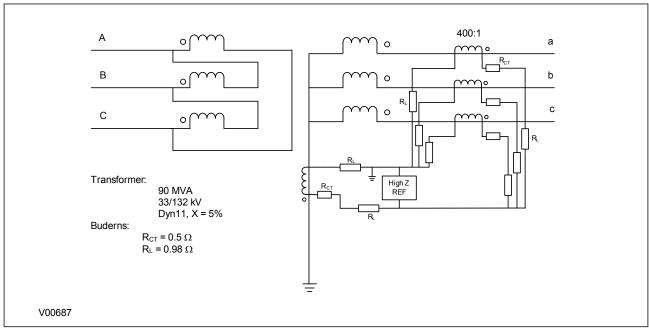


Figure 111: High Impedance REF for the LV winding

4.3.2.1 STABILITY VOLTAGE CALCULATION

The transformer full load current, IFLC, is:

$$I_{FLC} = (90 \times 10^6) / (132 \times 10^3 \times \sqrt{3}) = 394 \text{ A}$$

To calculate the stability voltage the maximum through fault level should be considered. The maximum through fault level, ignoring the source impedance, I_F, is:

$$I_F = I_{FLC} / X_{TX} = 394 / 0.05 = 7873 A$$

The required stability voltage, VS, and assuming one CT saturated is:

$$V_S = KI_F(R_{CT} + 2R_L)$$

The following figure can be used to determine the K factor and the operating time. The K factor is valid when:

• 5 ≤ X/R ≤ 120

and

• 0.5ln ≤ l f ≤ 40ln

We recommend a value of VK/VS = 4.

With the transformer at full load current and percentage impedance voltage of 394A and 5% respectively, the prospective fault current is 7873 A and the required stability voltage Vs (assuming that one CT is saturated) is:

$$V_s = 0.9 \times 7873 \times (0.5 + 2 \times 0.98) / 400 = 45.5 \text{ V}$$

The CTs knee point voltage should be at least 4 times Vs so that an average operating time of 40 ms is achieved.

4.3.2.2 PRIMARY CURRENT CALCULATION

The primary operating current should be between 10 and 60 % of the winding rated current. Assuming that the relay effective setting or primary operating current is approximately 30% of the full load current, the calculation below shows that a setting of less than 0.3 A is required.

Effective setting = $0.3I_{FLC}$ / CT Ratio = $30.3 \times 394 / 400$ = approximately 0.3 A

4.3.2.3 STABILISING RESISTOR CALCULATION

Assuming that a setting of 0.1A is selected the value of the stabilizing resistor, RST, required is

$$R_{ST} = V_S / (IREF > Is1 (HV)) = 45.5 / 0.1 = 455 \text{ ohms}$$

To achieve an average operating time of 40 ms, Vk/Vs should be 3.5.

The Kneepoint voltage is:

$$V_K = 4V_S = 4 \times 45.5 = 182 \text{ V}.$$

If the actual V_K is greater than 4 times V_S , then the K factor increases. In this case, V_S should be recalculated.

Note:

K can reach a maximum value of approximately 1.

4.3.2.4 CURRENT TRANSFORMER CALCULATION

The effective primary operating current setting is:

$$I_P = N(I_S + nI_\rho)$$

By re-arranging this equation, you can calculate the excitation current for each of the current transformers at the stability voltage. This turns out to be:

$$I_e = (0.3 - 0.1) / 4 = 0.05 A$$

In summary, the current transformers used for this application must have a kneepoint voltage of 182 V or higher (note that maximum Vk/Vs that may be considered is 16 and the maximum K factor is 1), with a secondary winding resistance of 0.5 ohms or lower and a magnetizing current at 45.5 V of less than 0.05 A.

Assuming a CT kneepoint voltage of 200 V, the peak voltage can be estimated as:

$$V_P = 2\sqrt{2}V_K(V_F-V_K) = 2\sqrt{2}(200)(9004-200) = 3753 \text{ V}$$

This value is above the peak voltage of 3000 V and therefore a non-linear resistor is required.

Note:

The kneepoint voltage value used in the above formula should be the actual voltage obtained from the CT magnetizing characteristic and not a calculated value.

Note:

One stabilizing resistor, Alstom part No. ZB9016 756, and one varistor, Alstom part No. 600A/S1/S256 might be used.

CHAPTER 8

CB FAIL PROTECTION

1 CHAPTER OVERVIEW

The device provides a Circuit Breaker Fail Protection function. This chapter describes the operation of this function including the principles, logic diagrams and applications.

This chapter contains the following sections:

Chapter Overview	193
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2 CIRCUIT BREAKER FAIL PROTECTION

When a fault occurs, one or more protection devices will operate and issue a trip command to the relevant circuit breakers. Operation of the circuit breaker is essential to isolate the fault and prevent, or at least limit, damage to the power system. For transmission and sub-transmission systems, slow fault clearance can also threaten system stability.

For these reasons, it is common practice to install Circuit Breaker Failure protection (CBF). CBF protection monitors the circuit breaker and establishes whether it has opened within a reasonable time. If the fault current has not been interrupted following a set time delay from circuit breaker trip initiation, the CBF protection will operate, whereby the upstream circuit breakers are back-tripped to ensure that the fault is isolated.

CBF operation can also reset all start output contacts, ensuring that any blocks asserted on upstream protection are removed.

3 CIRCUIT BREAKER FAIL IMPLEMENTATION

Circuit Breaker Failure Protection is implemented in the CB FAIL column of the relevant settings group.

3.1 CIRCUIT BREAKER FAIL TIMERS

The circuit breaker failure protection incorporates two timers, *CB Fail 1 Timer* and *CB Fail 2 Timer*, allowing configuration for the following scenarios:

- Simple CBF, where only CB Fail 1 Timer is enabled. For any protection trip, the CB Fail 1 Timer is started, and normally reset when the circuit breaker opens to isolate the fault. If breaker opening is not detected, the CB Fail 1 Timer times out and closes an output contact assigned to breaker fail (using the programmable scheme logic). This contact is used to back-trip upstream switchgear, generally tripping all infeeds connected to the same busbar section.
- A retripping scheme, plus delayed back-tripping. Here, CB Fail 1 Timer is used to issue a trip command to a
 second trip circuit of the same circuit breaker. This requires the circuit breaker to have duplicate circuit
 breaker trip coils. This mechanism is known as retripping. If retripping fails to open the circuit breaker, a
 back-trip may be issued following an additional time delay. The back-trip uses CB Fail 2 Timer, which was
 also started at the instant of the initial protection element trip.

You can configure the CBF elements *CB Fail 1 Timer* and *CBF Fail 2 Timer* to operate for trips triggered by protection elements within the device. Alternatively you can use an external protection trip by allocating one of the opto-inputs to the *External Trip* DDB signal in the PSL.

You can reset the CBF from a breaker open indication (from the pole dead logic) or from a protection reset. In these cases resetting is only allowed if the undercurrent elements have also been reset. The resetting mechanism is determined by the settings **Volt Prot Reset** and **Ext Prot Reset**.

The resetting options are summarised in the following table:

Initiation (Menu Selectable)	CB Fail Timer Reset Mechanism		
Current based protection	The resetting mechanism is fixed (e.g. 50/51/46/21/87) IA< operates AND IB< operates AND IC< operates AND IN< operates		
Sensitive Earth Fault element	The resetting mechanism is fixed. ISEF< Operates		
Non-current based protection (e.g. 27/59/81/32L)	Three options are available: • All I< and IN< elements operate • Protection element reset AND all I< and IN< elements operate • CB open (all 3 poles) AND all I< and IN< elements operate		
External protection	Three options are available. • All I< and IN< elements operate • External trip reset AND all I< and IN< elements operate • CB open (all 3 poles) AND all I< and IN< elements operate		

3.2 ZERO CROSSING DETECTION

When there is a fault and the circuit breaker interrupts the CT primary current, the flux in the CT core decays to a residual level. This decaying flux introduces a decaying DC current in the CT secondary circuit known as subsidence current. The closer the CT is to its saturation point, the higher the subsidence current.

The time constant of this subsidence current depends on the CT secondary circuit time constant and it is generally long. If the protection clears the fault, the CB Fail function should reset fast to avoid maloperation due to the subsidence current. To compensate for this the device includes a zero-crossing detection algorithm, which ensures that the CB Fail re-trip and back-trip signals are not asserted while subsidence current is flowing. If all the samples within half a cycle are greater than or smaller than 0 A (10 mS for a 50 Hz system), then zero crossing detection is asserted, thereby blocking the operation of the CB Fail function. The zero-crossing detection algorithm is used

after the circuit breaker in the primary system has opened ensuring that the only current flowing in the AC secondary circuit is the subsidence current.

4 CIRCUIT BREAKER FAIL LOGIC

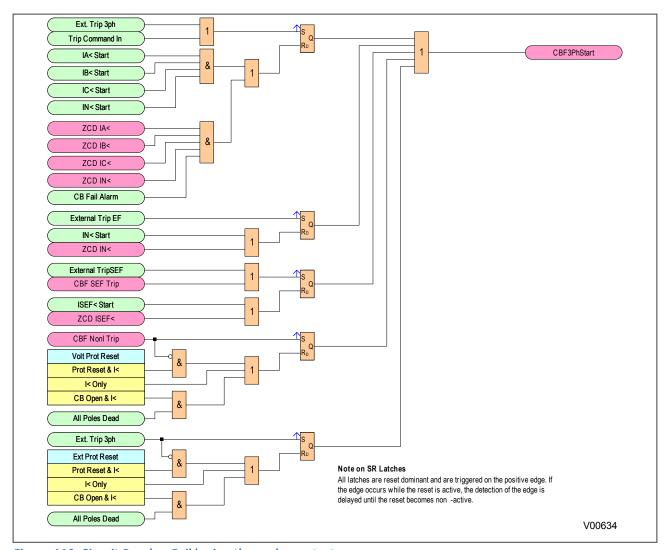


Figure 112: Circuit Breaker Fail logic - three phase start

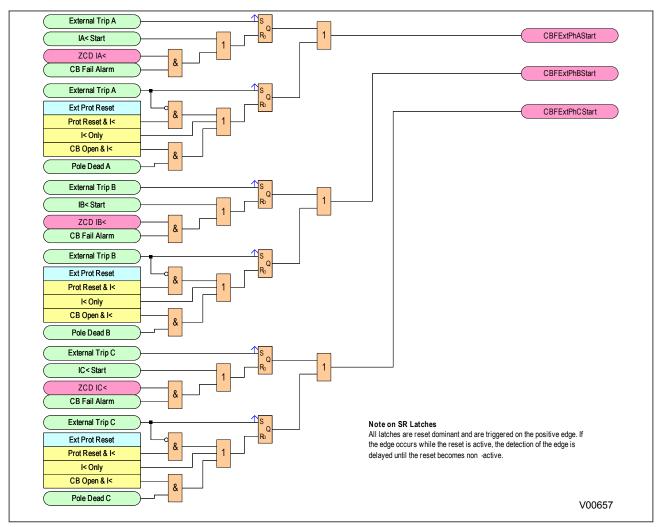


Figure 113: Circuit Breaker Fail logic - single phase start

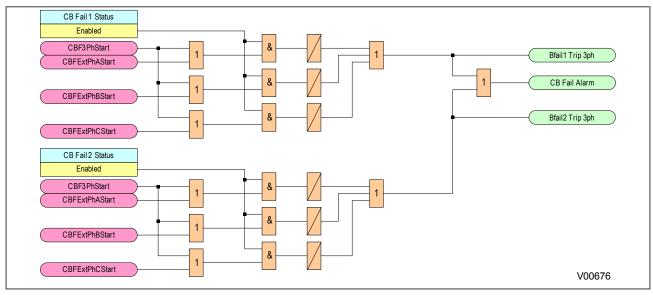


Figure 114: Circuit Breaker Fail Trip and Alarm

5 UNDERCURRENT AND ZCD LOGIC FOR CB FAIL

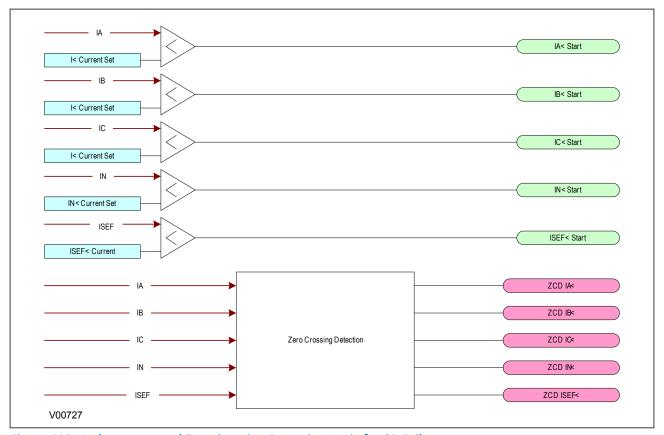


Figure 115: Undercurrent and Zero Crossing Detection Logic for CB Fail

6 CB FAIL SEF PROTECTION LOGIC

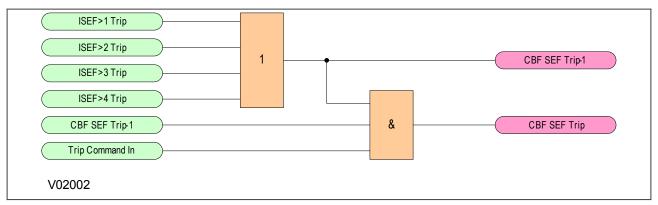


Figure 116: CB Fail SEF Protection Logic

7 CB FAIL NON CURRENT PROTECTION LOGIC

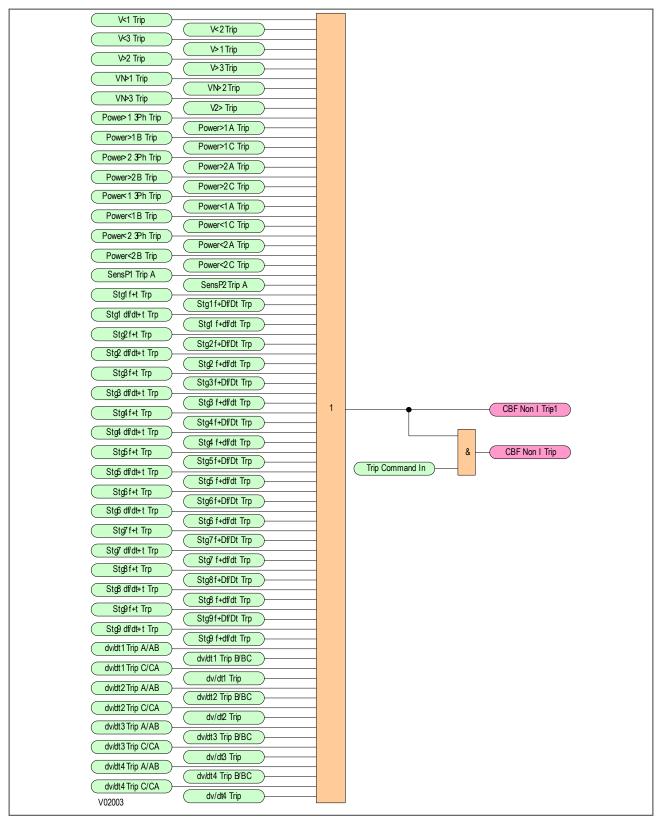


Figure 117: CB Fail Non Current Protection Logic

CB Closed 3 ph CB in Service V02026

Figure 118: Circuit Breaker mapping

9 APPLICATION NOTES

9.1 RESET MECHANISMS FOR CB FAIL TIMERS

It is common practise to use low set undercurrent elements to indicate that circuit breaker poles have interrupted the fault or load current. This covers the following situations:

- Where circuit breaker auxiliary contacts are defective, or cannot be relied on to definitely indicate that the breaker has tripped.
- Where a circuit breaker has started to open but has become jammed. This may result in continued arcing at
 the primary contacts, with an additional arcing resistance in the fault current path. Should this resistance
 severely limit fault current, the initiating protection element may reset. Therefore, reset of the element may
 not give a reliable indication that the circuit breaker has opened fully.

For any protection function requiring current to operate, the device uses operation of undercurrent elements to detect that the necessary circuit breaker poles have tripped and reset the CB fail timers. However, the undercurrent elements may not be reliable methods of resetting CBF in all applications. For example:

- Where non-current operated protection, such as under/overvoltage or under/overfrequency, derives
 measurements from a line connected voltage transformer. Here, I< only gives a reliable reset method if the
 protected circuit would always have load current flowing. In this case, detecting drop-off of the initiating
 protection element might be a more reliable method.
- Where non-current operated protection, such as under/overvoltage or under/overfrequency, derives measurements from a busbar connected voltage transformer. Again using I< would rely on the feeder normally being loaded. Also, tripping the circuit breaker may not remove the initiating condition from the busbar, and so drop-off of the protection element may not occur. In such cases, the position of the circuit breaker auxiliary contacts may give the best reset method.

9.2 SETTING GUIDELINES (CB FAIL TIMER)

The following timing chart shows the CB Fail timing during normal and CB Fail operation. The maximum clearing time should be less than the critical clearing time which is determined by a stability study. The CB Fail back-up trip time delay considers the maximum CB clearing time, the CB Fail reset time plus a safety margin. Typical CB clearing times are 1.5 or 3 cycles. The CB Fail reset time should be short enough to avoid CB Fail back-trip during normal operation. Phase and ground undercurrent elements must be asserted for the CB Fail to reset. The assertion of the undercurrent elements might be delayed due to the subsidence current that might be flowing through the secondary AC circuit.

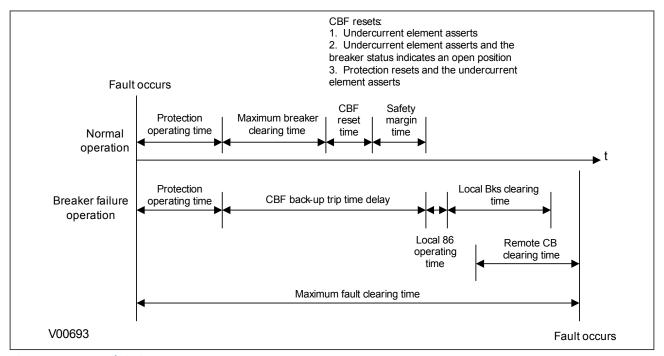


Figure 119: CB Fail timing

The following examples consider direct tripping of a 2-cycle circuit breaker. Typical timer settings to use are as follows:

CB Fail Reset Mechanism	tBF Time Delay	Typical Delay For 2 Cycle Circuit Breaker
Initiating element reset	CB interrupting time + element reset time (max.) + error in tBF timer + safety margin	50 + 50 + 10 + 50 = 160 ms
CB open	CB auxiliary contacts opening/ closing time (max.) + error in tBF timer + safety margin	50 + 10 + 50 = 110 ms
Undercurrent elements	CB interrupting time + undercurrent element (max.) + safety margin operating time	50 + 25 + 50 = 125 ms

Note:

All CB Fail resetting involves the operation of the undercurrent elements. Where element resetting or CB open resetting is used, the undercurrent time setting should still be used if this proves to be the worst case. Where auxiliary tripping relays are used, an additional 10-15 ms must be added to allow for trip relay operation.

9.3 SETTING GUIDELINES (UNDERCURRENT)

The phase undercurrent settings (I<) must be set less than load current to ensure that I< operation correctly indicates that the circuit breaker pole is open. A typical setting for overhead line or cable circuits is 20%In. Settings of 5% of In are common for generator CB Fail.

The earth fault undercurrent elements must be set less than the respective trip. For example:

IN < = (IN > trip)/2

CHAPTER 9

CURRENT TRANSFORMER REQUIREMENTS

1 CHAPTER OVERVIEW

This cha	pter coi	ntains 1	the fo	llowing	sections

Chapter Overview	207

CT requirements 208

2 CT REQUIREMENTS

The current transformer requirements are based on a maximum fault current of 50 times the rated current (In) with the device having an instantaneous overcurrent setting of 25 times the rated current. The current transformer requirements are designed to provide operation of all protection elements.

Where the criteria for a specific application are in excess of this, or the lead resistance exceeds the limiting lead resistance shown in the following table, the CT requirements may need to be modified according to the formulae in the subsequent sections:

Nominal Rating	Nominal Output	Accuracy Class	Accuracy Limited Factor	Limiting Lead Resistance
1A	2.5 VA	10P	20	1.3 ohms
5A	7.5 VA	10P	20	0.11 ohms

The formula subscripts used in the subsequent sections are as follows:

 V_K = Required CT knee-point voltage (volts)

 $I_f = Maximum through-fault current level (amps)$

 I_n = Rated secondary current (amps)

 I_{CD} = Maximum prospective secondary earth fault current or 31 times I> setting (whichever is lower) (amps)

 I_{CD} = Maximum prospective secondary phase fault current or 31 times I> setting (whichever is lower) (amps)

 R_{CT} = Resistance of current transformer secondary winding (ohms)

 R_L = Resistance of a single lead from relay to current transformer (ohms)

 R_{st} = Value of stabilising resistor for REF applications (ohms)

 I_S = Current setting of REF elements (amps)

 V_S = Required stability voltage

2.1 PHASE OVERCURRENT PROTECTION

2.1.1 DIRECTIONAL ELEMENTS

Time-delayed phase overcurrent elements

$$V_{K} = \frac{I_{cp}}{2} (R_{CT} + R_{L} + R_{p})$$

Instantaneous phase overcurrent elements

$$V_{K} = \frac{I_{fp}}{2} (R_{CT} + R_{L} + R_{p})$$

2.1.2 NON-DIRECTIONAL ELEMENTS

Time-delayed phase overcurrent elements

$$V_K = \frac{I_{cp}}{2} (R_{CT} + R_L + R_p)$$

Instantaneous phase overcurrent elements

$$V_K = I_{sp}(R_{CT} + R_L + R_p)$$

2.2 EARTH FAULT PROTECTION

2.2.1 DIRECTIONAL ELEMENTS

Instantaneous earth fault overcurrent elements

$$V_{K} = \frac{I_{fn}}{2} (R_{CT} + 2R_{L} + R_{p} + Rn)$$

2.2.2 NON-DIRECTIONAL ELEMENTS

Time-delayed earth fault overcurrent elements

$$V_{K} = \frac{I_{cn}}{2} (R_{CT} + 2R_{L} + R_{p} + R_{n})$$

Instantaneous earth fault overcurrent elements

$$V_K = I_{sn}(R_{CT} + 2R_L + R_n + R_n)$$

2.3 SEF PROTECTION (RESIDUALLY CONNECTED)

2.3.1 DIRECTIONAL ELEMENTS

Time delayed SEF protection

$$V_K \ge \frac{I_{cn}}{2} (R_{CT} + 2R_L + R_p + Rn)$$

Instantaneous SEF protection

$$V_{K} \ge \frac{I_{fn}}{2} (R_{CT} + 2R_{L} + R_{p} + Rn)$$

2.3.2 NON-DIRECTIONAL ELEMENTS

Time delayed SEF protection

$$V_K \ge \frac{I_{cn}}{2} (R_{CT} + 2R_L + R_p + Rn)$$

Instantaneous SEF protection

$$V_K \ge \frac{I_{sn}}{2} (R_{CT} + 2R_L + R_p + Rn)$$

2.4 SEF PROTECTION (CORE-BALANCED CT)

2.4.1 DIRECTIONAL ELEMENTS

Instantaneous element

$$V_K \ge \frac{I_{fn}}{2} (R_{CT} + 2R_L + Rn)$$

Note

Ensure that the phase error of the applied core balance current transformer is less than 90 minutes at 10% of rated current and less than 150 minutes at 1% of rated current.

2.4.2 NON-DIRECTIONAL ELEMENTS

Time delayed element

$$V_K \ge \frac{I_{cn}}{2} (R_{CT} + 2R_L + Rn)$$

Instantaneous element

$$V_K \ge I_{sn}(R_{CT} + 2R_L + Rn)$$

Note:

Ensure that the phase error of the applied core balance current transformer is less than 90 minutes at 10% of rated current and less than 150 minutes at 1% of rated current.

2.5 LOW IMPEDANCE REF PROTECTION

For X/R < 40 and I_f < 15 I_n

$$V_K \ge 24I_n(R_{CT} + 2R_L)$$

For 40 < X/R < 120 and $15I_n < If < <math>40I_n$

$$V_{\scriptscriptstyle K} \geq 48I_{\scriptscriptstyle n}(R_{\scriptscriptstyle CT}+2R_{\scriptscriptstyle L})$$

Note:

Class x or Class 5P CTs should be used for low impedance REF applications.

2.6 HIGH IMPEDANCE REF PROTECTION

The high impedance REF element will maintain stability for through-faults and operate in less than 40ms for internal faults, provided the following equations are met:

$$R_{st} = \frac{I_f (R_{CT} + 2R_L)}{I_s}$$

$$V_{K} \ge 4I_{s}R_{st}$$

Note:

Class x CTs should be used for high impedance REF applications.

2.7 HIGH IMPEDANCE BUSBAR PROTECTION

The high impedance bus bar protection element will maintain stability for through faults and operate for internal faults. You should select Vk/Vs based on the X/R of the system. The equation is:

$$V_S = K^*I_f^*(R_{CT} + R_L)$$

For X/R <= 40

$$V_k/V_S >= 2$$

Typical operating time = 25 ms

For X/R > 40

$$V_k/V_s>=4$$

Typical operating time = 30 ms

Note:

K is a constant affected by the dynamic response of the device. K is always equal to 1.

2.8 USE OF METROSIL NON-LINEAR RESISTORS

Current transformers can develop high peak voltages under internal fault conditions. Metrosils are used to limit these peak voltages to a value below the maximum withstand voltage (usually 3 kV).

You can use the following formulae to estimate the peak transient voltage that could be produced for an internal fault. The peak voltage produced during an internal fault is a function of the current transformer kneepoint voltage and the prospective voltage that would be produced for an internal fault if current transformer saturation did not occur.

$$Vp = 2\sqrt{2VK(V_F-V_K)}$$

$$Vf = I'f(R_{CT} + 2_{RL} + R_{ST})$$

where:

- Vp = Peak voltage developed by the CT under internal fault conditions
- Vk = Current transformer kneepoint voltage
- Vf = Maximum voltage that would be produced if CT saturation did not occur
- I'f = Maximum internal secondary fault current
- R_{CT} = Current transformer secondary winding resistance
- R_L = Maximum lead burden from current transformer to relay
- R_{ST} = Relay stabilising resistor

You should always use Metrosils when the calculated values are greater than 3000 V. Metrosils are connected across the circuit to shunt the secondary current output of the current transformer from the device to prevent very high secondary voltages.

Metrosils are externally mounted and take the form of annular discs. Their operating characteristics follow the expression:

$$V = CI^{0.25}$$

where:

- V = Instantaneous voltage applied to the Metrosil
- C = Constant of the Metrosil
- I = Instantaneous current through the Metrosil

With a sinusoidal voltage applied across the Metrosil, the RMS current would be approximately 0.52×10^{-5} the peak current. This current value can be calculated as follows:

$$I_{RMS} = 0.52 \left(\frac{\sqrt{2}V_{S(RMS)}}{C}\right)^4$$

where:

V_{S(RMS)} = RMS value of the sinusoidal voltage applied across the metrosil.

This is due to the fact that the current waveform through the Metrosil is not sinusoidal but appreciably distorted.

The Metrosil characteristic should be such that it complies with the following requirements:

- The Metrosil current should be as low as possible, and no greater than 30 mA RMS for 1 A current transformers or 100 mA RMS for 5 A current transformers.
- At the maximum secondary current, the Metrosil should limit the voltage to 1500 V RMS or 2120 V peak for 0.25 second. At higher device voltages it is not always possible to limit the fault voltage to 1500 V rms, so higher fault voltages may have to be tolerated.

The following tables show the typical Metrosil types that will be required, depending on relay current rating, REF voltage setting etc.

Metrosils for devices with a 1 Amp CT

The Metrosil units with 1 Amp CTs have been designed to comply with the following restrictions:

- The Metrosil current should be less than 30 mA rms.
- At the maximum secondary internal fault current the Metrosil should limit the voltage to 1500 V rms if possible.

The Metrosil units normally recommended for use with 1Amp CTs are as shown in the following table:

	Nominal Ch	aracteristic	Recommended	l Metrosil Type
Device Voltage Setting	С	β	Single Pole Relay	Triple Pole Relay
Up to 125 V RMS	450	0.25	600A/S1/S256	600A/S3/1/S802
125 to 300 V RMS	900	0.25	600A/S1/S1088	600A/S3/1/S1195

Note:

Single pole Metrosil units are normally supplied without mounting brackets unless otherwise specified by the customer.

Metrosils for devices with a 5 Amp CT

These Metrosil units have been designed to comply with the following requirements:

- The Metrosil current should be less than 100 mA rms (the actual maximum currents passed by the devices shown below their type description.
- At the maximum secondary internal fault current the Metrosil should limit the voltage to 1500 V rms for 0.25secs. At the higher relay settings, it is not possible to limit the fault voltage to 1500 V rms so higher fault voltages have to be tolerated.

The Metrosil units normally recommended for use with 5 Amp CTs and single pole relays are as shown in the following table:

Secondary Internal Fault Current	Recommended Metrosil types for various voltage settings			
Amps RMS	Up to 200 V RMS	250 V RMS	275 V RMS	300 V RMS
50A	600A/S1/S1213 C = 540/640 35 mA RMS	600A/S1/S1214 C = 670/800 40 mA RMS	600A/S1/S1214 C =670/800 50 mA RMS	600A/S1/S1223 C = 740/870 50 mA RMS
100A	600A/S2/P/ S1217 C = 470/540 70 mA RMS	600A/S2/P/S1215 C = 570/670 75 mA RMS	600A/S2/P/S1215 C =570/670 100 mA RMS	600A/S2/P/S1196 C =620/740 100 mA RMS
150A	600A/S3/P/ S1219 C = 430/500 100 mA RMS	600A/S3/P/S1220 C = 520/620 100 mA RMS	600A/S3/P/S1221 C = 570/670 100 mA RMS	600A/S3/P/S1222 C =620/740 100 mA RMS

In some situations single disc assemblies may be acceptable, contact General Electric for detailed applications.

Note:

The Metrosils recommended for use with 5 Amp CTs can also be used with triple pole devices and consist of three single pole units mounted on the same central stud but electrically insulated from each other. To order these units please specify "Triple pole Metrosil type", followed by the single pole type reference. Metrosil for higher voltage settings and fault currents are available if required.

2.9 USE OF ANSI C-CLASS CTS

Where American/IEEE standards are used to specify CTs, the C class voltage rating can be used to determine the equivalent knee point voltage according to IEC. The equivalence formula is:

 $V_K = 1.05(C \ rating \ in \ volts) + 100R_{CT}$

CHAPTER 10

VOLTAGE PROTECTION FUNCTIONS

1 CHAPTER OVERVIEW

The device provides a wide range of voltage protection functions. This chapter describes the operation of these functions including the principles, logic diagrams and applications.

This chapter contains the following sections:

Chapter Overview	217
Undervoltage Protection	218
Overvoltage Protection	221
Rate of Change of Voltage Protection	224
Residual Overvoltage Protection	226
Negative Sequence Overvoltage Protection	236
Sensitive Overvoltage Supervision	238

2 UNDERVOLTAGE PROTECTION

Undervoltage conditions may occur on a power system for a variety of reasons, some of which are outlined below:

- Undervoltage conditions can be related to increased loads, whereby the supply voltage will decrease in magnitude. This situation would normally be rectified by voltage regulating equipment such as AVRs (Auto Voltage Regulators) or On Load Tap Changers. However, failure of this equipment to bring the system voltage back within permitted limits leaves the system with an undervoltage condition, which must be cleared.
- If the regulating equipment is unsuccessful in restoring healthy system voltage, then tripping by means of an undervoltage element is required.
- Faults occurring on the power system result in a reduction in voltage of the faulty phases. The proportion by
 which the voltage decreases is dependent on the type of fault, method of system earthing and its location.
 Consequently, co-ordination with other voltage and current-based protection devices is essential in order to
 achieve correct discrimination.
- Complete loss of busbar voltage. This may occur due to fault conditions present on the incomer or busbar
 itself, resulting in total isolation of the incoming power supply. For this condition, it may be necessary to
 isolate each of the outgoing circuits, such that when supply voltage is restored, the load is not connected.
 Therefore, the automatic tripping of a feeder on detection of complete loss of voltage may be required. This
 can be achieved by a three-phase undervoltage element.
- Where outgoing feeders from a busbar are supplying induction motor loads, excessive dips in the supply may cause the connected motors to stall, and should be tripped for voltage reductions that last longer than a pre-determined time.

2.1 UNDERVOLTAGE PROTECTION IMPLEMENTATION

Undervoltage Protection is implemented in the *VOLT PROTECTION* column of the relevant settings group. The Undervoltage parameters are contained within the sub-heading *UNDERVOLTAGE*.

The product provides three stages of Undervoltage protection with independent time delay characteristics.

Stage 1 provides a choice of operate characteristics, where you can select between:

- An IDMT characteristic
- DT (Definite Time)

You set this using the *V<1 Function* setting.

The IDMT characteristic is defined by the following formula:

t = K/(M-1)

where:

- K = Time multiplier setting
- t = Operating time in seconds
- M = Measured voltage / IED setting voltage (V<(n) Voltage Set)

The undervoltage stages can be configured either as phase-to-neutral or phase-to-phase voltages in the *V*< *Measur't Mode* cell.

There is no Timer Hold facility for Undervoltage.

Stages 2, 3 and 4 can have definite time characteristics only. This is set, for example, in the *V<2 Status* cell.

Outputs are available for single or three-phase conditions via the *V< Operate Mode* cell for each stage.

V< Measur't Mode V<1 Start A/AB VAB V<1 Voltage Set V<1 Trip A/AB V<1 Time Delay V< Measur't Mode V<1 Start B/B C VBC V<1 Voltage Set V<1 Trip B/BC V<1 Time Delay V< Measur't Mode VC V<1 Start C/CA · VCA V<1 Voltage Set V<1 Trip C/CA V<1 Time Delay All Poles De ad V<1 Start V<1 Poled ead Inh Enabled VTS Fast Block V<1 Timer Block V<1 Trip V< Operate Mode Any Phase Three Phase Note: This diagram does not show all stages. Other stages follow similar principles. VTS Fast Block only applies for directional models V00803

2.2 UNDERVOLTAGE PROTECTION LOGIC

Figure 120: Undervoltage - single and three phase tripping mode (single stage)

The Undervoltage protection function detects when the voltage magnitude for a certain stage falls short of a set threshold. If this happens a *Start* signal, signifying the "Start of protection", is produced. This Start signal can be blocked by the *VTS Fast Block* signal and an *All Poles Dead* signal. This *Start* signal is applied to the timer module to produce the *Trip* signal, which can be blocked by the undervoltage timer block signal (*V<(n) Timer Block*). For each stage, there are three Phase undervoltage detection modules, one for each phase. The three *Start* signals from each of these phases are OR'd together to create a 3-phase Start signal (*V<(n) Start*), which can be be activated when any of the three phases start (Any Phase), or when all three phases start (Three Phase), depending on the chosen *V< Operate Mode* setting.

The outputs of the timer modules are the trip signals which are used to drive the tripping output relay. These tripping signals are also OR'd together to create a 3-phase Trip signal, which are also controlled by the *V< Operate Mode* setting.

If any one of the above signals is low, or goes low before the timer has counted out, the timer module is inhibited (effectively reset) until the blocking signal goes high.

In some cases, we do not want the undervoltage element to trip; for example, when the protected feeder is deenergised, or the circuit breaker is opened, an undervoltage condition would obviously be detected, but we would not want to start protection. To cater for this, an *All Poles Dead* signal blocks the *Start* signal for each phase. This is controlled by the *V<Poledead Inh* cell, which is included for each of the stages. If the cell is enabled, the relevant stage will be blocked by the integrated pole dead logic. This logic produces an output when it detects either an open circuit breaker via auxiliary contacts feeding the opto-inputs or it detects a combination of both undercurrent and undervoltage on any one phase.

2.3 APPLICATION NOTES

2.3.1 UNDERVOLTAGE SETTING GUIDELINES

In most applications, undervoltage protection is not required to operate during system earth fault conditions. If this is the case you should select phase-to-phase voltage measurement, as this quantity is less affected by single-phase voltage dips due to earth faults.

The voltage threshold setting for the undervoltage protection should be set at some value below the voltage excursions that may be expected under normal system operating conditions. This threshold is dependent on the system in question but typical healthy system voltage excursions may be in the order of 10% of nominal value.

The same applies to the time setting. The required time delay is dependent on the time for which the system is able to withstand a reduced voltage.

If motor loads are connected, then a typical time setting may be in the order of 0.5 seconds.

3 OVERVOLTAGE PROTECTION

Overvoltage conditions are generally related to loss of load conditions, whereby the supply voltage increases in magnitude. This situation would normally be rectified by voltage regulating equipment such as AVRs (Auto Voltage Regulators) or On Load Tap Changers. However, failure of this equipment to bring the system voltage back within permitted limits leaves the system with an overvoltage condition which must be cleared.

Note:

During earth fault conditions on a power system there may be an increase in the healthy phase voltages. Ideally, the system should be designed to withstand such overvoltages for a defined period of time.

3.1 OVERVOLTAGE PROTECTION IMPLEMENTATION

Overvoltage Protection is implemented in the *VOLT PROTECTION* column of the relevant settings group. The Overvoltage parameters are contained within the sub-heading *OVERVOLTAGE*.

The product provides two stages of overvoltage protection with independent time delay characteristics.

Stage 1 provides a choice of operate characteristics, where you can select between:

- An IDMT characteristic
- DT (Definite Time)

You set this using the **V>1 Function** setting.

The IDMT characteristic is defined by the following formula:

$$t = K/(M-1)$$

where:

- K = Time multiplier setting
- t = Operating time in seconds
- M = Measured voltage setting voltage (V>(n) Voltage Set)

The overvoltage stages can be configured either as phase-to-neutral or phase-to-phase voltages in the *V> Measur't Mode* cell.

There is no Timer Hold facility for Overvoltage.

Stages 2, 3 and 4 can have definite time characteristics only. This is set, for example, in the *V>2 Status* cell.

Outputs are available for single or three-phase conditions via the *V> Operate Mode* cell for each stage.

V> Measur't Mode V>1 Start A/AB VAB V>1 Trip A/AB V>1 Voltage Set V>1 Time Delay V> Measur't Mode V>1 Start B/B C VBC V>1 Trip B/BC V>1 Voltage Set V>1 Time Delay V> Measur't Mode V>1 Start C/CA VC -VCA V>1 Trip C/CA V>1 Voltage Set V>1 Time Delay V>1 Start V>1 Timer Block V>1 Trip V> Operate mode Any Phase Three Phase Notes: This diagram does not show all stages. Other stages follow similar principles VTS Fast Block only applies for directional models V00804

3.2 OVERVOLTAGE PROTECTION LOGIC

Figure 121: Overvoltage - single and three phase tripping mode (single stage)

The Overvoltage protection function detects when the voltage magnitude for a certain stage exceeds a set threshold. If this happens a **Start** signal, signifying the "Start of protection", is produced. This Start signal can be blocked by the **VTS Fast Block** signal. This start signal is applied to the timer module to produce the **Trip** signal, which can be blocked by the overvoltage timer block signal (**V>(n) Timer Block**). For each stage, there are three Phase overvoltage detection modules, one for each phase. The three **Start** signals from each of these phases are OR'd together to create a 3-phase Start signal (**V>(n) Start**), which can then be activated when any of the three phases start (Any Phase), or when all three phases start (Three Phase), depending on the chosen **V> Operate Mode** setting.

The outputs of the timer modules are the trip signals which are used to drive the tripping output relay. These tripping signals are also OR'd together to create a 3-phase Trip signal, which are also controlled by the **V> Operate Mode** setting.

If any one of the above signals is low, or goes low before the timer has counted out, the timer module is inhibited (effectively reset) until the blocking signal goes high.

3.3 APPLICATION NOTES

3.3.1 OVERVOLTAGE SETTING GUIDELINES

The provision of multiple stages and their respective operating characteristics allows for a number of possible applications:

- Definite Time can be used for both stages to provide the required alarm and trip stages.
- Use of the IDMT characteristic allows grading of the time delay according to the severity of the overvoltage. As the voltage settings for both of the stages are independent, the second stage could then be set lower than the first to provide a time-delayed alarm stage.
- If only one stage of overvoltage protection is required, or if the element is required to provide an alarm only, the remaining stage may be disabled.

This type of protection must be co-ordinated with any other overvoltage devices at other locations on the system.

4 RATE OF CHANGE OF VOLTAGE PROTECTION

Where there are very large loads, imbalances may occur, which could result in rapid decline in system voltage. The situation could be so bad that shedding one or two stages of load would be unlikely to stop this rapid voltage decline. In such a situation, standard undervoltage protection will normally have to be supplemented with protection that responds to the rate of change of voltage. An element is therefore required, which identifies the high rate of decline of voltage and adapts the load shedding scheme accordingly.

Such protection can identify voltage variations occurring close to nominal voltage thereby providing early warning of a developing voltage problem. The element can also be used as an alarm to warn operators of unusually high system voltage variations.

Rate of Change of Voltage protection is also known as dv/dt protection.

4.1 RATE OF CHANGE OF VOLTAGE PROTECTION IMPLEMENTATION

The dV/dt protection functions can be found in the the *VOLT PROTECTION* column under the sub-heading DV/DT *PROTECTION*. The dv/dt protection consists of two independent stages, which can be configured as either *phase-to-phase* or *phase-to-neutral* using the *dv/dt Meas mode* cell.

4.2 RATE OF CHANGE OF VOLTAGE LOGIC

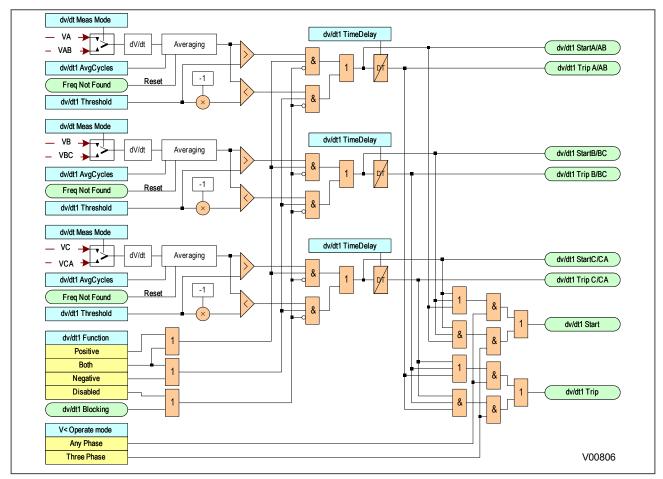


Figure 122: Rate of Change of Voltage protection logic

The dv/dt logic works by differentiating the RMS value of each phase voltage input, which can be with respect to neutral, or respect to another phase depending on the selected measurement mode. This differentiated value is then averaged over a number of cycles, determined by the setting *dv/dt1 AvgCycles* and comparing this with a

threshold (*dv/dt1 Threshold*) in both the positive and negative directions. A start signal is produced depending on the selected direction (positive, negative or both), set by the setting *dv/dt1 Function*, which can also disable the function on a per stage basis. Each stage can also be blocked by the DDB signal *dv/dt1 Blocking*. The trip signal is produced by passing the Start signal through a DT timer.

The function also produces three-phase Start and Trip signals, which can be set to Any Phase (where any of the phases can trigger the start) or Three Phase (where all three phases are required to trigger the start). The averaging buffer is reset either when the stage is disabled or no frequency is found (*Freq Not Found* DDB signal).

5 RESIDUAL OVERVOLTAGE PROTECTION

On a healthy three-phase power system, the sum of the three-phase to earth voltages is nominally zero, as it is the vector sum of three balanced vectors displaced from each other by 120°. However, when an earth fault occurs on the primary system, this balance is upset and a residual voltage is produced. This condition causes a rise in the neutral voltage with respect to earth. Consequently this type of protection is also commonly referred to as 'Neutral Voltage Displacement' or NVD for short.

This residual voltage may be derived (from the phase voltages) or measured (from a measurement class open delta VT). Derived values will normally only be used where the model does not support measured functionality (a dedicated measurement class VT). If a measurement class VT is used to produce a measured Residual Voltage, it cannot be used for other features such as Check Synchronisation.

This offers an alternative means of earth fault detection, which does not require any measurement of current. This may be particularly advantageous in high impedance earthed or insulated systems, where the provision of core balanced current transformers on each feeder may be either impractical, or uneconomic, or for providing earth fault protection for devices with no current transformers.

5.1 RESIDUAL OVERVOLTAGE PROTECTION IMPLEMENTATION

Residual Overvoltage Protection is implemented in the RESIDUAL O/V NVD column of the relevant settings group.

Some applications require more than one stage. For example an insulated system may require an alarm stage and a trip stage. It is common in such a case for the system to be designed to withstand the associated healthy phase overvoltages for a number of hours following an earth fault. In such applications, an alarm is generated soon after the condition is detected, which serves to indicate the presence of an earth fault on the system. This gives time for system operators to locate and isolate the fault. The second stage of the protection can issue a trip signal if the fault condition persists.

The product provides two stages of Residual Overvoltage protection with independent time delay characteristics.

Stage 1 provides a choice of operate characteristics, where you can select between:

- An IDMT characteristic
- DT (Definite Time)

The IDMT characteristic is defined by the following formula:

$$t = K/(M - 1)$$

where:

- K= Time multiplier setting
- t = Operating time in seconds
- M = Derived residual voltage setting voltage (VN> Voltage Set)

You set this using the **VN>1 Function** setting.

Stage 1 also provides a Timer Hold facility.

Stages 2, 3 and 4 can have definite time characteristics only. This is set, for example, in the VN>2 status cell.

The device derives the residual voltage internally from the three-phase voltage inputs supplied from either a 5-limb VT or three single-phase VTs. These types of VT design provide a path for the residual flux and consequently permit the device to derive the required residual voltage. In addition, the primary star point of the VT must be earthed. Three-limb VTs have no path for residual flux and are therefore unsuitable for this type of protection.

5.2 RESIDUAL OVERVOLTAGE LOGIC

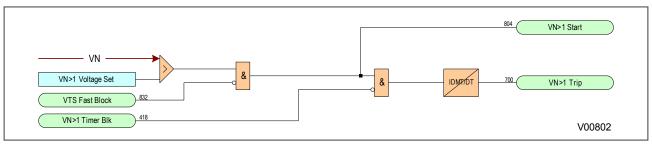


Figure 123: Residual Overvoltage logic

The Residual Overvoltage module (VN>) is a level detector that detects when the voltage magnitude exceeds a set threshold, for each stage. When this happens, the comparator output produces a *Start* signal (*VN>(n) Start*), which signifies the "Start of protection". This can be blocked by a *VTS Fast block* signal. This *Start* signal is applied to the timer module. The output of the timer module is the *VN> (n) Trip* signal which is used to drive the tripping output relay.

5.3 APPLICATION NOTES

5.3.1 CALCULATION FOR SOLIDLY EARTHED SYSTEMS

Consider a Phase-A to Earth fault on a simple radial system.

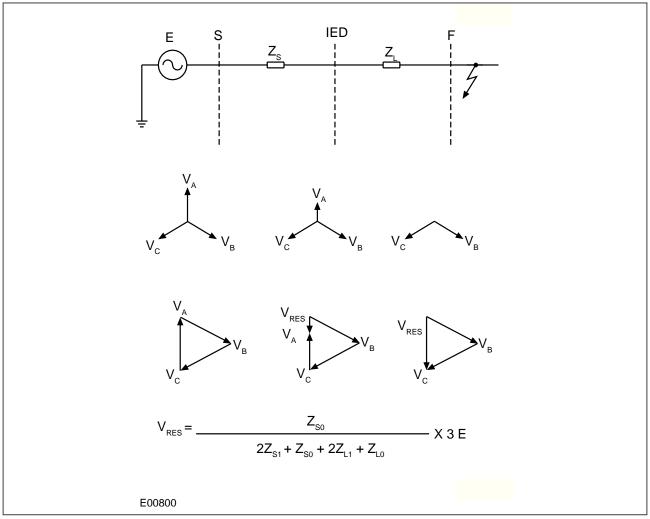


Figure 124: Residual voltage for a solidly earthed system

As can be seen from the above diagram, the residual voltage measured on a solidly earthed system is solely dependent on the ratio of source impedance behind the protection to the line impedance in front of the protection, up to the point of fault. For a remote fault far away, the Z_S/Z_L : ratio will be small, resulting in a correspondingly small residual voltage. Therefore, the protection only operates for faults up to a certain distance along the system. The maximum distance depends on the device setting.

5.3.2 CALCULATION FOR IMPEDANCE EARTHED SYSTEMS

Consider a Phase-A to Earth fault on a simple radial system.

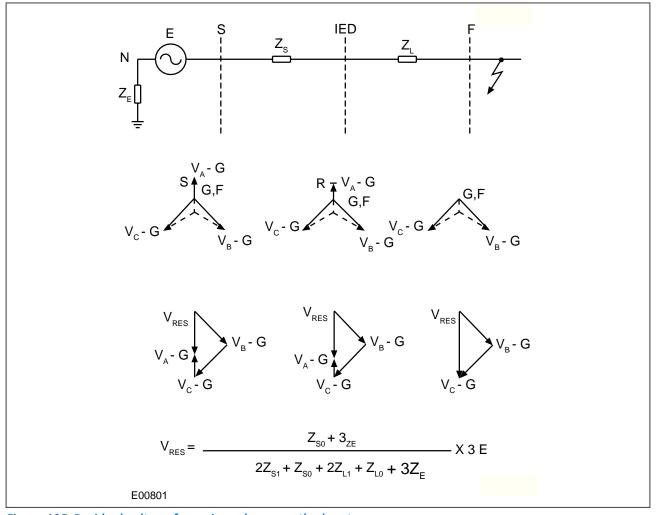


Figure 125: Residual voltage for an impedance earthed system

An impedance earthed system will always generate a relatively large degree of residual voltage, as the zero sequence source impedance now includes the earthing impedance. It follows then that the residual voltage generated by an earth fault on an insulated system will be the highest possible value (3 x phase-neutral voltage), as the zero sequence source impedance is infinite.

5.3.3 NEUTRAL VOLTAGE DISPLACEMENT (NVD) PROTECTION APPLIED TO CONDENSER BUSHINGS (CAPACITOR CONES)

Voltage Transformers are not fitted at distribution levels, due to their expense. Instead, capacitor cones, or condenser bushings, may be used at 11kV and 33kV substations to provide a neutral voltage displacement output to a suitable protection device.

Often, bushings are starred together, and the star point used to provide the displacement voltage to the device, as seen in the diagram, below.



Warning:

As protection method requires the device to be placed in a primary circuit location, all relevant safety measures must be in place.



Warning:

When operating in areas with restricted space, suitable protective barriers must be used where there is a risk of electric shock due to exposed terminals.

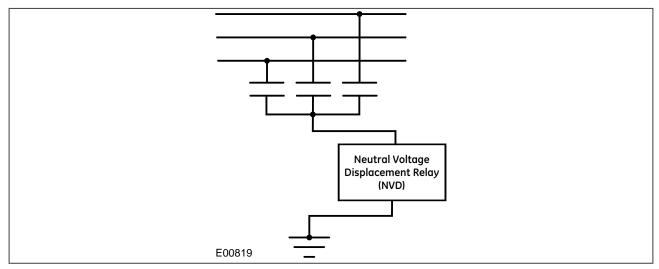


Figure 126: Star connected condenser bushings

Calculations for Condenser Bushing Systems

Consider a single-phase fault to ground on B-Phase:

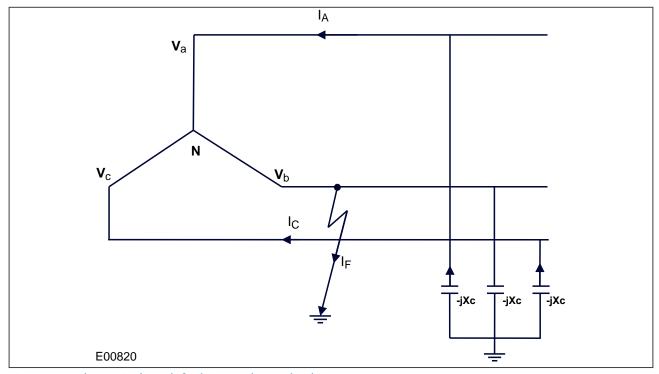


Figure 127: Theoretical earth fault in condenser bushing system

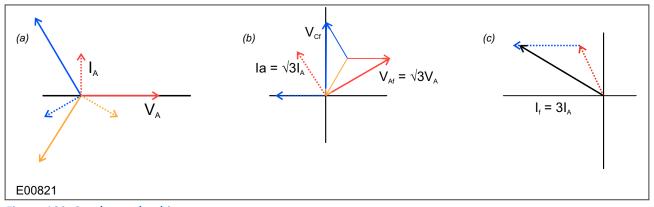


Figure 128: Condenser bushing system vectors

In the figure above:

(a) Shows three healthy voltages, three capacitor currents that lead their respective voltages by 90° and sum to zero,

(b) Shows B phase earthed, A and C voltages are $\sqrt{3}$ times their healthy magnitude & at 60° to each other, giving correspondingly altered capacitor currents Ia and Ic.

The vector sum of the A & C phase capacitor currents is:

$$I_f = \sqrt{3} \times I_{a}$$

$$= \sqrt{3} \times \sqrt{3} \times I_A$$

$$= 3 \times I_A$$

Therefore, the total fault current I_f equals three times a single capacitor healthy condition current I_A .

(c) Shows the vector sum of the fault condition I_f .

Therefore, I_f is the current which will flow in the Neutral Displacement Relay under fault conditions (neglecting the impedance of the relay itself).

For example, for a 60pF capacitor on a 33kV system, the single capacitor healthy condition current I_A is given by:

$$I_A = V_A / X_C$$

 $= V_A / (1/2\pi fC)$

=
$$\frac{33 \times 10^3}{\sqrt{3}}$$
 / (1/(2 × π × 50 × 60 × 10⁻¹²)) $\sqrt{3}$

= 0.359 mA

Therefore, the total fault current which would flow in an NVD relay (neglecting the impedance of the relay itself):

$$I_f = 3 \times 0.359 = 1.08 \text{mA}$$

The table below shows the total fault current I_f for a 60pF capacitor, and also I_f for a 90pF capacitor, and for a 150pF capacitor.

C (pF)	60.00	90.00	150.00
Χc (ΜΩ)	53.08	35.39	21.23
VA (kV)	19.00	19.00	19.00
IA (mA)	0.359	0.539	0.898
If (mA)	1.08	1.62	2.69

Where If is the total fault current which would flow in an NVD relay (neglecting the impedance of the relay itself), then knowing this current (If) and the input impedance of the relay (Rr) we can calculate the voltage produced across it (Vr) during a fault condition:

 $Vr = If \times Rr$

Therefore, we would recommend setting the relay to less than half this voltage:

Vs < Vr/2

Practical Application

In practice, the device's input impedance varies with voltage, which will have some effect on actual settings. Therefore, we recommend the use a $23\frac{1}{2}k\Omega$ resistor combination in parallel with this input, to fix the impedance. This value is achieved by the use of two $47k\Omega$ resistors in parallel. Utilising two resistors in parallel also gives increased security.

The resistors used must have a continuous working voltage rating of 5kVdc minimum and a minimum power rating of 1W.



Warning:

There is the risk of high voltage developing on removal of the device or PCB from its case. Fixed resistors on the device input will prevent this, but we would also recommend use of an externally connected shorting contact.

Note

A suitable shorting contact is available on each device. Please see diagram, below.

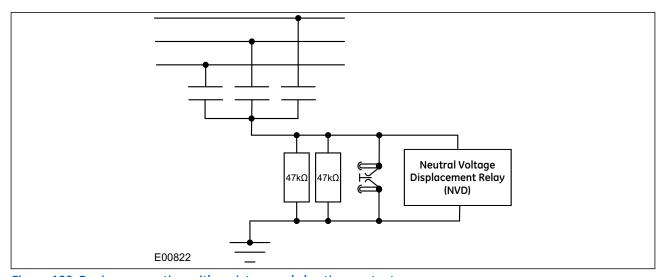


Figure 129: Device connection with resistors and shorting contact

Voltage Setting (P141, P142, P143, P145)

The device has a minimum setting on the residual OV/NVD of 1V, which should provide a sensitive enough setting for most applications. The operating voltage to be applied can be calculated for various capacitor ratings, shown in calculations provided above.

For maximum settings for various capacitors (assuming 23½ $k\Omega$ resistance applied in conjunction with the device), see the table below.

C (pF)	60.00	90.00	150.00
Xc (MΩ)	53.08	35.39	21.23
VA (kV)	19.00	19.00	19.00
If (mA)	1.08	1.62	2.69
Rr (kΩ)*	22.00	22.00	22.00
Vr (V)	23.63	35.44	59.06
Vs (V)	11.81	17.72	29.53

^{*}Relay and Resistor Combination

Voltage Setting (P144)

The device has a minimum setting on the residual OV/NVD of 4V, which should provide a sensitive enough setting for most applications. The operating voltage to be applied can be calculated for various capacitor ratings, shown in calculations provided above.

For maximum settings for various capacitors (assuming 23½ $k\Omega$ resistance applied in conjunction with the device), see the table below.

C (pF)	60.00	90.00	150.00
Χc (ΜΩ)	53.08	35.39	21.23
VA (kV)	19.00	19.00	19.00
If (mA)	1.08	1.62	2.69
Rr (kΩ)*	22.00	22.00	22.00
Vr (V)	23.63	35.44	59.06
Vs (V)	11.81	17.72	29.53

^{*}Relay and Resistor Combination

Wiring Diagram (P141, P142, P143, P145)

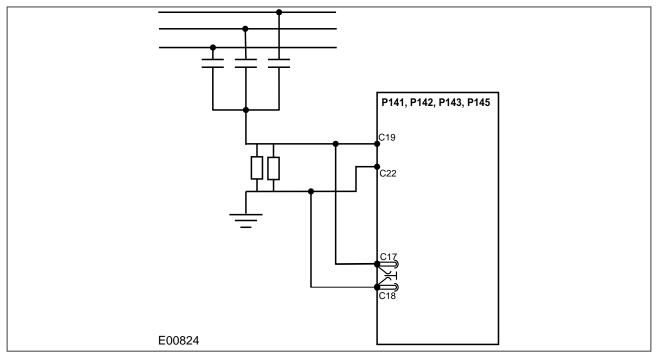


Figure 130: Device connection P141/ P142/ P143/ P145

Note

Residual voltage measurement is derived from phase inputs, but neutral voltage may be connected into one of the phase inputs. This assumes that voltage inputs are not used for other purposes

Wiring Diagram (P144)

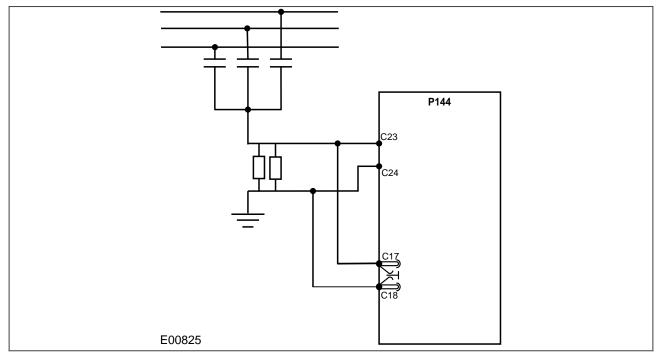


Figure 131: Device connection P144

5.3.4 SETTING GUIDELINES

The voltage setting applied to the elements is dependent on the magnitude of residual voltage that is expected to occur during the earth fault condition. This in turn is dependent on the method of system earthing employed.

Also, you must ensure that the protection setting is set above any standing level of residual voltage that is present on the system.

6 NEGATIVE SEQUENCE OVERVOLTAGE PROTECTION

Where an incoming feeder is supplying rotating plant equipment such as an induction motor, correct phasing and balance of the supply is essential. Incorrect phase rotation will result in connected motors rotating in the wrong direction. For directionally sensitive applications, such as elevators and conveyor belts, it is unacceptable to allow this to happen.

Imbalances on the incoming supply cause negative phase sequence voltage components. In the event of incorrect phase rotation, the supply voltage would effectively consist of 100% negative phase sequence voltage only.

6.1 NEGATIVE SEQUENCE OVERVOLTAGE IMPLEMENTATION

Negative Sequence Overvoltage Protection is implemented in the *NEG SEQUENCE O/V* column of the relevant settings group.

The device includes one Negative Phase Sequence Overvoltage element with a single stage. Only Definite time is possible.

This element monitors the input voltage rotation and magnitude (normally from a bus connected voltage transformer) and may be interlocked with the motor contactor or circuit breaker to prevent the motor from being energised whilst incorrect phase rotation exists.

The element is enabled using the *V2> status* cell.

6.2 NEGATIVE SEQUENCE OVERVOLTAGE LOGIC

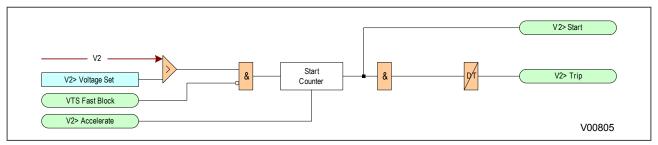


Figure 132: Negative Sequence Overvoltage logic

The Negative Voltage Sequence Overvoltage module (*V2>*) is a level detector that detects when the voltage magnitude exceeds a set threshold. When this happens, the comparator output Overvoltage Module produces a *Start* signal (*V2> Start*), which signifies the "Start of protection". This can be blocked by a *VTS Fast block* signal. This *Start* signal is applied to the DT timer module. The output of the DT timer module is the *V2> Trip* signal which is used to drive the tripping output relay.

The *V2> Accelerate* signal accelerates the operating time of the function, by reducing the number of confirmation cycles needed to start the function. At 50 Hz, this means the protection Start is reduced by 20 ms.

6.3 APPLICATION NOTES

6.3.1 SETTING GUIDELINES

The primary concern is usually the detection of incorrect phase rotation (rather than small imbalances), therefore a sensitive setting is not required. The setting must be higher than any standing NPS voltage, which may be present due to imbalances in the measuring VT, device tolerances etc.

A setting of approximately 15% of rated voltage may be typical.

Note:

Standing levels of NPS voltage (V2) are displayed in the **V2 Magnitude** cell of the MEASUREMENTS 1 column.

The operation time of the element depends on the application, but a typical setting would be in the region of 5 seconds.

7 SENSITIVE OVERVOLTAGE SUPERVISION

Software versions 52 and 61 introduce Sensitive Overvoltage Protection (SOV). The SOV function provides an extended range for the pickup setting (from 2V to 185V). The unique characteristic in SOV function extends the relay's capability to mimic the buswire supervision function in a high impedance busbar protection scheme. P14x relay can detect open circuit scenarios in buswire by using the sensitive overvoltage function. This enables the P14x relay to provide cost & space efficient one box solution for both high impedance busbar protection and buswire supervision.

7.1 SENSITIVE OVERVOLTAGE IMPLEMENTATION

The device provides two stages of Sensitive Overvoltage Supervision; SOV>1 and SOV>2. Two measurement modes are available; phase-to-phase or phase-to-neutral. You choose the measurement mode with the **SOV Meas't Mode** setting. Two operation modes are also available; any phase, or three-phase. You choose the operating mode with the **SOV Operate Mode** setting. This setting determines whether any one of the phases or all three of the phases have to satisfy the overvoltage criteria before a decision is made.

Both of these settings are global for both stages and cannot be applied individually to each stage.

Each stage can be enabled or disabled individually with the *SOV>1 Status* and *SOV>2 Status* settings. The pickup threshold voltage for each stage can be set using, *SOV>1 Volt Set* and *SOV>2 Volt Set* settings respectively. A DT time delay for each stage can also be set with the *SOV>1 Time Delay* and *SOV>2 Time Delay* settings.

7.1.1 SENSITIVE OVERVOLTAGE FILTER MODE

The SOV function also has **SOV Filter Mod**. When the **SOV Filter Mod** is enabled, the SOV protection provides adaptive pickup responding to the frequency of the voltage input. In the **SOV Filter Mod**, the SOV function is tuned to operate sensitively on nominal frequency, but adapt the pickup level to higher when the frequency is outside nominal range.

Note:

The SOV function in **SOV Filter Mod** has a pickup setting range from 10V to 185V, this will respond to the relay's frequency tracking range (40Hz to 70Hz). SOV protection in **SOV Filter Mod** will be blocked if the frequency of the voltage input is outside the frequency tracking range.

It is possible to enable a band pass frequency characteristic for this function using the **SOV Filter Mod** setting. If you set this to <code>Disabled</code>, the normal mode is chosen, which is no different from previous models. If you select <code>Enabled</code>, however, this allows you to set the rate of operation voltage for various proportions of the system frequency. You can set this individually from 0.8 times system frequency through to 1.2 times system frequency, with the setting cells under the <code>SOV OPERA CURVE</code> sub heading.

7.2 SENSITIVE OVERVOLTAGE LOGIC

7.2.1 SENSITIVE OVERVOLTAGE OPERATION LOGIC

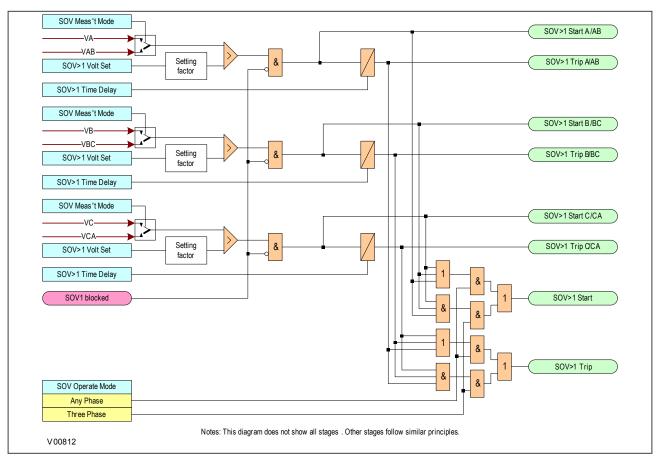


Figure 133: Sensitive Overvoltage operation logic

7.2.2 SENSITIVE OVERVOLTAGE FILTER MODE LOGIC

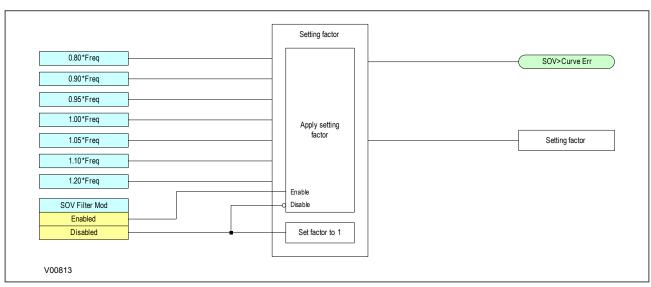


Figure 134: Sensitive Overvoltage filter mode logic

7.2.3 SENSITIVE OVERVOLTAGE BLOCKING LOGIC

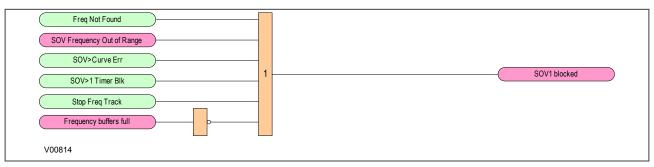


Figure 135: Sensitive Overvoltage blocking logic

CHAPTER 11

FREQUENCY PROTECTION FUNCTIONS

1 CHAPTER OVERVIEW

The device provides a range of frequency protection functions. This chapter describes the operation of these functions including the principles, logic diagrams and applications.

This chapter contains the following sections:

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Overfrequency Protection	248
Independent R.O.C.O.F Protection	250
Frequency-supervised R.O.C.O.F Protection	252
Average Rate of Change of Frequency Protection	255
Load Shedding and Restoration	258

2 FREQUENCY PROTECTION OVERVIEW

Power generation and utilisation needs to be well balanced in any industrial, distribution or transmission network. These electrical networks are dynamic entities, with continually varying loads and supplies, which are continually affecting the system frequency. Increased loading reduces the system frequency and generation needs to be increased to maintain the frequency of the supply. Conversely decreased loading increases the system frequency and generation needs to be reduced. Sudden fluctuations in load can cause rapid changes in frequency, which need to be dealt with quickly.

Unless corrective measures are taken at the appropriate time, frequency decay can go beyond the point of no return and cause widespread network collapse, which has dire consequences.

Protection devices capable of detecting low frequency conditions are generally used to disconnect unimportant loads in order to re-establish the generation-to-load balance. However, with such devices, the action is initiated only after the event and this form of corrective action may not be effective enough to cope with sudden load increases that cause large frequency decays in very short times. In such cases a device that can anticipate the severity of frequency decay and act to disconnect loads before the frequency reaches dangerously low levels, are very effective in containing damage. This is called instantaneous rate of change of frequency protection (ROCOF).

During severe disturbances, the frequency of the system oscillates as various generators try to synchronise to a common frequency. The measurement of instantaneous rate of change of frequency can be misleading during such a disturbance. The frequency decay needs to be monitored over a longer period of time to make the correct decision for load shedding. This is called average rate of change of frequency protection.

Normally, generators are rated for a particular band of frequency. Operation outside this band can cause mechanical damage to the turbine blades. Protection against such contingencies is required when frequency does not improve even after load shedding steps have been taken. This type of protection can be used for operator alarms or turbine trips in case of severe frequency decay.

2.1 FREQUENCY PROTECTION IMPLEMENTATION

Earlier versions of the product provided just four stages of underfrequency protection and two stages of overfrequency protection. The present version of the product provides an additional advanced version of frequency protection consisting of 9 stages each of the following protection functions:

- Underfrequency Protection: abbreviated to f+t<
- Overfrequency Protection: abbreviated to f+t>
- Independent Rate of Change of Frequency Protection: abbreviated to Independent R.O.C.O.F, or df/dt+t
- Frequency-supervised Rate of Change of Frequency Protection: abbreviated to Frequency-supervised R.O.C.O.F, or f+df/dt
- Average Rate of Change of Frequency Protection: abbreviated to Average R.O.C.O.F, or f+Df/Dt (note the uppercase 'D')
- Load Shedding and Restoration

The basic version of frequency protection is implemented in the *FREQ PROTECTION* column of the relevant settings group. The advanced version of frequency protection is implemented in the *ADV. FREQ PROT'N* column of the relevant settings group.

If you require only four stages of underfrequency protection and two stages of overfrequency protection, you can still use the basic version of frequency protection, however we recommend using the advanced version in all cases.

If using basic frequency protection you must enable it and disable the advanced frequency protection. If using advanced frequency protection, you must enable it and disable the basic frequency protection. You do this by setting the *Freq Protection* and the *Adv. Freq Prot'n* settings in the *CONFIGURATION* column to *enabled* or *disabled* accordingly.

With basic frequency protection you can enable or disable each stage of underfrequency and overfrequency protection separately with the settings *F<1 Status*, *F<2 Status*, *F<3 Status*, *F<4 Status*, *F>1 Status*, *F>2 Status*.

With advanced frequency protection you can enable or disable all frequency protections for each stage with the *Stage (n)* setting. The frequency protection can also be blocked by an undervoltage condition if required.

3 UNDERFREQUENCY PROTECTION

A reduced system frequency implies that the net load is in excess of the available generation. Such a condition can arise, when an interconnected system splits, and the load left connected to one of the subsystems is in excess of the capacity of the generators in that particular subsystem. Industrial plants that are dependent on utilities to supply part of their loads will experience underfrequency conditions when the incoming lines are lost.

Many types of industrial loads have limited tolerances on the operating frequency and running speeds (e.g. synchronous motors). Sustained underfrequency has implications on the stability of the system, whereby any subsequent disturbance may damage equipment and even lead to blackouts. It is therefore essential to provide protection for underfrequency conditions.

3.1 UNDERFREQUENCY PROTECTION IMPLEMENTATION

The following settings are relevant for underfrequency:

- Stg (n) f+t Status: determines whether the stage is underfrequency, overfrequency, or disabled
- Stg (n) f+t Freq: defines the frequency pickup setting
- Stg (n) f+t Time: sets the time delay

Note:

This section refers to advanced frequency protection. The basic frequency protection works in a similar manner, but the setting names and DDB signal names are different.

3.2 UNDERFREQUENCY PROTECTION LOGIC

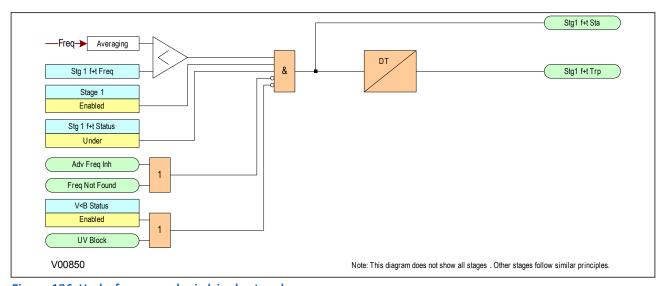


Figure 136: Underfrequency logic (single stage)

If the frequency is below the setting and not blocked the DT timer is started. If the frequency cannot be determined, the function is blocked.

Note

This section refers to advanced frequency protection. The basic frequency protection works in a similar manner, but the setting names and DDB signal names are different.

3.3 APPLICATION NOTES

3.3.1 SETTING GUIDELINES

In order to minimise the effects of underfrequency, a multi-stage load shedding scheme may be used with the plant loads prioritised and grouped. During an underfrequency condition, the load groups are disconnected sequentially, with the highest priority group being the last one to be disconnected.

The effectiveness of each load shedding stage depends on the proportion of power deficiency it represents. If the load shedding stage is too small compared with the prevailing generation deficiency, then there may be no improvement in the frequency. This should be taken into account when forming the load groups.

Time delays should be sufficient to override any transient dips in frequency, as well as to provide time for the frequency controls in the system to respond. These should not be excessive as this could jeopardize system stability. Time delay settings of 5 - 20 s are typical.

An example of a four-stage load shedding scheme for 50 Hz systems is shown below:

Stage	Element	Frequency Setting (Hz)	Time Setting (Sec)
1	Stage 1(f+t)	49.0	20 s
2	Stage 2(f+t)	48.6	20 s
3	Stage 3(f+t)	48.2	10 s
4	Stage 4(f+t)	47.8	10 s

The relatively long time delays are intended to provide sufficient time for the system controls to respond. This will work well in a situation where the decline of system frequency is slow. For situations where rapid decline of frequency is expected, this load shedding scheme should be supplemented by rate of change of frequency protection elements.

Note:

This section refers to advanced frequency protection. The basic frequency protection works in a similar manner, but the setting names and DDB signal names are different.

4 OVERFREQUENCY PROTECTION

An increased system frequency arises when the mechanical power input to a generator exceeds the electrical power output. This could happen, for instance, when there is a sudden loss of load due to tripping of an outgoing feeder from the plant to a load centre. Under such conditions, the governor would normally respond quickly to obtain a balance between the mechanical input and electrical output, thereby restoring normal frequency. Overfrequency protection is required as a backup to cater for cases where the reaction of the control equipment is too slow.

4.1 OVERFREQUENCY PROTECTION IMPLEMENTATION

The following settings are relevant for overfrequency:

- Stg (n) f+t Status: determines whether the stage is underfrequency, overfrequency, or disabled
- Stg (n) f+t Freq: defines the frequency pickup setting
- Stg (n) f+t Time: sets the time delay

Note

This section refers to advanced frequency protection. The basic frequency protection works in a similar manner, but the setting names and DDB signal names are different.

4.2 OVERFREQUENCY PROTECTION LOGIC

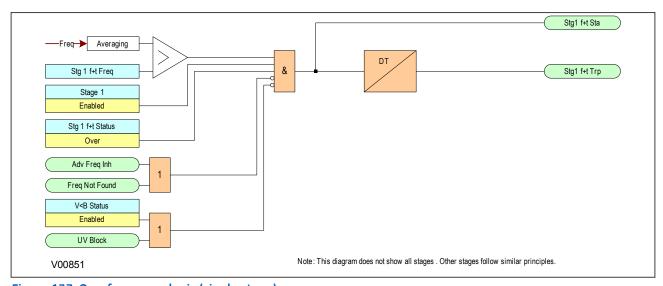


Figure 137: Overfrequency logic (single stage)

If the frequency is above the setting and not blocked, the DT timer is started and after this has timed out, the trip is produced. If the frequency cannot be determined, the function is blocked.

Note:

This section refers to advanced frequency protection. The basic frequency protection works in a similar manner, but the setting names and DDB signal names are different.

4.3 APPLICATION NOTES

4.3.1 SETTING GUIDELINES

Following changes on the network caused by faults or other operational requirements, it is possible that various subsystems will be formed within the power network. It is likely that these subsystems will suffer from a generation/load imbalance. The "islands" where generation exceeds the existing load will be subject to overfrequency conditions. Severe over frequency conditions may be unacceptable to many industrial loads, since running speeds of motors will be affected. The overfrequency element can be suitably set to sense this contingency.

An example of two-stage overfrequency protection is shown below using stages 5 and 6 of the f+t elements. However, settings for a real system will depend on the maximum frequency that equipment can tolerate for a given period of time.

Stage	Element	Frequency Setting (Hz)	Time Setting (Sec.)
1	Stage 5(f+t)	50.5	30
2	Stage 6(f+t)	51.0	20

The relatively long time delays are intended to provide time for the system controls to respond and will work well in a situation where the increase of system frequency is slow.

For situations where rapid increase of frequency is expected, the protection scheme above could be supplemented by rate of change of frequency protection elements.

In the system shown below, the generation in the MV bus is sized according to the loads on that bus, whereas the generators linked to the HV bus produce energy for export to utility. If the links to the grid are lost, the generation will cause the system frequency to rise. This rate of rise could be used to isolate the MV bus from the HV system.

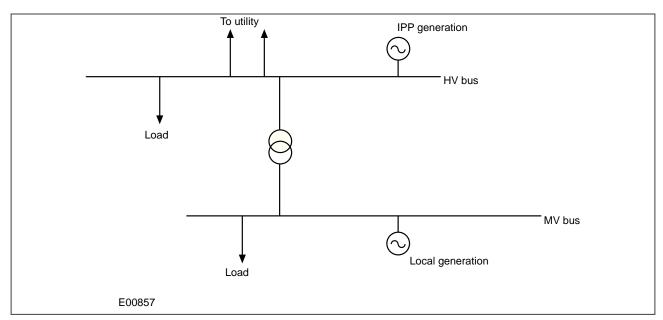


Figure 138: Power system segregation based upon frequency measurements

Note

This section refers to advanced frequency protection. The basic frequency protection works in a similar manner, but the setting names and DDB signal names are different.

5 INDEPENDENT R.O.C.O.F PROTECTION

Where there are very large loads, imbalances may occur that result in rapid decline in system frequency. The situation could be so bad that shedding one or two stages of load is unlikely to stop this rapid frequency decline. In such a situation, standard underfrequency protection will normally have to be supplemented with protection that responds to the rate of change of frequency. An element is therefore required which identifies the high rate of decline of frequency, and adapts the load shedding scheme accordingly.

Such protection can identify frequency variations occurring close to nominal frequency thereby providing early warning of a developing frequency problem. The element can also be used as an alarm to warn operators of unusually high system frequency variations.

5.1 INDEPENENT R.O.C.O.F PROTECTION IMPLEMENTATION

The device provides nine independent stages of protection. Each stage can respond to either rising or falling frequency conditions. This depends on whether the frequency threshold is set above or below the system nominal frequency. For example, if the frequency threshold is set above nominal frequency, the rate of change of frequency setting is considered as positive and the element will operate for rising frequency conditions. If the frequency threshold is set below nominal frequency, the setting is considered as negative and the element will operate for falling frequency conditions.

The following settings are relevant for df/dt+t protection:

- df/dt+t (n) Status: determines whether the stage is for falling or rising frequency conditions
- df/dt+t (n) Set: defines the rate of change of frequency pickup setting
- df/dt+t (n) Time: sets the time delay

5.2 INDEPENDENT R.O.C.O.F PROTECTION LOGIC

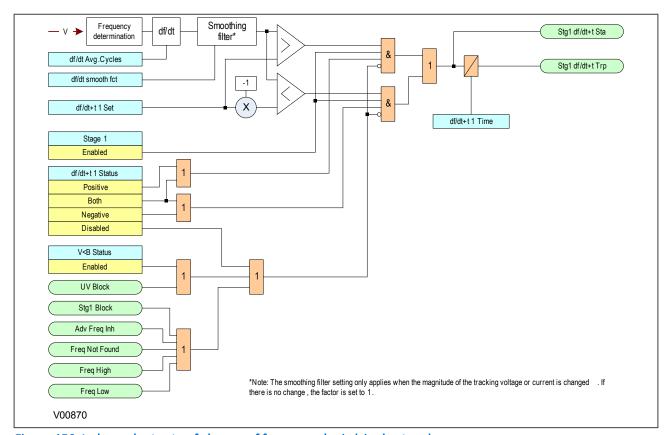


Figure 139: Independent rate of change of frequency logic (single stage)

5.3 APPLICATION NOTES

5.3.1 SETTING GUIDELINES

Considerable care should be taken when setting this element because it is not supervised by a frequency setting. Setting of the time delay or increasing the number of df/dt averaging cycles will improve stability but this is traded against reduced tripping times.

It is likely that this element would be used in conjunction with other frequency based protection elements to provide a scheme that accounts for severe frequency fluctuations. An example scheme is shown below:

	Frequency "f+t [81U/810]" Elements		Frequency Supervised Rate of Change of Frequency "f+df/dt [81RF]" Elements	
Stage	Frequency Setting (Hz)	Time Setting (Sec.)	Frequency Setting (Hz)	Rate of Change of Frequency Setting (Hz/ Sec.)
1	49	20	49.2	1.0
2	48.6	20	48.8	1.0
3	48.2	10	48.4	1.0
4	47.8	10	48.0	1.0
5	-	-	-	-

Stage	Rate of Change of Frequency "df/dt+t [81R]" Elements					
	Rate of Change of Frequency Setting (Hz/Sec.) Time Setting (Sec.)					
1	-	-				
2	-	-				
3	-3.0	0.5				
4	-3.0	0.5				
5	-3.0	0.1				

In this scheme, tripping of the last two stages is accelerated by using the independent rate of change of frequency element. If the frequency starts falling at a high rate (> 3 Hz/s in this example), then stages 3 & 4 are shed at around 48.5 Hz, with the objective of improving system stability. Stage 5 serves as an alarm and gives operators advance warning that the situation is critical.

6 FREQUENCY-SUPERVISED R.O.C.O.F PROTECTION

Frequency-supervised Rate of Change of Frequency protection works in a similar way to Independent Rate of change of Frequency Protection. The only difference is that with frequency supervision, the actual frequency itself is monitored and the protection operates when both the rate of change of frequency AND the frequency itself go outside the set limits.

Frequency-supervised Rate of Change of Frequency protection is also known as f+df/dt protection.

6.1 FREQUENCY-SUPERVISED R.O.C.O.F IMPLEMENTATION

The device provides nine independent stages of protection. Each stage can respond to either rising or falling frequency conditions. This depends on whether the frequency threshold is set above or below the system nominal frequency. For example, if the frequency threshold is set above nominal frequency, the rate of change of frequency setting is considered as positive and the element will operate for rising frequency conditions. If the frequency threshold is set below nominal frequency, the setting is considered as negative and the element will operate for falling frequency conditions.

The following settings are relevant for f+ df/dt protection:

- f+df/dt 1 Status: determines whether the stage is for falling or rising frequency conditions
- f+df/dt 1 freq: defines the frequency pickup setting
- f+df/dt 1 df/dt: defines the rate of change of frequency pickup setting

The device will also indicate when an incorrect setting has been applied if the frequency threshold is set to the nominal system frequency. There is no intentional time delay associated with this element, but time delays could be applied using the PSL if required.

Frequency determination df/dt Stg 1 df/dt+t Trp df/dt Avg.Cycles f+df/dt 1 df/dt & Frequency Frequency determination averaging Freq Avg.Cycles f+df/dt 1 freq Stage 1 Enabled f+df/dt 1 Status Positive Both Negative Disabled V<B Status Enabled UV Block Stg1 Block Adv Freq Inh Freq Not Found Freq High Freq Low V00853 Note: This diagram does not show all stages . Other stages follow similar principles.

6.2 FREQUENCY-SUPERVISED R.O.C.O.F LOGIC

Figure 140: Frequency-supervised rate of change of frequency logic (single stage)

6.3 APPLICATION NOTES

6.3.1 FREQUENCY-SUPERVISED R.O.C.O.F EXAMPLE

In the load shedding scheme below, we assume that for falling frequency conditions, the system can be stabilised at frequency f2 by shedding a stage of load. For slow rates of decay, this can be achieved using the underfrequency protection element set at frequency f1 with a suitable time delay. However, if the generation deficit is substantial, the frequency will rapidly decrease and it is possible that the time delay imposed by the underfrequency protection will not allow for frequency stabilisation. In this case, the chance of system recovery will be enhanced by disconnecting the load stage based on a measurement of rate of change of frequency and bypassing the time delay.

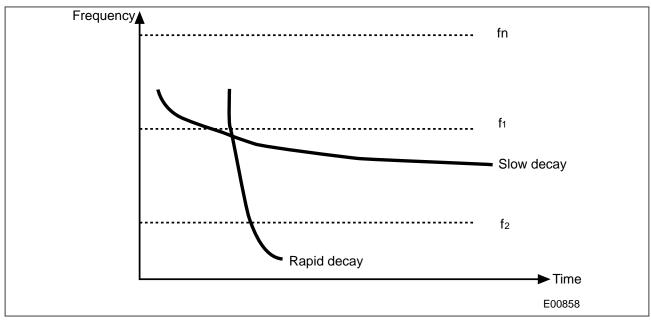


Figure 141: Frequency supervised rate of change of frequency protection

6.3.2 SETTING GUIDELINES

We recommend that the frequency supervised rate of change of frequency protection (f+df/dt) element be used in conjunction with the time delayed frequency protection (f+t) elements.

A four stage high speed load shedding scheme may be configured as indicated below, noting that in each stage, both the "f+t" and the "f+df/dt" elements are enabled.

	Frequency "f+t [81U/810]" Elements		Frequency Supervised Rate of Change of Frequency "f+df/dt [81RF]" Elements	
Stage	Frequency Setting (Hz)	Time Setting (Sec.)	Frequency Setting (Hz)	Rate of Change of Frequency Setting (Hz/sec.)
1	49	20	49	1.0
2	48.6	20	48.6	1.0
3	48.2	10	48.2	1.0
4	47.8	10	47.8	1.0

It may be possible to further improve the speed of load shedding by changing the frequency setting on the f+df/dt element. In the settings outlined below, the frequency settings for this element have been set slightly higher than the frequency settings for the f+t element. This difference will allow for the measuring time, and will result in the tripping of the two elements at approximately the same frequency value. Therefore, the slow frequency decline and fast frequency decline scenarios are independently monitored and optimised without sacrificing system security.

	Frequency "f+t [81U/810]" Elements		Frequency Supervised Rate of Change of Frequency "f+df/dt [81RF]" Elements	
Stage	Frequency Setting (Hz)	Time Setting (Sec.)	Frequency Setting (Hz)	Rate of Change of Frequency Setting (Hz/ sec.)
1	49	20	49.2	1.0
2	48.6	20	48.8	1.0
3	48.2	10	48.4	1.0
4	47.8	10	48.0	1.0

7 AVERAGE RATE OF CHANGE OF FREQUENCY PROTECTION

Owing to the complex dynamics of power systems, variations in frequency during times of generation-to-load imbalance are highly non-linear. Oscillations will occur as the system seeks to address the imbalance, resulting in frequency oscillations typically in the order of 0.1 Hz to 1 Hz, in addition to the basic change in frequency.

The independent and frequency-supervised rate of change of frequency elements use an instantaneous measurement of the rate of change of frequency, based on a 3-cycle, filtered, rolling average technique. Due to the oscillatory nature of frequency excursions, this instantaneous value can sometimes be misleading, either causing unexpected operation or excessive instability. For this reason, the device also provides an element for monitoring the longer term frequency trend, thereby reducing the effects of non-linearity in the system.

Average Rate of Change of Frequency protection is also known as f+Df/Dt protection (note the upper-case "D").

7.1 AVERAGE R.O.C.O.F PROTECTION IMPLEMENTATION

The device provides nine independent stages of average rate of change of frequency protection. Each stage can respond to either rising or falling frequency conditions. This depends on whether the frequency threshold is set above or below the system nominal frequency. For example, if the frequency threshold is set above nominal frequency, the rate of change of frequency setting is considered as positive and the element will operate for rising frequency conditions. If the frequency threshold is set below nominal frequency, the setting is considered as negative and the element will operate for falling frequency conditions.

When the measured frequency crosses the supervising frequency threshold, a timer is initiated. At the end of this time period, the frequency difference is evaluated and if this exceeds the setting, a trip output is given.

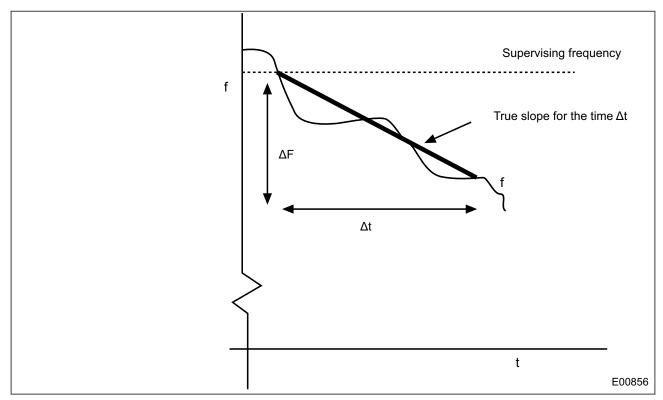


Figure 142: Average rate of change of frequency characteristic

After time Δt , the element is blocked from further operation until the frequency recovers to a value above the supervising frequency threshold. If the element has operated, the trip DDB signal will be ON until the frequency recovers to a value above the supervising frequency threshold.

The average rate of change of frequency is then measured based on the frequency difference, Δf over the settable time period, Δt .

The following settings are relevant for Df/Dt protection:

- f+Df/Dt (n) Status: determines whether the stage is for falling or rising frequency conditions
- f+Df/Dt (n) Freq: defines the frequency pickup setting
- f+Df/Dt (n) Dfreq: defines the change in frequency that must be measured in a set time period
- f+Df/Dt (n) Dtime: sets the time period over which the frequency is monitioned

7.2 AVERAGE R.O.C.O.F LOGIC

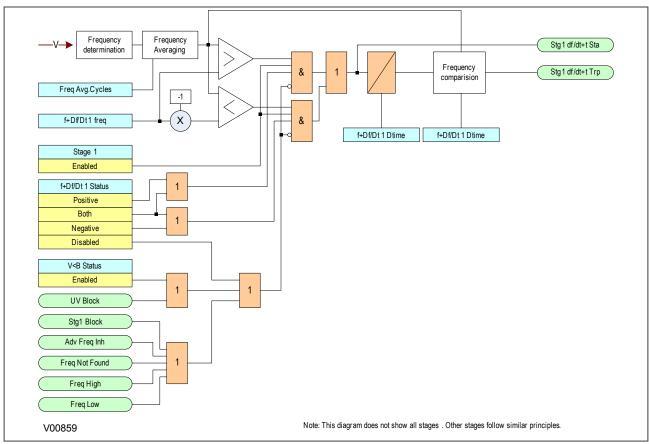


Figure 143: Average rate of change of frequency logic (single stage)

7.3 APPLICATION NOTES

7.3.1 SETTING GUIDELINES

The average rate of change of frequency element can be set to measure the rate of change over a short period as low as 20 ms (1 cycle @ 50 Hz) or a relatively long period up to 2 s (100 cycles @ 50 Hz). With a time setting, Dt, towards the lower end of this range, the element becomes similar to the frequency supervised rate of change function, "f+df/dt". With high Dt settings, the element acts as a frequency trend monitor.

Although the element has a wide range of setting possibilities we recommend that the Dt setting is set greater than 100 ms to ensure the accuracy of the element.

A possible four stage load shedding scheme using the average rate of change frequency element is shown in the following table:

	Frequency "f+t [81U/81O]" Elements		Average Rate of Change of Frequency "f+Df/Dt [81RAV]" Element		
Stage	(f+t) f Frequency Setting (Hz)	(f+t) t Time Setting (Sec.)	(f+Df/Dt) f Frequency Setting (Hz)	(f+Df/Dt) Df Frequency Diff Setting, (Hz)	(f+Df/Dt) Dt Time Period, (Sec.)
1	49	20	49	0.5	0.5
2	48.6	20	48.6	0.5	0.5
3	48.2	10	48.2	0.5	0.5
4	47.8	10	47.8	0.5	0.5

In the above scheme, the faster load shed decisions are made by monitoring the frequency change over 500 ms. Therefore tripping takes place more slowly than in schemes employing frequency-supervised df/dt, but the difference is not very much at this setting. If the delay jeopardises system stability, then the scheme can be improved by increasing the independent "f" setting. Depending on how much this value is increased, the frequency at which the "f+Df/Dt" element will trip also increases and so reduces the time delay under more severe frequency fluctuations. For example, with the settings shown below, the first stage of load shedding would be tripped approximately 300 msecs after 49.0 Hz is reached and at a frequency of approximately 48.7 Hz.

	Frequency "f+t [81U/810]" Elements		Average Rate of Change of Frequency "f+Df/Dt [81RAV]" Elements		
Stage	(f+t) f Frequency Setting (Hz)	(f+t) t Time Setting (Sec)	(f+Df/Dt) f Frequency Setting (Hz)	(f+Df/Dt) Df Frequency Diff Setting (Hz)	(f+Df/Dt) Dt Time Period, (Sec.)
1	49	20	49.2	0.5	0.5 s
2	48.6	20	48.8	0.5	0.5 s
3	48.2	10	48.4	0.5	0.5 s
4	47.8	10	48.0	0.5	0.5 s

8 LOAD SHEDDING AND RESTORATION

The goal of load shedding is to stabilise a falling system frequency. As the system stabilises and the generation capability improves, the system frequency will recover to near normal levels and after some time delay it is possible to consider the restoration of load onto the healthy system. However, load restoration needs to be performed carefully and systematically so that system stability is not jeopardized again.

In the case of industrial plants with captive generation, load restoration should be linked to the available generation since connecting additional load when the generation is still inadequate, will only result in declining frequency and more load shedding. If the in-plant generation is insufficient to meet the load requirements, then load restoration should be interlocked with recovery of the utility supply.

Whilst load shedding leads to an improvement in the system frequency, the disconnected loads need to be reconnected after the system is stable again. Loads should only be restored if the frequency remains stable for some period of time (minor frequency excursions can be ignored during this time period). The number of load restoration steps is normally less than the load shedding steps to reduce repeated disturbances while restoring load.

8.1 LOAD RESTORATION IMPLEMENTATION

The device uses the measurement of system frequency as the main criteria for load restoration. For each stage of load restoration, it is necessary that the same stage of load shedding has occurred previously and that no elements within that stage are configured for overfrequency or rising frequency conditions. If load shedding has not previously occurred, the load restoration for that stage is inactive.

The device provides nine independent stages of Load Restoration. It is implemented in the *FREQ PROTECTION* column of the relevant settings group. The following settings are relevant for Load Restoration:

- Restore(n) Status: determines whether the stage is disabled or enabled
- Restore(n) Freq: defines the frequency pickup setting
- Restore(n) Time: Timer period for which the measured frequency must be higher than the stage restoration.
- Holding Timer: Sets the holding timer value

8.2 HOLDING BAND

Load restoration for a given stage begins when the system frequency rises above the **Restore(n) Freq** setting for that stage and the stage restoration timer **Restore(n) Time** is initiated. If the system frequency remains above the frequency setting for the set time delay, load restoration of that stage will be triggered.

Unfortunately, frequency recovery profiles are highly non-linear and it would be reasonably common for the system frequency to fall transiently below the restoration frequency threshold. If the restoration timer immediately reset whenever a frequency dip occurred, it is likely that load restoration would never be successful. For this reason, the protection has a "holding band". This holding band is a region defined by the restoration frequency and the highest frequency setting used in the load shedding elements for that stage. The difference between these two settings must always be greater than 0.02 Hz, otherwise a *Wrong Setting* alarm will be generated. Whenever the system frequency dips into the holding band, operation of the stage restoration timer is suspended until the frequency rises above the restoration frequency setting, at which point timing will continue. If the system frequency dip is sufficiently large to cause any frequency element to start or trip in this stage, i.e. if the frequency falls below the lower limit of the holding band, the restoration timer will immediately be reset. This is demonstrated below.

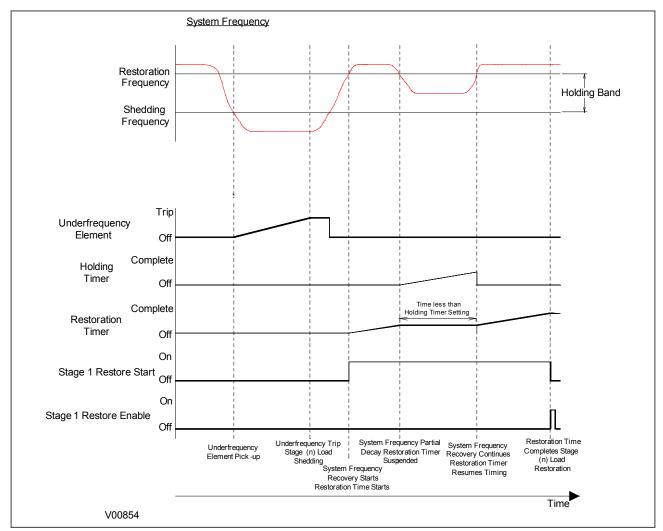


Figure 144: Load restoration with short deviation into holding band

If the system frequency remains in the holding band for too long it is likely that other system frequency problems are occurring and it would be prudent to reset the restoration timer for that stage. For this reason, as soon as the system frequency is measured to be within the holding band, the "Holding Timer" is initiated. If the system frequency doesn't leave the holding band before the holding timer setting has been exceeded, the load restoration time delay for that stage is immediately reset.

Note:

The holding timer has a common setting for all stages of load restoration.

An example of the case when the time in the holding band is excessive is shown below.

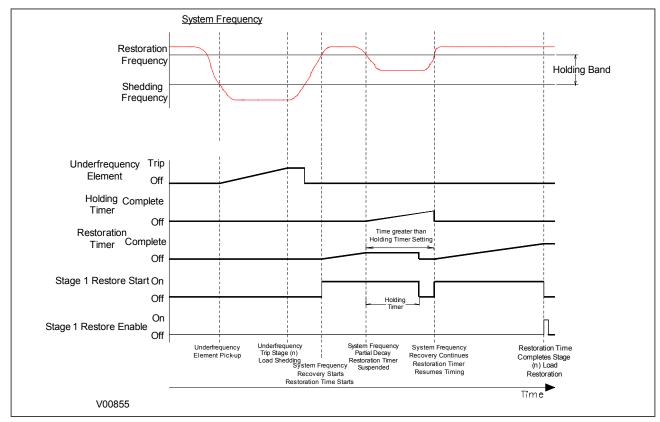


Figure 145: Load restoration with long deviation into holding band

Stg1 f+t Trp Stg1 df/dt+t Trp Load Restoration Cumulative Stg1 f+df/dt Trp Stg1 Restore Sta Function Timer Stg1f+DfDtTrp Stg1 Restore CIs Restore1 Status Restore1 Time Enabled Disabled V<B Status Enabled UV Block Stg1 Block Adv Freq Inh Freq Not Found Freq High Freq Low Frequency determination Averaging Freq Avg.Cycles Holding function Restore1 Freq Highest Freq setting Holding Timer 1 Note: This diagram does not show all stages . Other stages follow similar principles. V00860

8.3 LOAD RESTORATION LOGIC

Figure 146: Load Restoration logic

8.4 APPLICATION NOTES

8.4.1 SETTING GUIDELINES

A four stage, single frequency load restoration scheme is shown below. The frequency setting has been chosen such that there is sufficient separation between the highest load shed frequency and the restoration frequency to prevent any possible hunting. A restoration frequency setting closer to nominal frequency may be chosen if an operating frequency of 49.3 Hz is unacceptable.

Stage	Restoration Frequency Setting (Hz)	Restoration Time Delay (secs)	Holding Time Delay (secs)
1	49.3 Hz	240 sec	20 sec
2	49.3 Hz	180 sec	20 sec
3	49.3 Hz	120 sec	20 sec
4	49.3 Hz	60 sec	20 sec

In this scheme, the time delays ensure that the most critical loads are reconnected (assuming that the higher stages refer to more important loads). By restoring the load sequentially, system stability should normally be maintained. These time settings are system dependent; higher or lower settings may be required depending on the particular application.

It is possible to set up restoration schemes involving multiple frequencies. This allows faster restoration of loads, but there is the possibility of continuous system operation at frequencies far removed from the nominal. A typical scheme using two frequencies is illustrated below:

Stage	Restore Freq. Restoration Frequency Setting (Hz)	Restore DelayRestoration Time Delay (S)	Holding Time Delay (S)
1	49.5 Hz	120 sec	20 sec
2	49.5 Hz	60 sec	20 sec
3	49.0 Hz	120 sec	20 sec
4	49.0 Hz	60 sec	20 sec

Staggered time settings may be used in this scheme as well, but the time separation among the restoration of stages will be a function of the frequency recovery pattern. Time coordinated restoration can only be guaranteed for those stages with a common restoration frequency setting.

CHAPTER 12

POWER PROTECTION FUNCTIONS

1 CHAPTER OVERVIEW

Power protection is used for protecting generators. Although the main function of this device is for feeder applications, it can also be used as a cost effective alternative for protecting small distributed generators, typically less than 2 MW.

This chapter contains the following sections:

Chapter Overview	265
Overpower Protection	266
Underpower Protection	269
Sensitive Power Protection	272
Transient Earth Fault Detection	276

2 OVERPOWER PROTECTION

With Overpower, we should consider two distinct conditions: Forward Overpower and Reverse Overpower.

A forward overpower condition occurs when the system load becomes excessive. A generator is rated to supply a certain amount of power and if it attempts to supply power to the system greater than its rated capacity, it could be damaged. Therefore overpower protection in the forward direction can be used as an overload indication. It can also be used as back-up protection for failure of governor and control equipment. Generally the Overpower protection element would be set above the maximum power rating of the machine.

A reverse overpower condition occurs if the generator prime mover fails. When this happens, the power system may supply power to the generator, causing it to motor. This reversal of power flow due to loss of prime mover can be very damaging and it is important to be able to detect this with a Reverse Overpower element.

2.1 OVERPOWER PROTECTION IMPLEMENTATION

Overpower Protection is implemented in the *POWER PROTECTION* column of the relevant settings group, under the sub-heading *OVERPOWER*.

The Overpower Protection element provides 2 stages of directional overpower for both active and reactive power. The directional element can be configured as forward or reverse and can activate single-phase or three-phase trips.

The elements use three-phase power and single phase power measurements as the energising quantities. A Start condition occurs when two consecutive measurements exceed the setting threshold. A trip condition occurs if the Start condition is present for the set time delay. This can be inhibited by the VTS Slow Block and Pole Dead logic if desired.

The Start and Trip timer resets if the power falls below the drop-off level or if an inhibit condition occurs. The reset mechanism is similar to the overcurrent functionality for a pecking fault condition, where the percentage of elapsed time for the operate timer is memorised for a set reset time delay. If the Start condition returns before the reset timer has timed out, the operate time initialises from the memorised travel value. Otherwise the memorised value is reset to zero after the reset time times out.

Power>1 Start P(A, B, or C) DT Power>1 Trip Power>1 1 Ph Watt Power>1 1Ph VAR Power>1TimeDelay Power>1 Mode Active -1 Reactive Power>1 3 PhStart P(3 phase) DT Power>1 3Ph Watt Power>1 3Ph Trip Power>1 3Ph VAR Power>1TimeDelay Power>1 Mode Active -1 & Reactive Power>1Direction Forward Reverse Power>1 Status

2.2 OVERPOWER LOGIC

Figure 147: Overpower logic

V00900

Enabled
VTS Slow Block

2.3 APPLICATION NOTES

2.3.1 FORWARD OVERPOWER SETTING GUIDELINES

The relevant power threshold settings should be set greater than the full load rated power.

The operating mode should be set to Forward.

A time delay setting (*Power>(n) TimeDelay*) should be applied. This setting is dependant on the application, but would typically be around 5 seconds. The delay on the reset timer (*Power>(n) tRESET*), would normally be set to zero.

2.3.2 REVERSE POWER CONSIDERATIONS

A generator is expected to supply power to the connected system in normal operation. If the generator prime mover fails, it will begin to motor (if the power system to which it is connected has other generating sources). The consequences of generator motoring and the level of power drawn from the power system will be dependent on the type of prime mover.

Typical levels of motoring power and possible motoring damage that could occur for various types of generating plant are given in the following table.

Prime mover	Motoring power	Possible damage (percentage rating)		
Diesel Engine 5% - 25%		Risk of fire or explosion from unburned fuel		
Motoring level depends on compression ratio and cylinder bore stiffness. Rapid disconnection is required to limit power loss and risk of damage.				
Gas Turbine	10% - 15% (Split-shaft) >50% (Single-shaft)	With some gear-driven sets, damage may arise due to reverse torque on gear teeth.		

Prime mover	Motoring power	Possible damage (percentage rating)		
Compressor load on single shaft machines leads to a high motoring power compared to split-shaft machines. Rapid disconnection is required to limit power loss or damage.				
Hydraulic Turbines 0.2 - >2% (Blades out of water) >2.0% (Blades in water) Blade and runner damage may occur with a long period of motoring				
Power is low when blades are above tail-race water level. Hydraulic flow detection devices are often the main means of detecting loss of drive. Automatic disconnection is recommended for unattended operation.				
Steam Turbines 0.5% - 3% (Condensing sets) 3% - 6% (Non-condensing sets) Thermal stress damage may be inflicted on low-pressure turbine blades when steam flow is not available to dissipate losses due to air resistance.				
Damage may occur rapidly with non-condensing sets or when vacuum is lost with condensing sets. Reverse power protection may be used as a secondary method of detection and might only be used to raise an alarm.				

In some applications, the level of reverse power in the case of prime mover failure may fluctuate. This may be the case for a failed diesel engine. To prevent cyclic initiation and reset of the main trip timer, an adjustable reset time delay is provided. You will need to set this time delay longer than the period for which the reverse power could fall below the power setting. This setting needs to be taken into account when setting the main trip time delay.

Note:

A delay in excess of half the period of any system power swings could result in operation of the reverse power protection during swings.

2.3.3 REVERSE OVERPOWER SETTING GUIDELINES

Each stage of power protection can be selected to operate as a reverse power stage by selecting the **Power>(n) Direction** cell to *Reverse*.

The relevant power threshold settings should be set to less than 50% of the motoring power.

The operating mode should be set to Reverse.

The reverse power protection function should be time-delayed to prevent false trips or alarms being given during power system disturbances or following synchronisation.

A time delay setting, of approximately 5 s would be typically applied.

The delay on the reset timer, *Power>1 tRESET* or *Power>2 tRESET*, would normally be set to zero.

When settings of greater than zero are used for the reset time delay, the pick-up time delay setting may need to be increased to ensure that false tripping does not result in the event of a stable power swinging event.

Reverse overpower protection can also be used for loss of mains applications. If the distributed generator is connected to the grid but not allowed to export power to the grid, it is possible to use reverse power detection to switch off the generator. In this case, the threshold setting should be set to a sensitive value, typically less than 2% of the rated power. It should also be time-delayed to prevent false trips or alarms being given during power system disturbances, or following synchronisation. A typical time delay is 5 seconds.

3 UNDERPOWER PROTECTION

Although the Underpower protection is directional and can be configured as forward or reverse, the most common application is for Low Forward Power protection.

When a machine is generating and the circuit breaker connecting the generator to the system is tripped, the electrical load on the generator is cut off. This could lead to overspeeding of the generator if the mechanical input power is not reduced quickly. Large turbo-alternators, with low-inertia rotor designs, do not have a high over speed tolerance. Trapped steam in a turbine, downstream of a valve that has just closed, can rapidly lead to over speed. To reduce the risk of over speed damage, it may be desirable to interlock tripping of the circuit breaker and the mechanical input with a low forward power check. This ensures that the generator circuit breaker is opened only after the mechanical input to the prime mover has been removed, and the output power has reduced enough such that overspeeding is unlikely. This delay in tripping the circuit breaker may be acceptable for non-urgent protection trips (e.g. stator earth fault protection for a high impedance earthed generator). For urgent trips however (e.g. stator current differential protection), this Low Forward Power interlock should not be used.

3.1 UNDERPOWER PROTECTION IMPLEMENTATION

Underpower Protection is implemented in the *POWER PROTECTION* column of the relevant settings group, under the sub-heading *UNDERPOWER*.

The UNDERPOWER Protection element provides 2 stages of directional underpower for both active and reactive power. The directional element can be configured as forward or reverse and can activate single-phase or three-phase trips.

The elements use three-phase power and single phase power measurements as the energising quantity. A start condition occurs when two consecutive measurements fall below the setting threshold. A trip condition occurs if the start condition is present for the set trip time. This can be inhibited by the VTS slow block and pole dead logic if desired.

The Start and Trip timer resets if the power exceeds the drop-off level or if an inhibit condition occurs. The reset mechanism is similar to the overcurrent functionality for a pecking fault condition, where the percentage of elapsed time for the operate timer is memorised for a set reset time delay. If the Start condition returns before the reset timer has timed out, the operate time initialises from the memorised travel value. Otherwise the memorised value is reset to zero after the reset time times out.

3.2 UNDERPOWER LOGIC

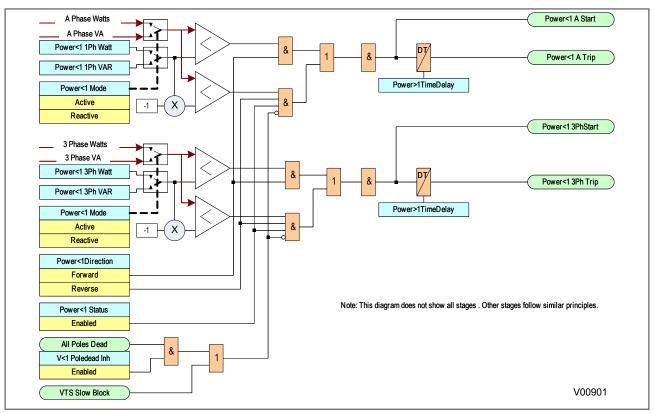


Figure 148: Underpower logic

3.3 APPLICATION NOTES

3.3.1 LOW FORWARD POWER CONSIDERATIONS

The Low Forward Power protection can be arranged to interlock 'non-urgent' protection tripping using the programmable scheme logic. It can also be arranged to provide a contact for external interlocking of manual tripping. To prevent unwanted alarms and flags, a Low Forward Power protection element can be disabled when the circuit breaker is opened via Pole Dead logic.

The Low Forward Power protection can also be used to provide loss of load protection when a machine is motoring. It can be used for example to protect a machine which is pumping from becoming unprimed, or to stop a motor in the event of a failure in the mechanical transmission.

A typical application would be for pump storage generators operating in the motoring mode, where there is a need to prevent the machine becoming unprimed which can cause blade and runner damage. During motoring conditions, it is typical for the protection to switch to another setting group with the low forward power enabled and correctly set and the protection operating mode set to *Reverse*.

A low forward power element may also be used to detect a loss of mains or loss of grid condition for applications where the distributed generator is not allowed to export power to the system.

3.3.2 LOW FORWARD POWER SETTING GUIDELINES

Each stage of power protection can be selected to operate as a forward power stage by selecting the **Power<(n) Direction** cell to Forward.

When required for interlocking of non-urgent tripping applications, the threshold setting of the low forward power protection function should be less than 50% of the power level that could result in a dangerous overspeed condition on loss of electrical loading.

When required for loss of load applications, the threshold setting of the low forward power protection function, is system dependent, however, it is typically set to 10 - 20% below the minimum load. The operating mode should be set to *Reverse* for this application.

For interlocking non-urgent trip applications the time delay associated with the low forward power protection function could be set to zero. However, some delay is desirable so that permission for a non-urgent electrical trip is not given in the event of power fluctuations arising from sudden steam valve/throttle closure. A typical time delay is 2 seconds.

For loss of load applications the pick-up time delay is application dependent but is normally set in excess of the time between motor starting and the load being established. Where rated power cannot be reached during starting (for example where the motor is started with no load connected) and the required protection operating time is less than the time for load to be established then it will be necessary to inhibit the power protection during this period. This can be done in the PSL using AND logic and a pulse timer triggered from the motor starting to block the power protection for the required time.

When required for loss of mains or loss of grid applications where the distributed generator is not allowed to export power to the system, the threshold setting of the reverse power protection function, should be set to a sensitive value, typically <2% of the rated power.

The low forward power protection function should be time-delayed to prevent false trips or alarms being given during power system disturbances or following synchronisation. A time delay setting, of 5 s should be applied typically.

The delay on the reset timers would normally be set to zero.

To prevent unwanted alarms and flags, the protection element can be disabled when the circuit breaker is open via Pole Dead logic.

4 SENSITIVE POWER PROTECTION

In some applications, it is necessary to have very high accuracy when applying power protection. For such applications it is possible to use metering class CTs and separate Sensitive Power elements.

The Sensitive Power protection is a single-phase power element using phase A current and voltage. It provides two independent stages of Low Forward Power, Reverse Power and Over Power protection with timer and pole-dead blocking.

Note:

Sensitive Power Protection is only available for models equipped with a SEF transformer.

4.1 SENSITIVE POWER PROTECTION IMPLEMENTATION

Sensitive Power Protection is implemented in the *POWER PROTECTION* column of the relevant settings group, under the sub-heading *SENSITIVE POWER*. It is a single phase power element using the A-phase voltage and sensitive current ISEF.

There are two stages of Sensitive Power protection, which can be independently selected as Low Forward Power, Reverse Power and Overpower.

Note

When the sensitive power function is used, the SEF CT must be connected to Phase A current, making the measured power ISEF \times VA.

4.2 SENSITIVE POWER MEASUREMENTS

Three sensitive power related measurements are added to the Measurements column, the visibility of which will depend on the protection configuration.

- A-Phase Sensitive Active Power in Watts (APh Sen Watts)
- A-Phase Sensitive Re-active Power in VArs (APh Sen VARs)
- A-Phase Sensitive Power Angle (APh Power Angle)

SensP1 Start A Aph Sen Watts DT Sens P>1 Setting SensP1 Trip A Sens P1 Delay Aph Sen Watts Sens -P>1Setting Aph Sen Watts Sens P<1 Setting Aph Sens Power Enabled Sens P1 Function Note: This diagram does not show all stages. Other stages follow similar principles. It also does not show all phases. Other phases follow similar principles. Reverse Low Forward Disabled P1 Poledead Inh Enabled VTS Slow Block

4.3 SENSITIVE POWER LOGIC

Figure 149: Sensitive Power logic diagram

4.4 APPLICATION NOTES

4.4.1 SENSITIVE POWER CALCULATION

Input Quantities

V00902

Sensitive power is calculated from the A-phase-neutral voltage and the A-phase sensitive current input.

The calculation for active power with the correction angle is:

$$P_{A} = I_{AS}V_{A}\cos(\varphi - \theta_{C})$$

where:

- P_A = sensitive power
- $V_A = A$ -phase voltage
- I_{AS} = A-phase sensitive current
- Φ = the angle of I_{AS} with respect to V_A
- θ_C = the CT correction angle

Calculations within the device are based upon quadrature components obtained from the Fourier analysis of the input signals. The quadrature values for V_A and I_{AS} are used for the sensitive power calculation as shown:

$$\overline{V}_{A} = V_{Ar} + jV_{Ai}$$

$$\overline{I}_{AS} = I_{ASr} + jI_{ASi}$$

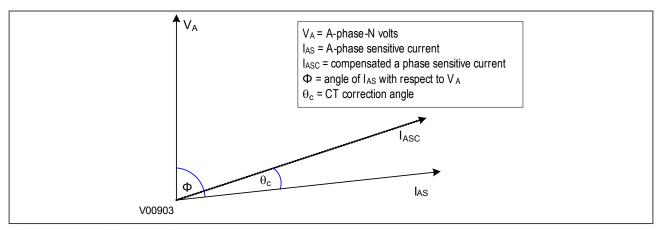


Figure 150: Sensitive Power input vectors

CT Compensation

The CT correction rotates the I_{AS} vector by the correction angle. This correction is performed before the power calculation and can be achieved with the use of a rotation matrix:

$$\begin{bmatrix} \cos \theta_C & -\sin \theta_C \\ \sin \theta_C & \cos \theta_C \end{bmatrix}$$

The corrected phase-A sensitive current $I_{\mbox{\scriptsize ASC}}$ is therefore:

$$\overline{I}_{ASC} = \begin{bmatrix} I_{ASCr} \\ I_{ASCi} \end{bmatrix} = \overline{I}_{AS} = \begin{bmatrix} I_{ASr} \\ I_{ASi} \end{bmatrix} \begin{bmatrix} \cos \theta_C & -\sin \theta_C \\ \sin \theta_C & \cos \theta_C \end{bmatrix} = \begin{bmatrix} I_{ASr} \cos \theta_C - I_{ASi} \sin \theta_C \\ I_{ASr} \sin \theta_C + I_{ASi} \cos \theta_C \end{bmatrix}$$

therefore:

$$I_{ASCr} = I_{ASr} \cos \theta_C - I_{ASi} \sin \theta_C$$

and

$$I_{ASCi} = I_{ASr} \sin \theta_C + I_{ASi} \cos \theta_C$$

Active Power Calculation

The compensated A-phase sensitive current vector is used to calculate the sensitive A-Phase active power P_{AS} .

Using the equation:

$$P_{AS} = Re \overline{V}_A \overline{I}_{ASC}^*$$

we can derive:

$$\begin{split} P_{AS} &= Re\left(V_{Ar} + jV_{Ai}\right)\left(I_{ASCr} + jI_{ASCi}\right) \\ &= Re\left(V_{Ar} + jV_{Ai}\right)\left(I_{ASCr} - jI_{ASCi}\right) = Re\left(V_{Ar}I_{ASCr} + V_{Ai}I_{ASCi}\right) + j\left(V_{Ai}I_{ASCr} - V_{Ar}I_{ASCi}\right) \\ &= V_{Ar}I_{ASCr} + V_{Ai}I_{ASCi} \end{split}$$

4.4.2 SENSITIVE POWER SETTING GUIDELINES

For reverse and low forward power protection, if settings greater than 3% Pn are used, the phase angle errors of suitable protection class current transformers will not result in any risk of maloperation. If settings of less than 3% are used, however, we recommend that the current input is driven by a correctly loaded metering class current transformer.

The sensitive power protection has a minimum setting accuracy of 0.5% Pn. It uses the In sensitive CT to calculate single-phase active power. It also provides phase compensation to remove errors introduced by the primary input transformers.

5 TRANSIENT EARTH FAULT DETECTION

Some distribution systems run completely insulated from earth. Such systems are called unearthed systems. The advantage of an unearthed system is that a single phase to earth fault does not cause an earth fault current to flow. This means the whole system remains operational and the supply is not interrupted. The system must be designed to withstand high transient and steady state overvoltages, however, and so its use is generally restricted to low and medium voltage distribution systems.

When there is an earth fault in an unearthed 3-phase system, the voltage of the faulted phase is reduced to the earth potential. This causes the phase voltage in the other two phases to increase, which causes a significant charging current between the phase-to-earth capacitances. This can cause arcing at the fault location. Many systems use a Petersen coil to compensate for this, thus eliminating the arcing problem. Such systems are called compensated networks. The network is earthed with an inductive reactor, where its reactance is made nominally equal to the total system capacitance to earth. Under this condition, a single-phase earth fault does not result in any steady state earth fault current.

The introduction of a Petersen coil introduces major difficulties when it comes to determining the direction of the fault. This is because the faulted line current is the sum of the inductive current introduced by the Petersen coil and the capacitive current of the line, which are in anti-phase with each other. If they are equal in magnitude, the current in the faulted line is zero. If the inductive current is larger than capacitance current, the direction of the faulted line current will appear to be in the same direction as that of the healthy line.

Standard directionalizing techniques used by conventional feeder protection devices are not adequate for this scenario, therefore we need a different method for determining the direction of the fault. Two commonly used methods are the First Half Wave method and the Residual Active Power method.

First Half Wave Method

The initial transient wave, generated at the fault point travels towards the bus along the faulted line, until it reaches the healthy line. For forward faults the high frequency fault voltage and current components are in opposite directions during the first half wave, whereas for reverse faults, they are in phase. This fact can be used to determine the fault direction. This method, however, is subject to the following disadvantages:

- The time duration of the characteristic is very short, in most cases not more than 3 ms. Because of this, it requires a high sampling frequency (3000Hz or even higher)
- It requires an analogue high pass filter, necessitating special hardware
- It is affected by the fault inception angle. For example, when the fault inception angle is 0°, there are no initial travelling waves.

Residual Active Power Method

Residual Active power, which is sometimes used to detect the instance of a fault can also in some cases be used for detecting the fault direction. Although the capacitive currents can be compensated by an inductive current generated by a Petersen coil, the active (instantaneous) current can never be compensated for and this is still opposite to that of the healthy line. This fact can also be used to directionalise the fault.

For a forward directional fault, the zero-sequence active power is the power loss of Petersen's coil, which is negative. For a reverse fault, the zero-sequence active power is the power loss of the transmission line, which is positive. This method, however, is subject to the following disadvantages:

- The zero-sequence active power will be very small in magnitude for a reverse directional fault. Its value depends on the power loss of transmission line.
- The zero-sequence active power may be too small in magnitude to be detected for a forward directional fault. Its value depends on the power loss of Petersen coil.
- High resolution CTs are required

Due to the low magnitude of measured values, reliability is compromised

This product does not use the above techniques for directionalisation. This product uses an innovative patented technique called Transient Reactive Power method to determine the fault direction of an earth fault in a compensated network.

5.1 TRANSIENT EARTH FAULT DETECTION IMPLEMENTATION

Transient Earth Fault Detection (TEFD) in this device comprises three modules:

- Transient Earth Fault Detection module (TEF)
- Fault Type Detector (FTD)
- Direction Detector (DD)

5.1.1 TRANSIENT EARTH FAULT DETECTOR

To establish if there is an earth fault on the system somewhere is straightforward. A simple residual overvoltage comparison can determine this. Therefore, a TEF> Start signal is produced by comparing the neutral voltage with a threshold voltage set by *TEF VN> Start* in the *TEF DETECTION* column. The difficulty comes with establishing the type of fault and its direction.

5.1.2 FAULT TYPE DETECTOR

The FTD uses a Fundamental analysis (FA) technique to establish whether the fault is an intermittent fault or a steady state faults. For Transient Earth Fault Detection, the detector counts the Residual Voltage bursts within a specified time window. With some clever signal processing the detector module creates pulses by comparing the bursts with a settable threshold, then counts these pulses. If the number of pulses equals or exceeds the number specified by the FTD> Fault Count setting, within the time window specified by FTD> Time Window, the fault is deemed to be intermittent and the TEF> Intermit DDB signal is asserted. If there are fewer pulses than this number, this indicates either a disturbance or a permanent fault. To establish which, we need to look at the RMS value of the residual voltage.

If there are fewer pulses than specified and the RMS value does not drop below setting within the specified time window, the fault is deemed to be permanent. In this case the *TEF> Steady* DDB signal is asserted.

If there are fewer pulses than specified and the RMS value does drop below setting, this indicates that a disturbance has been detected but it is not a fault. In this case, the *TEF> Steady* DDB signal is not asserted.

The user can map the signals *TEF>Steady*, *TEF>Intermit*, *TEF>DIR FWD* or *TEF> DIR REV* to the TEF Alarm Logic DDB to generate a TEF Alarm.

The inputs to this module are:

- The residual voltage
- FTD> VN (defines the threshold which converts the residual voltage burst into a pulse
- FTD> Time Window (defines the time window default is 2 seconds)
- FTD> Fault Count (defines the fault count)

The FTD outputs two signals to indicate whether the fault is steady state or intermittent.

5.1.3 DIRECTION DETECTOR

The Direction Detector (DD) uses a patented technique based on Transient Reactive Power (TRP) to establish the direction of the fault. Unlike traditional methods, this TRP method does not require high resolution CTs or special analogue filtering hardware and is therefore cheaper to implement.

It can be shown that the residual voltage and residual current components can be reliably used as discriminative criteria between a faulty and healthy feeder at 220Hz.

The admittance response of a healthy distributed feeder is shown below using a Pi model:

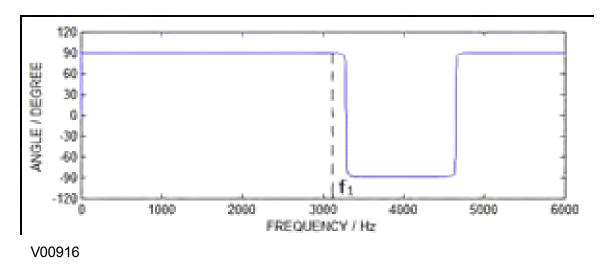


Figure 151: Healthy line response

In the above figure, the phase response of the admittance is consistent at 900 up to frequency f1 (approximately 3000Hz). For a compensated faulty feeder, the admittance response is shown below using a Pi model:

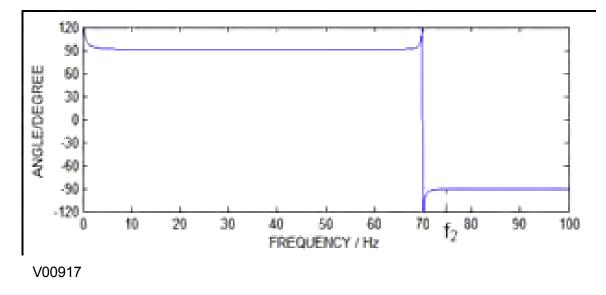


Figure 152: Faulty line response

We can observe that the phase angle (and thus, the reactive power flow) changes from 900 to -900 at frequencies higher than f2. Based on the above, we have clear direction discrimination between a healthy and faulted feeder at any frequency between f2 and f1 approximately.

Note:

The resonant frequency in the above system is 70Hz. For a perfectly compensated system, this will be 50Hz.

MiCOM relays use an anti-aliasing band pass filter with cut-off frequency of 150Hz. Furthermore, at 220Hz the post-filter magnitude is approximately 0.5pu, and at 330Hz, it is less than 0.2pu. To avoid any integer harmonics, and to avoid severely attenuated quantities due to the filter, we have chosen 220Hz as the most suitable frequency for direction determination.

In the forward direction, the residual voltage leads the residual current by 90°, and in the reverse direction the residual voltage lags the residual current by 90°. These criteria can be used to directionalise the fault.

The residual voltage (Vres) after passing through the bandpass filter tuned to 220 Hz, has 90° added to its phase. The residual current (Ires) is also passed through a 220 Hz bandpass filter, but no phase shift is applied. The resulting components which we shall call VH1 and IH2 are therefore in antiphase with each other for forward faults and in phase if the forward line is not faulted.

The VH1 and IH2 components are passed through a sign filter and multiplied to create a reactive power component in the range of -1 to +1. This is the transient reactive power Q_{tran} . If $Q_{tran} > 0$, then there forward line is healthy. If $Q_{tran} < 0$, then the forward line is faulty.

There are two modes of operation for the direction detector; Standard and Advanced. Standard mode is used in most cases and is described here. Advanced mode is for special applications that deviate from the standard model o_{ftw} 0 or more geographically close feeders outgoing from a power transformer. The following default settings are recommended for majority of applications:

- Dir>Vnf Thresh 8.000 V
- Dir>Inf Thresh 50.00 mA
- Dir>On Thresh 100.0e-3
- Dir>Qr Thresh 40.00e-3

When *TEF>Dir Mod* is set to *Advance*, the following settings become visible:

- Dir>Os Thresh 50.00e-3
- Qn Smooth fct 20.00e-3
- Operate.Cycles 6

Here, Qs is an integration of Q_n , with the window of integration being the first **Operate cycles** setting after the start signal is triggered. Q_s is used as a further discriminative directional feature if direction cannot be determined by Q_n only. Q_s is calculated by the following formula:

$$Q_{S} = \int_{(t=0)}^{(t=K*T)} (Q_{N(t)})$$

Where 'K' is the setting Operate Cycles. Operate Cycles affects Qs only.

Qn Smooth fact is a smoothing factor for consecutive Qn values which prevents sudden changes in the value of Qn. The calculated new value of Qn is:

new valueQn = old value*(1-smoothing factor)+ new value*smoothing factor.

It is important to note that all settings for the TGFD function, including those at 220Hz, can be set based on 50Hz nominal secondary values. This is because the gain of the 220Hz transient filter is 1.

The inputs to this module are:

- The residual voltage
- The residual current
- Dir> Vnf Thresh (defines the threshold for the residual voltage sign filter).
- Dir> Inf Thresh (defines the threshold for the residual current sign filter

The DD outputs two signals to indicate a forward fault and a reverse fault

Sign Filter Thresholds

The *Dir> Vnf Thresh* setting is used to get the sign of instantaneous voltage value by sign filter. If the input value is larger than Vnf, the output is +1. If the input value is less than -1*Vnf, the output is -1. Otherwise the output is 0.

The Dir > Inf Thresh setting is used to get the sign of instantaneous current value by sign filter. If the input value is larger than Vnf, the output is +1. If the input value is less than -1*Vnf, the output is -1. Otherwise the output is 0.

Qtran Thresholds

The setting Dir>Qn Thresh is the forward direction Q_{tran} threshold calculated from the quantised Vnf and Inf values.

The setting Dir is the reverse direction Q_{trans} threshold calculated from the quantised Vnf and Inf values.

The following DDBs are also available:

Timer Block: used to inhibit the TEF function and reset all associated DDBs

Reset TEF: can be configured as a user-defined manual reset alarms

TEF Alarm Output: This is the main TEF alarm that can be mapped to a relay output for a trip

5.2 TRANSIENT EARTH FAULT DETECTION LOGIC

5.2.1 TRANSIENT EARTH FAULT DETECTION LOGIC OVERVIEW

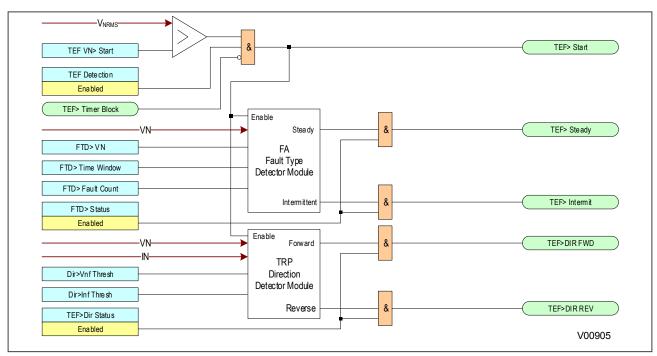


Figure 153: Transient Earth Fault Logic Overview

5.2.2 FAULT TYPE DETECTOR LOGIC

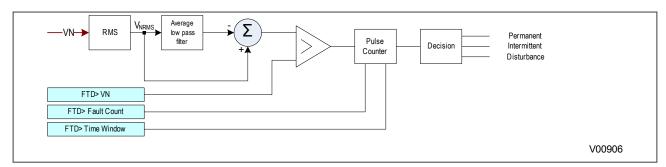


Figure 154: Fault Type Detector Logic

5.2.3 DIRECTION DETECTOR LOGIC - STANDARD MODE

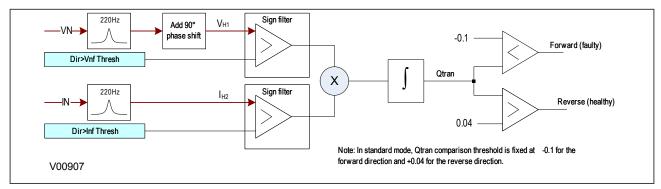


Figure 155: Direction Detector Logic - Standard Mode

5.2.4 TRANSIENT EARTH FAULT DETECTION OUTPUT ALARM LOGIC

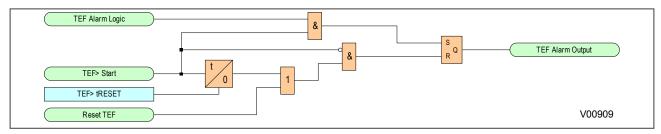


Figure 156: TEFD output alarm logic

CHAPTER 13

AUTORECLOSE

1 CHAPTER OVERVIEW

Selected models of this product provide sophisticated Autoreclose (AR) functionality. The purpose of this chapter is to describe the operation of this functionality including the principles, logic diagrams and applications.

This chapter contains the following sections:

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2 INTRODUCTION TO 3-PHASE AUTORECLOSE

It is known that approximately 80 - 90% of faults are transient in nature. This means that most faults do not last long and are self-clearing. A common example of a transient fault is an insulator flashover, which may be caused for example by lightning, clashing conductors or wind-blown debris.

A transient fault, such as an insulator flashover, is a self-clearing 'non-damage' fault. The flashover will cause one or more circuit breakers to trip, but it may also have the effect of clearing the fault. If the fault clears itself, the fault does not recur when the line is re-energised.

The remaining 10 – 20% of faults are either semi-permanent or permanent. A small tree branch falling on the line could cause a semi-permanent fault. Here the cause of the fault would not be removed by the immediate tripping of the circuit, but could be burnt away during a time-delayed trip. Permanent faults could be broken conductors, transformer faults, cable faults or machine faults, which must be located and repaired before the supply can be restored.

In the majority of fault incidents, if the faulty line is immediately tripped out, and time is allowed for the fault arc to deionise, reclosure of the circuit breakers will result in the line being successfully re-energised.

Autoreclose schemes are used to automatically reclose a circuit breaker a set time after it has been opened due to operation of a protection element.

On HV/MV distribution networks, autoreclosing is applied mainly to radial feeders, where system stability problems do not generally arise. The main advantages of using Autoreclose are:

- Minimal interruption in supply to the consumer
- Reduction of operating costs fewer man hours in repairing fault damage and the possibility of running unattended substations
- With Autoreclose, instantaneous protection can be used which means shorter fault durations. This in turn means less fault damage and fewer permanent faults

Autoreclosing provides an important benefit on circuits using time-graded protection, in that it allows the use of instantaneous protection to provide a high speed first trip. With fast tripping, the duration of the power arc resulting from an overhead line fault is reduced to a minimum. This lessens the chance of damage to the line, which might otherwise cause a transient fault to develop into a permanent fault. Using instantaneous protection also prevents blowing of fuses in teed feeders, as well as reducing circuit breaker maintenance by eliminating prearc heating.

When instantaneous protection is used with autoreclosing, the scheme is normally arranged to block the instantaneous protection after the first trip. Therefore, if the fault persists after re-closure, the time-graded protection will provide discriminative tripping resulting in the isolation of the faulted section. However, for certain applications, where the majority of the faults are likely to be transient, it is common practise to allow more than one instantaneous trip before the instantaneous protection is blocked.

Some schemes allow a number of re-closures and time-graded trips after the first instantaneous trip, which may result in the burning out and clearance of semi-permanent faults. Such a scheme may also be used to allow fuses to operate in teed feeders where the fault current is low.

When considering feeders that are partly overhead line and partly underground cable, any decision to install autoreclosing should be subject to analysis of the data (knowledge of the frequency of transient faults). This is because this type of arrangement probably has a greater proportion of semi-permanent and permanent faults than for purely overhead feeders. In this case, the advantages of autoreclosing are small. It can even be disadvantageous because re-closing on to a faulty cable is likely to exacerbate the damage.

3 IMPLEMENTATION

Autoreclose functionality is a software option, which is selected when ordering the device, so this description only applies to models with this option.

Autoreclose works for phase overcurrent (POC) earth fault (EF) and sensitive earth fault (SEF) protection. It is implemented in the *AUTORECLOSE* column of the relevant settings group. In addition to the settings contained in this column, you will also need to make some settings in the blocking cells of the relevant protection columns.

The Autoreclose function can be set to perform a single-shot, two-shot, three-shot or four-shot cycle. You select this by the *Number of Shots* cell in the *AUTORECLOSE* column. You can also initiate a separate Autoreclose cycle for the SEF protection, with a different number of shots, selected by the *Number SEF Shots* cell. Dead times for all shots can be adjusted independently.

An Autoreclose cycle can be initiated internally by operation of a protection element, or externally by a separate protection device. The dead time starts in one of two cases; when the circuit breaker has tripped, or when the protection has reset. You select this using the **Start Dead t On** cell.

At the end of the relevant dead time, a *CB Closed 3 ph* signal is given, providing it is safe for the circuit breaker to close. This is determined by checking that certain system conditions are met as specified by the **System Checks** functionality.

It is safe to close the circuit breaker providing that:

- only one side of the circuit breaker is live (either dead line / live bus, or live line / dead bus), or
- if both bus and line sides of the circuit breaker are live, the system voltages are synchronised.

In addition, the energy source powering the circuit breaker (for example the closing spring) must be fully charged. This is indicated from the *CB Healthy* DDB input.

When the CB has closed, the reclaim time starts. If the circuit breaker does not trip again, the Autoreclose function resets at the end of the set reclaim time. If the protection operates during the reclaim time the device either advances to the next shot in the Autoreclose cycle, or if all reclose attempts have been made, goes to lockout.

CB Status signals must also be available, so the default setting for *CB Status Input* should be modified according to the application. The default PSL requires 52A, 52B and CB Healthy logic inputs, so a setting of both **52A and 52B** would be required for the *CB Status Input* if used with the default PSL.

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4 AUTORECLOSE FUNCTION INPUTS

The Autoreclose function has several logic inputs, which can be mapped to any of the opto-inputs or to one or more of the DDB output signals generated by the PSL. The functions of these inputs are described below.

4.1 CB HEALTHY

It is necessary to establish if there is sufficient energy in the circuit breaker (spring charged, gas pressure healthy, etc.) before the CB can be closed. This **CB Healthy** input is used to ensure this before initiating a **CB closed 3ph** command. If on completion of the dead time, the **CB Healthy** input is low, and remains low for a period given by the **CB Healthy Time** timer, lockout will result and the circuit breaker will remain open.

The majority of circuit breakers are only capable of providing a single trip-close-trip cycle, in which case the **CB Healthy** signal would stay low after one Autoreclose shot, resulting in lockout.

This check can be disabled by not allocating an opto-input for the *CB Healthy* signal, whereby the signal defaults to a High state.

4.2 BLOCK AR

The *Block AR* input blocks the Autoreclose function and causes a lockout. It can be used when protection operation without Autoreclose is required. A typical example is on a transformer feeder, where Autoreclose may be initiated by the feeder protection but blocked by the transformer protection.

4.3 RESET LOCKOUT

The **Reset Lockout** input can be used to reset the Autoreclose function following lockout. It also resets any Autoreclose alarms, provided that the signals that initiated the lockout have been removed.

4.4 AR AUTO MODE

The **AR Auto Mode** input is used to select the Auto operating mode. In this mode, the Autoreclose function is in service.

4.5 AUTO MODE

The Auto Mode input is used to select the Auto operating mode. In this mode, the Autoreclose function is in service.

4.6 LIVELINE MODE

The *Live Line Mode* input is used to select the Live Line operating mode when Autoreclose is out of service and all blocking of instantaneous protection by Autoreclose is disabled. This operating mode takes precedence over all other operating modes for safety reasons, as it indicates that utility personnel are working near live equipment.

4.7 TELECONTROL MODE

The **Telecontrol** input is used to select the Telecontrol operating mode so that the Auto and Non-auto modes of operation can be selected remotely.

4.8 CIRCUITS OK

The *Circuits OK* signal is a signal indicating the status of the Live Line / Dead Bus or Live Bus / Dead Line system conditions (High = OK, Low = Not OK). The logic required can be derived in the PSL from the Live Line, Dead Line, Live Bus and Dead Bus signals in the System Check logic (if applicable), or it can come from an external source depending on the application.

4.9 AR SYS CHECKS OK (403)

The *AR Sys Checks OK* signal can be mapped from the system checks output *SysChksInactive*, to enable autoreclosing without any system checks, providing the *System Checks* setting in the *CONFIGURATION* column is disabled. This mapping is not essential, because the *No System Checks* setting in the *AUTORECLOSE* column can be enabled to achieve the same effect.

This signal can also be mapped to an opto-input, to allow the IED to receive a signal from an external system monitoring device, indicating that the system conditions are suitable for CB closing. This should not normally be necessary, since the IED has comprehensive built in system check functionality.

4.10 EXT AR PROT TRIP (EXTERNAL AR PROTECTION TRIP)

The Ext AR Prot Trip signal allows Autoreclose initiation by a Trip from a separate protection device.

4.11 EXT AR PROT START (EXTERNAL AR PROTECTION START)

The Ext AR Prot Strt signal allows Autoreclose initiation by a Start from a separate protection device.

4.12 DAR COMPLETE (DELAYED AUTORECLOSE COMPLETE)

Some utilities require Delayed Autoreclose (DAR) functionality.

The *DAR Complete* signal can, if required, be mapped in PSL to provide a short pulse when a CB Close command is given at the end of the dead time. If *DAR Complete* is activated during an Autoreclose cycle, the output signal *DAR in Progress* resets, even though the reclaim time may still be running, and *AR in Progress* remains set until the end of the reclaim time.

For most applications, *DAR complete* can be ignored (not mapped in PSL). In such cases, *DAR in Progress* operates and resets in parallel with *AR in Progress*.

4.13 CB IN SERVICE (CIRCUIT BREAKER IN SERVICE)

The *CB In Service* signal must remain asserted when protection operates if autoreclose is to be initiated. For most applications, it can be mapped to *CB Closed 3ph*. More complex PSL mapping can be programmed if required, for example where it is necessary to confirm not only that the CB is closed but also that the line and/or bus VT is actually live up to the instant of protection operation.

4.14 AR RESTART

In some applications, it is sometimes necessary to initiate an Autoreclose cycle by means of connecting an external signal to an opto-input. This would be when the normal interlock conditions are not all satisfied, i.e. when the CB is open and the associated feeder is dead. If the *AR Restart* input is mapped to an opto-input, activation of that opto-input will initiate an Autoreclose cycle irrespective of the status of the *CB in Service* input, provided the other interlock conditions, are still satisfied.

4.15 DT OK TO START (DEAD TIME OK TO START)

This is an optional extra interlock in the dead time initiation logic. In addition to the CB being open and the protection reset, *DT OK To Start* has to be set high to allow the dead time function to be primed after an AR cycle has started. Once the dead time function is primed, this signal has no further affect – the dead time function stays primed even if the signal subsequently goes low. A typical PSL mapping for this input is from the *Dead Line* signal from the System Check logic. This would enable dead time priming only when the feeder has gone dead after CB tripping. If this extra dead time priming interlock is not required, *DT OK To Start* can be left unmapped, and it will default to a high state.

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4.16 DEADTIME ENABLED

This is an optional interlock in the dead time logic. This signal has to be high to allow the dead time to run. If this signal goes low, the dead time stops and resets, but stays primed, and will restart from zero when it goes high again. A typical PSL mapping is from the *CB Healthy* input or from selected signals from the System Check logic. It could also be mapped to an opto-input to provide a 'hold off' function for the follower CB in a 'master/follower' application with 2 CBs. If this optional interlock is not required, *DeadTime Enabled* can be left unmapped, and it will default to a high state.

4.17 AR INIT TRIPTEST (INITIATE TRIP TEST)

If *AR Init TripTest* is mapped to an opto-input, and that input is activated momentarily, the IED generates a CB trip output via *AR Trip Test*. The default PSL then maps this to output to the trip output relay and initiates an Autoreclose cycle.

4.18 AR SKIP SHOT 1

If **AR Skip Shot 1** is mapped to an opto-input, and that input is activated momentarily, the IED logic will cause the Autoreclose sequence counter to increment by 1. This will decrease the available number of reclose shots and will lockout the re-closer.

4.19 INH RECLAIM TIME (INHIBIT RECLAIM TIME)

If *Inh Reclaim Time* is mapped to an opto-input, and that input is active at the start of the reclaim time, the IED logic will cause the reclaim timers to be blocked.

5 AUTORECLOSE FUNCTION OUTPUTS

The Autoreclose function has several logic outputs, which can be assigned to output relay contacts, monitor bits in the COMMISSION TESTS column, or the PSL. The functions of these outputs are described below.

5.1 AR IN PROGRESS

This signal is present during the complete re-close cycle from the start of protection to the end of the reclaim time or lockout.

5.2 AR IN PROGRESS 1 (DAR IN PROGRESS)

This operates together with the **AR In Progress** signal at the start of Autoreclose. If **DAR Complete** does not operate, **DAR in Progress** remains operated until **AR In Progress** resets at the end of the cycle. If **DAR Complete** goes high during the Autoreclose cycle, **AR in Progress 1** resets.

5.3 SEQUENCE COUNTER STATUS DDB SIGNALS

During each Autoreclose cycle a sequence Counter increments by 1 after each fault trip and resets to zero at the end of the cycle.

- Seq Counter = 0 is set when the counter is at zero
- Seq Counter = 1 is set when the counter is at 1
- Seq Counter = 2 is set when the counter is at 2
- Seq Counter = 3 is set when the counter is at 3
- Seq Counter = 4 is set when the counter is at 4

5.4 SUCCESSFUL CLOSE

The **Successful Close** output indicates that an Autoreclose cycle has been successfully completed. A successful Autoreclose signal is given after the protection has tripped the CB and it has reclosed successfully. The successful Autoreclose output is reset at the next CB trip or from one of the reset lockout methods.

5.5 AR IN SERVICE

The **AR In Service** output indicates whether the Autoreclose is in or out of service. Autoreclose is In Service when the device is in **Auto** mode and Out of Service when in the **Non Auto** and **Live Line** modes.

5.6 BLOCK MAIN PROT (BLOCK MAIN PROTECTION)

The *Block Main Prot* signal blocks the DT-only stages (instantaneous stages) of the main current protection elements. These are *I>3, I>4, I>6, IN1>3, IN1>4, IN2>3,* and *IN2>4.* You block the instantaneous stages for each trip of the Autoreclose cycle using the Overcurrent and Earth Fault 1 and 2 settings, *I> Blocking, IN1> Blocking, IN2> Blocking* and the *Trip 1/2/3/4/5 Main* settings.

5.7 BLOCK SEF PROT (BLOCK SEF PROTECTION)

The **Block SEF Prot** signal blocks the DT-only stages (instantaneous stages) of the SEF protection elements. These are **ISEF>3**, and **ISEF>4**. You block the instantaneous SEF stages for each trip of the Autoreclose cycle using the SEF PROTECTION setting **ISEF> Blocking**, and the **Trip 1/2/3/4/5 SEF** settings.

5.8 RECLOSE CHECKS

The Reclose Checks output indicates that the AR System Checks are in progress.

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5.9 DEADT IN PROG (DEAD TIME IN PROGRESS)

The **Dead T in Prog** output indicates that the dead time is in progress. This signal is set when **Reclose Checks** is set AND input **Dead TimeEnabled** is high. This may be useful during commissioning to check the operation of the Autoreclose cycle.

5.10 DT COMPLETE (DEAD TIME COMPLETE)

DT *Complete* (Dead time complete) operates at the end of the set dead time, and remains operated until either the scheme resets at the end of the reclaim time or a further protection operation or Autoreclose initiation occurs. It can be applied purely as an indication, or included in PSL mapping to logic input *DAR Complete*.

5.11 AR SYNC CHECK (AR SYNCHRONISATION CHECK)

AR Sync Check indicates that the Autoreclose Synchronism checks are satisfactory. This is when either of the synchronisation check modules (CS1 or CS2), confirms an In-Synchronism condition.

5.12 AR SYSCHECKS OK (AR SYSTEM CHECKS OK)

AR SysChecks OK indicates that the Autoreclose System checks are satisfactory. This is when any selected system check condition (synchronism check, live bus/dead line etc.) is confirmed.

This DDB signal ihas the number 463 and is an output from the Autoreclose function (i.e. a PSL input). It should not be confused with DDB signal 403, which is an input to the Autoreclose function (i.e. a PSL output).

5.13 AUTO CLOSE

The **Auto Close** output indicates that the Autoreclose logic has issued a Close signal to the CB. This output feeds a signal to the control close pulse timer and remains on until the CB has closed. This signal may be useful during commissioning to check the operation of the Autoreclose cycle.

5.14 PROTECTION LOCKT (PROTECTION LOCKOUT)

Protection Lockt (Protection Lockout) operates if **AR lockout** is triggered by protection operation either during the inhibit period following a manual CB close or when the device is in **Non-auto** or **Live Line** mode.

5.15 RESET LCKOUT ALM (RESET LOCKOUT ALARM)

Reset Lckout Alm operates when the device is in **Non-auto mode**, if the **Reset Lockout** setting is set to Select Non Auto.

5.16 RECLAIM IN PROG

Reclaim in Prog output indicates that a reclaim timer is in progress and will drop-off once the reclaim timer resets.

5.17 RECLAIM COMPLETE

Reclaim Complete operates at the end of the set reclaim time and is a fast reset. To maintain the output indication a dwell timer has to be implemented in PSL.

6 AUTORECLOSE FUNCTION ALARMS

The following DDB signals will produce an alarm. These are described below.

6.1 AR NO SYS CHECK

The **AR No Sys Check** alarm indicates that the system voltages are not suitable for autoreclosing at the end of the system check time (setting **Sys Check Time**), leading to a lockout condition. This alarm is latched and must be reset manually.

6.2 AR CB UNHEALTHY

The **AR CB Unhealthy** alarm indicates that the **CB Healthy** input was not energised at the end of the **CB Healthy** Time, leading to a lockout condition. This alarm is latched and must be reset manually.

6.3 AR LOCKOUT

The *AR Lockout* alarm indicates that the device is in a lockout status and that further re-close attempts will not be made. This alarm can configured to reset automatically (self-reset) or manually as determined by the setting *Reset Lockout by* in the *CB CONTROL* column.

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7 AUTORECLOSE OPERATION

The Autoreclose function is a complex function consisting of several modules interacting with one another. This is described in terms of separate logic diagrams, which link together by means of Internal signals (depicted by the pink-coloured boxes. To help you with the analysis of the various Autoreclose modules, the following table describes how these internal signals link up in the various logic diagrams. Each internal signal is allocated with an ID, and the diagrams on which they appear are also identified.

Internal signal ID	Input to AR function	Appearing in diagrams	Output from AR function	Appearing in diagrams
1	Autoreclose Disabled	V00505, V00507	Autoreclose Disabled	V00501
2	Live Line Mode	V00505, V00507, V00514	Live Line Mode	V00501
3	Non Auto Mode	V00505, V00507, V00514	Non Auto Mode	V00501
4	Auto Mode (int)	V00505, V00507, V00512	Auto Mode (int)	V00501
5	Main Protection Start	V00504, V00505, V00507, V00511, V00512	Main Protection Start	V00502
6	SEF Protection Start	V00504, V00505, V00511, V00512	SEF Protection Start	V00502
7	Main Protection Trip	V00505, V00513, V00514	Main Protection Trip	V00503
8	SEF Protection Trip	V00505, V00507, V00513, V00514	SEF Protection Trip	V00503
9	Block Autoreclose	V00513	Block Autoreclose	V00515
10	SC Count >= Main Shots	V00504	SC Count >= Main Shots	V00505
11	SC Count >= SEF Shots	V00504	SC Count >= SEF Shots	V00505
12	Main High Shots	V00505, V00513	Main High Shots	V00504
13	SEF High Shots	V00505, V00513	SEF High Shots	V00504
14	Autoreclose Inhibit	V00505, V00507, V00514	Autoreclose Inhibit	V00512
15	Autoreclose Start	V00508, V00509, V00511, V00513	Autoreclose Start	V00505
16	Autoreclose Initiate	V00508, V00513	Autoreclose Initiate	V00505
17	SC Count > 4	V00506	SC Count > 4	V00505
18	Block Main Prot Trips	V00507	Block Main Prot Trips	V00506
19	Block SEF Prot Trips	V00507	Block SEF Prot Trips	V00506
20	Hold Reclaim Output	V00511	Hold Reclaim Output	V00509

External DDB signals

Some of the External DDB signal names may vary slightly between products. The following table shows equivalence of these variations.

DDB Signal Number	Variation 1	Variation 2
240	AR LiveLine Mode	Live Line Mode
241	AR Auto Mode	Auto Mode
358	AR Blk Main Prot	Block Main Prot
359	AR BIk SEF Prot	Block SEF Prot
362	AR SeqCounter 0	Seq Counter = 0
363	AR SeqCounter 1	Seq Counter = 1
364	AR SeqCounter 2	Seq Counter = 2
365	AR SeqCounter 3	Seq Counter = 3
366	AR SeqCounter 4	Seq Counter = 4
368	DeadTime in Prog	Dead T in Prog
403	AR Sys Checks	AR Sys Checks OK

DDB Signal Number	Variation 1	Variation 2
456	DAR In Progress	AR In Progress 1
461	LiveDead Ccts OK	Circuits OK

7.1 OPERATING MODES

The Autoreclose function has three operating modes:

- Auto Mode: Autoreclose is in service
- Non-auto Mode: Autoreclose is out of service AND the chosen protection functions are blocked if setting AR
 Deselected = Block Inst Prot.
- Live Line Mode: Autoreclose is out of service, but protection functions are NOT blocked, even if setting AR
 Deselected = Block Inst Prot.

Note:

Live Line Mode provides extra security for live line working on the protected feeder.

The Autoreclose function must first be enabled in the *CONFIGURATION* column. You can then select the operating mode according to application requirements. The basic method of mode selection is determined by the setting *AR Mode Select* in the *AUTORECLOSE* column, as summarised in the following table:

AR Mode Select Setting	Description
Command Mode	Auto or Non-auto mode selection is determined by the command cell <i>Autoreclose Mode</i> in the <i>CB CONTROL</i> column.
Opto Set Mode	Auto or Non-auto mode selection is determined by an opto-input mapped to AR Auto Mode If the AR Auto Mode input is high, Auto operating mode is selected. If the AR Auto Mode input is low, Non-Auto operating mode is selected.
User Set Mode	Auto or Non-auto mode selection is controlled by the <i>Telecontrol Mode</i> input. If the <i>Telecontrol Mode</i> input is high, the setting <i>Autoreclose Mode</i> in the <i>CB CONTROL</i> column is used to select Auto or Non Auto operating mode. If the <i>Telecontrol Mode</i> input is low, it behaves as for the <i>Opto Set Mode</i> setting.
Pulse Set Mode	Auto or Non-auto mode selection is determined by the falling edge of <i>AR Auto Mode</i> signal. If the Telecontrol input is high, the operating mode is toggled between Auto and Non Auto Mode on the falling edge of the <i>AR Auto Mode</i> signal as it goes low. The Auto Mode pulses are produced by the SCADA system. If the Telecontrol input is low, it behaves as for the <i>Opto Set Mode</i> setting.

The Live Line Mode is controlled by **AR LiveLine Mode**. If this is high, the scheme is forced into Live Line Mode irrespective of the other signals.

7.1.1 FOUR-POSITION SELECTOR SWITCH IMPLEMENTATION

It is quite common for some utilities to apply a four position selector switch to control the mode of operation. This application can be implemented using the DDB signals **AR LiveLine Mode**, **AR Auto Mode** and **Telecontrol Mode**. This is demonstrated in the following diagram.

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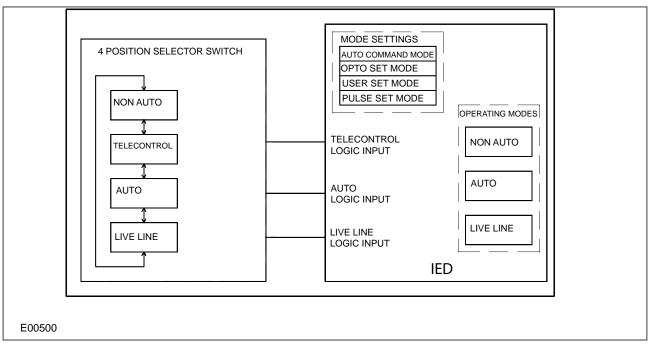


Figure 157: Four-position selector switch implementation

The required logic truth table for this arrangement is as follows:

Switch position	AR Auto Mode	Telecontrol Mode	AR Live Line Mode
Non-auto	0	0	0
Telecontrol	0 or SCADA pulse	1	0
Auto	1	0	0
Live Line	0	0	1

V00501

Auto-Reclose Autoredose disabled Disable Enable Live Line Mode (int) AR LiveLine Mode AR Mode Select Opto Set Mode & User Set Mode Non Auto Mode & Pulse Set Mode & Command Mode Auto Mode (int) Autoreclose Mode & Auto No Operation Non Auto Output pulse on rising edge of 'Tele & Enable Output pulse on AR Auto Mode

7.1.2 OPERATING MODE SELECTION LOGIC

Figure 158: Autoreclose mode select logic

Telecontrol Mode

The mode selection logic includes a 100 ms delay for *Auto Mode, Telecontrol* and *Live Line* logic inputs, to ensure a predictable change of operating modes. This is of particular importance for the case when the four position switch does not have 'make-before-break' contacts. The logic also ensures that when the switch is moved from Auto or Non-Auto position to Telecontrol, the scheme remains in the previously selected mode (Auto or Non-Auto) until a different mode is selected by remote control.

For applications where live line operating mode and remote selection of Auto/Non-auto modes are not required, a simple two position switch can be arranged to activate **Auto Mode** input. In this case, the **Live Line** and **Telecontrol** inputs would be unused.

7.2 AUTORECLOSE INITIATION

Autoreclose is usually initiated from the IED's internal protection function. Different stages of phase overcurrent and earth fault protection can be programmed to initiate or block the main Autoreclose function. The stages of sensitive earth fault protection can also be programmed to initiate or block both the Main Autoreclose function or the SEF Autoreclose function.

The associated settings are found in the AUTORECLOSE column under the sub-heading AR INITIATION.

For example:

If I>1 AR is set to Initiate Main AR, operation of the I>1 protection stage will initiate Autoreclose

If *ISEF>1 AR* is set to *No* Action, operation of the *ISEF>1* protection stage will lead to a CB trip but no reclose. Otherwise it can be used to initiate Main autoreclose or SEF autoreclose.

Note:

A selection must be made for each protection stage that is enabled.

A separate protection device may also initiate Autoreclose. The Autoreclose can be initiated from a protection Trip, or when sequence coordination is required from a protection Start. If external triggering of Autoreclose is required, the following DDB signals should be mapped to opto-inputs:

- Ext AR Prot Trip
- Ext AR Prot Strt (if applicable)

In addition, the setting *Ext Prot* should be set to *Initiate Main AR*.

Although a protection start and a protection trip can initiate an AR cycle, several checks still have to be performed before the initialisation signal is given. Some of the checks are listed below:

- Auto Mode has been selected
- Live line mode is disabled
- The number of main protection and SEF shots have not been reached
- Sequence co-ordination is enabled (for protection start to initiate AR. This is not necessary if a protection trip is doing the initiating)
- The CB Ops Lockout DDB signal is not set
- The CB in Service DDB signal is high

Note

The relevant protection trip must be mapped to the **Trip Command In** DDB.

7.2.1 START SIGNAL LOGIC

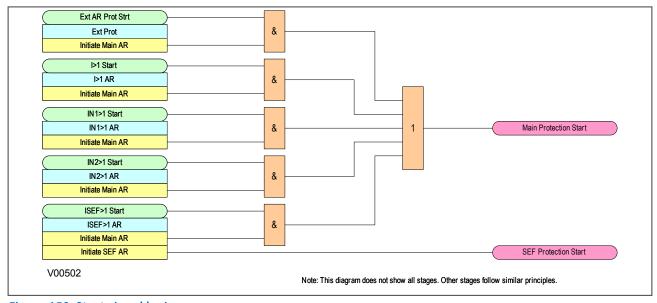


Figure 159: Start signal logic

7.2.2 TRIP SIGNAL LOGIC

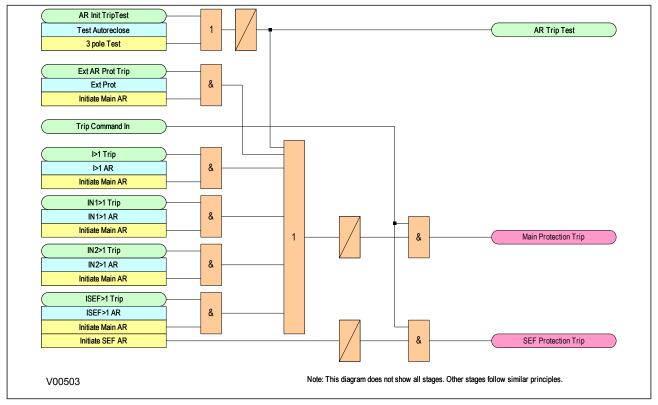


Figure 160: Trip signal logic

7.2.3 BLOCKING SIGNAL LOGIC

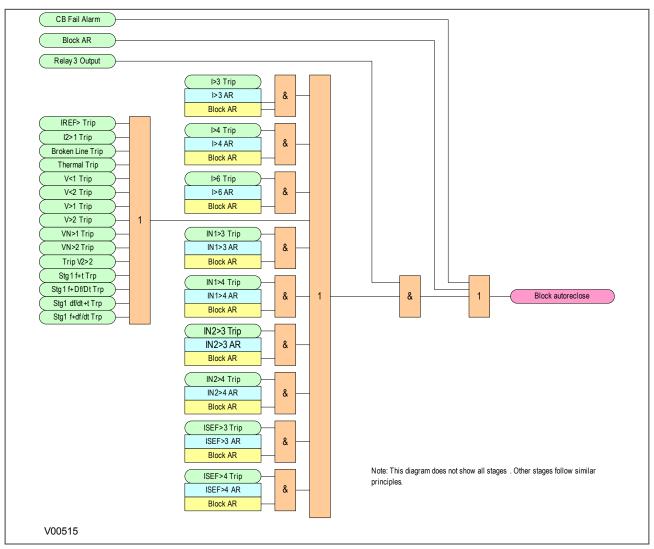


Figure 161: Blocking signal logic

7.2.4 SHOTS EXCEEDED LOGIC

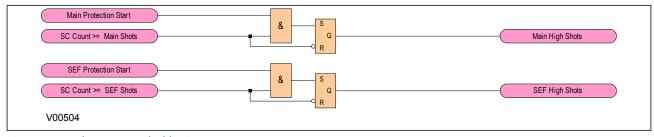


Figure 162: Shots Exceeded logic

7.2.5 AR INITIATION LOGIC

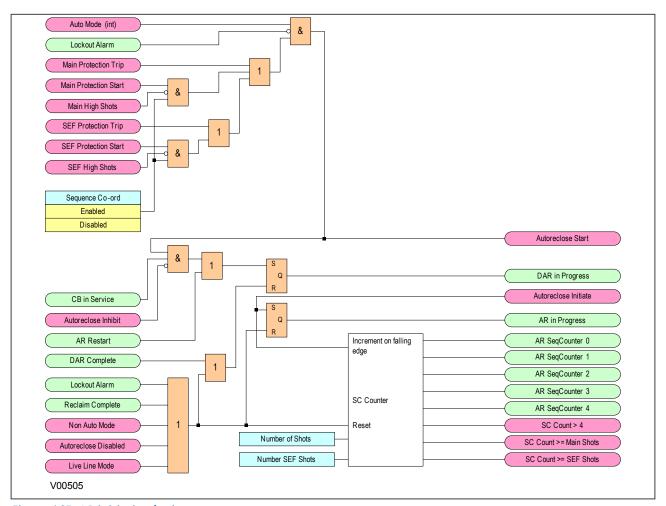


Figure 163: AR initiation logic

7.3 BLOCKING INSTANTANEOUS PROTECTION FOR SELECTED TRIPS

Instantaneous protection may be blocked or not blocked for each trip in an Autoreclose cycle. This is selected using the *Trip (n) Main* and *Trip (n) SEF* settings, where n is the number of the trip in the autoreclose cycle. These allow the instantaneous elements of phase, earth fault and SEF protection to be selectively blocked for a CB trip sequence. For example, if *Trip 1 Main* is set to *No Block* and *Trip 2 Main* is set to *Block Inst Prot*, the instantaneous elements of the phase and earth fault protection will be available for the first trip but blocked afterwards for the second trip during the Autoreclose cycle. The logic for this is shown below.

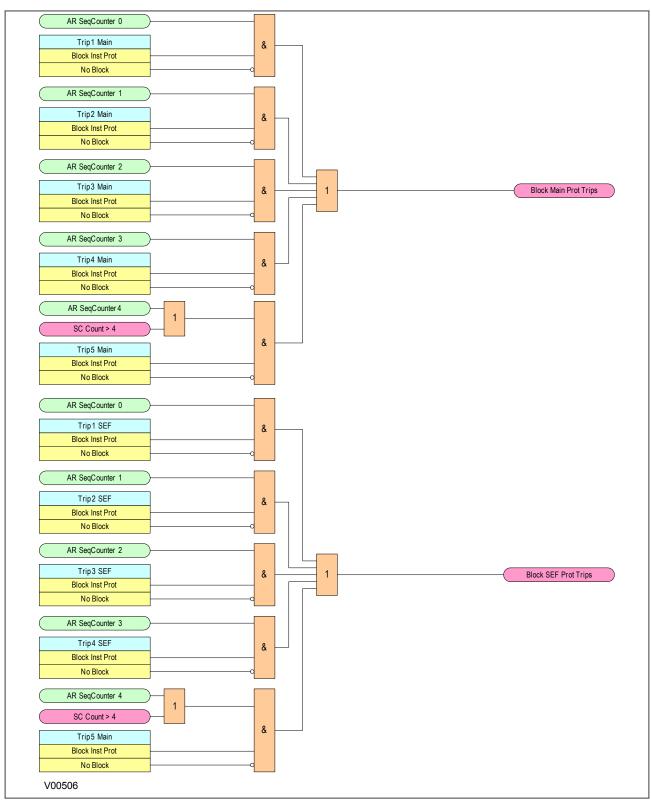


Figure 164: Blocking instantaneous protection for selected trips

7.4 BLOCKING INSTANTANEOUS PROTECTION FOR LOCKOUTS

Instantaneous protection can also be blocked for certain lockout conditions:

It is blocked when the CB maintenance lockout counter or excessive fault frequency lockout has reached its penultimate value.

For example, if the setting **No. CB Ops Lock** in the **CB MONITOR SETUP** column is set to 100 and the **No. CB Ops Maint** = '99', the instantaneous protection can be blocked to ensure that the last CB trip before lockout will be due to discriminative protection operation. This is controlled using the **EFF Maint Lock** setting (Excessive Fault Frequency maintenance lockout). If this is set to **Block Inst Prot**, the instantaneous protection will be blocked for the last CB Trip before lockout occurs.

Instantaneous protection can also be blocked when the IED is locked out, using the **AR Lockout** setting. It can also be blocked after a manual close using the **Manual Close** setting. When the IED is in the Non-auto mode it can be blocked by using the **AR Deselected** setting. The logic for these features is shown below.

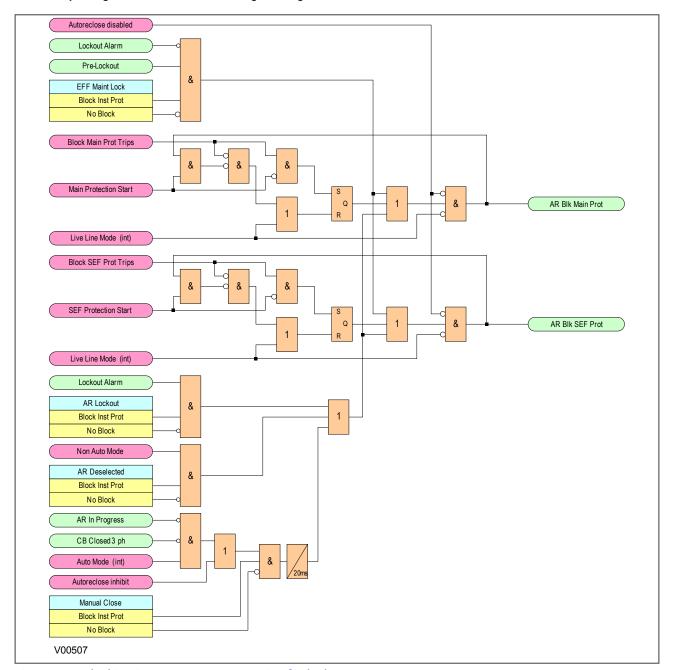


Figure 165: Blocking instantaneous protection for lockouts

7.5 DEAD TIME CONTROL

When the setting *CS AR Immediate* is enabled, immediate re-closure of the circuit breaker is allowed providing that both sides of the circuit breaker are live and in synchronism at any time after the dead time has started. This allows for quicker load restoration, as it is not necessary to wait for the full dead time to expire.

If **CS AR Immediate** is disabled, or neither Line nor Bus are live, the dead timer will continue to run, if the **DeadTime Enabled** signal is high. The **DeadTime Enabled** function could be mapped to an opto-input to indicate that the circuit breaker is healthy. Mapping the **DeadTime Enabled** function in PSL increases the flexibility by allowing it to be triggered by other conditions such as Live Line/Dead Bus. If **DeadTime Enabled** is not mapped in PSL, it defaults to high, so the dead time can run.

The dead time control logic is shown below.

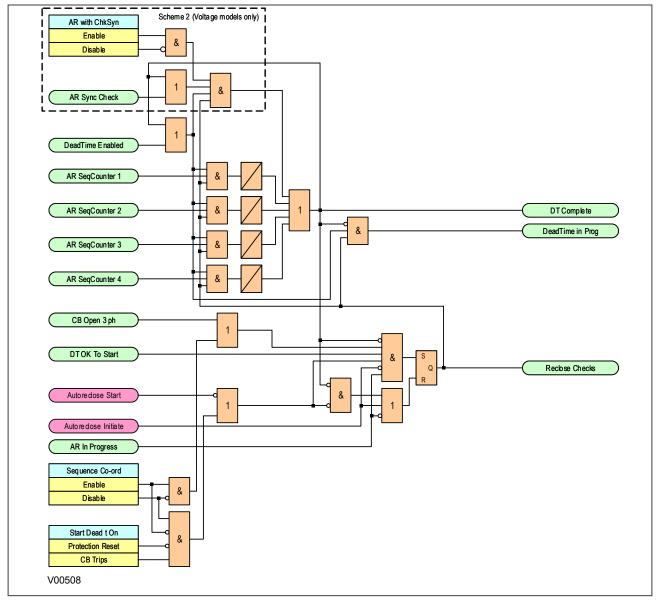


Figure 166: Dead Time Control logic

7.5.1 AR CB CLOSE CONTROL

Once the dead time is completed or a synchronism check is confirmed, the **Auto Close** signal is given, provided both the **CB Healthy** and the **System Checks** are satisfied. The **Auto Close** signal triggers a CB Close command via the CB Control functionality.

The AR CB Close Control Logic is as follows:

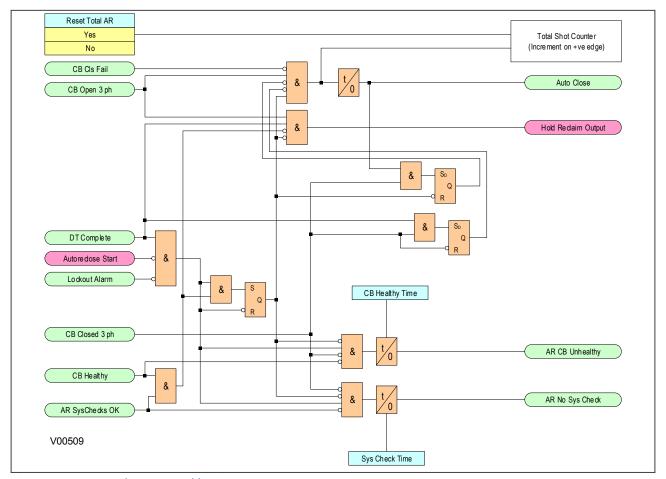


Figure 167: AR CB Close Control logic

7.6 AR SYSTEM CHECKS

The permission to initiate an Autoreclose depends on the following AR system check settings. These are found in the *AUTORECLOSE* column under the *AR SYSTEM CHECKS* sub-heading and are not to be confused with the main system check settings in the *SYSTEM CHECKS* column.

The AR SYSTEM CHECKS are as follows:

- Live/Dead Ccts: When enabled this setting will give an AR Check OK signal when the LiveDead Ccts OK
 signal is high. This logic input DDB would normally be mapped in PSL to appropriate combinations of Line
 Live, Line Dead, Bus Live and Bus Dead DDB signals.
- **No System Checks**: When enabled this setting completely disables system checks thus allowing Autoreclose initiation under any system conditions.
- SysChk on Shot 1: Can be used to disable system checks on the first AR shot.
- AR with ChkSyn: Only allows Autoreclose when the system satisfies the Check Sync Stage 1 (CS1) settings in the main SYSTEM CHECKS menu.
- AR with SysSyn: Only allows Autoreclose when the system satisfies the Check Sync Stage 2 (CS2) settings in the main SYSTEM CHECKS menu.



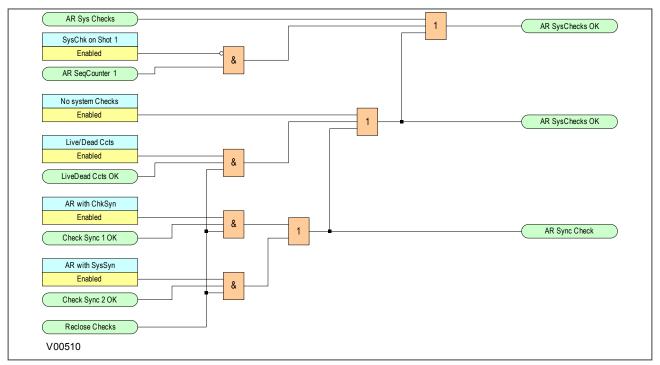


Figure 168: AR System Check logic

7.7 RECLAIM TIMER INITIATION

The $tReclaim\ Extend$ setting allows you to control whether the timer is suspended from the protection start contacts or not. When a setting of $No\ Operation$ is used, the reclaim timer operates from the instant the CB is closed and will continue until the timer expires. The $Reclaim\ Time$ must therefore be set in excess of the timedelayed protection operating time, to ensure that the protection can operate before the Autoreclose function is reset.

For certain applications it is advantageous to set **tReclaim Extend** to On Prot Start. This facility allows the operation of the reclaim timer to be suspended after CB re-closure by a signal from the main protection start or SEF protection start signals. This feature ensures that the reclaim time cannot time out and reset the Autoreclose before the time delayed protection has operated.

Since the reclaim timer will be suspended, it is unnecessary to use a timer setting in excess of the protection operating time, therefore a short reclaim time can be used. Short reclaim time settings can help to prevent unnecessary lockout for a succession of transient faults in a short period, for example during a thunderstorm.

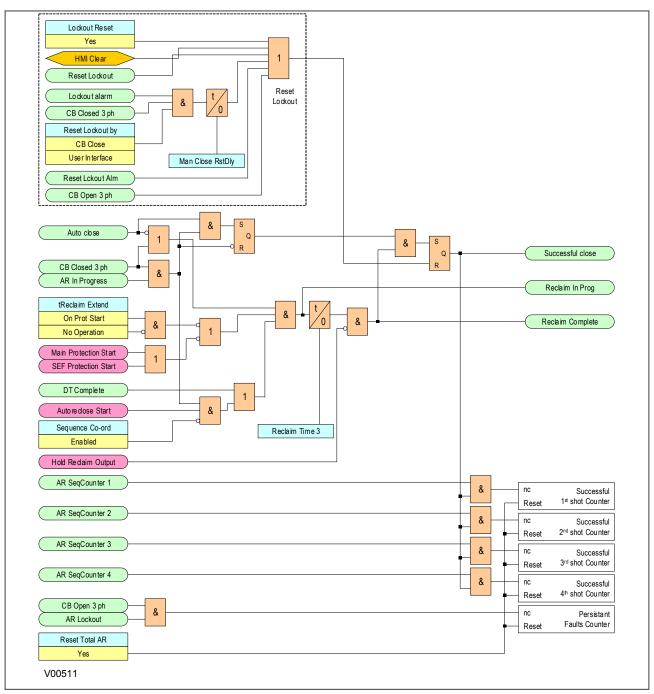


Figure 169: Reclaim Time logic

7.8 AUTORECLOSE INHIBIT

To ensure that autoreclosing is not initiated for a manual CB closure on to a pre-existing fault (switch on to fault), the **AR on Man Close** setting can be set to Inhibited. With this setting, Autoreclose initiation is inhibited for a period equal to setting **AR Inhibit Time** following a manual CB closure. The logic for AR Inhibit is as follows:

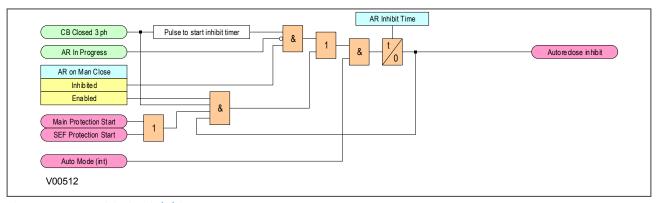


Figure 170: AR Initiation inhibit

If a protection operation occurs during the inhibit period, Autoreclose is not initiated. A further option is provided by setting Man Close on Flt. If this is set to Lockout, Autoreclose is locked out (AR Lockout) for a fault during the inhibit period following manual CB closure. If Man Close on Flt is set to No Lockout, the CB trips without reclosure, but Autoreclose is not locked out.

You may need to block selected fast non-discriminating protection in order to obtain fully discriminative tripping during the AR initiation inhibit period following CB manual close. You can do this by setting *Manual Close* to Block Inst Prot. A No Block setting will enable all protection elements immediately on CB closure.

If setting **AR on Man Close** is set to *Enabled*, Autoreclose can be initiated immediately on CB closure, and settings **AR Inhibit Time**, **Man Close on Flt** and **Manual Close** are irrelevant.

7.9 AUTORECLOSE LOCKOUT

If protection operates during the reclaim time following the final reclose attempt, the IED is driven to lockout and the Autoreclose function is disabled until the lockout condition is reset. This produces the alarm, **AR Lockout**. The **Block AR** input blocks Autoreclose and causes a lockout if Autoreclose is in progress.

Autoreclose lockout can also be caused by the CB failing to close due to an unhealthy circuit breaker (CB springs not charged or low gas pressure) or if there is no synchronisation between the system voltages. These two conditions are indicated by the alarms *CB Unhealthy* and *AR No Sys Check* This is shown in the AR Lockout logic diagram as follows:

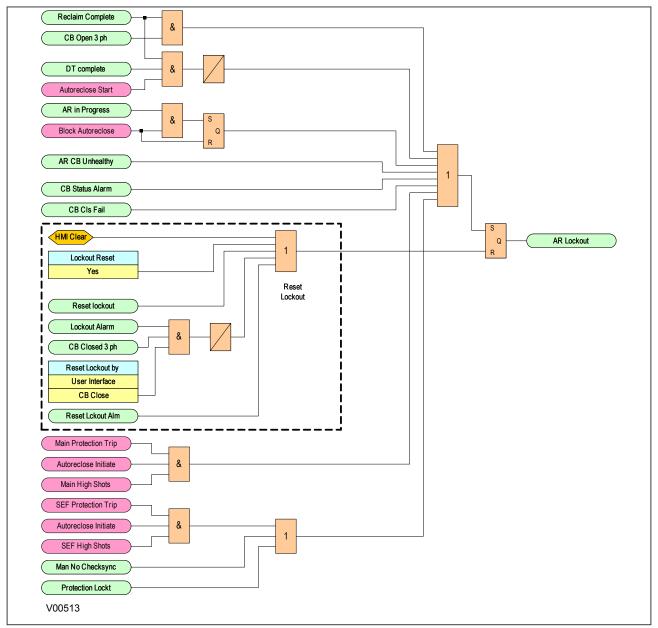


Figure 171: Overall Lockout logic

AR lockout may also be due to a protection operation when the IED is in the Live Line or Non-auto modes when the setting $Trip\ AR\ Inactive$ is set to Lockout. Autoreclose lockout can also be caused by a protection operation after manual closing during the $AR\ Inhibit\ Time$ when the $Man\ Close\ on\ Flt$ setting is set to Lockout. This is shown as follows:

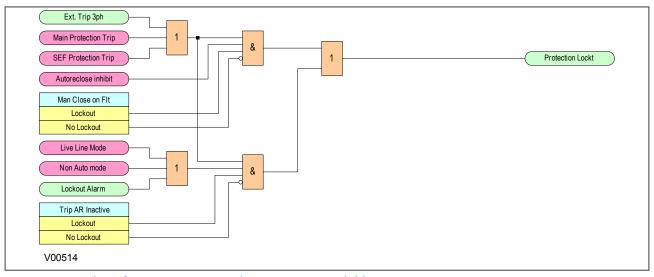


Figure 172: Lockout for protection trip when AR is not available

Note:

Lockout can also be caused by the CB condition monitoring functions in the CB MONITOR SETUP column.

The **Reset Lockout** input can be used to reset the Autoreclose function following lockout and reset any Autoreclose alarms, provided that the signals that initiated the lockout have been removed. Lockout can also be reset from the clear key or the command **Lockout Reset** from the CB CONTROL column.

There are two different *Reset Lockout by* settings. One in the *CB CONTROL* column and one in the *AUTORECLOSE* column.

The **Reset Lockout by** setting in the *CB CONTROL* column is used to enable or disable reset of lockout automatically from a manual close after the manual close time **Man Close RstDly**.

The **Reset Lockout by** setting in the AUTORECLOSE column is used to enable/disable the resetting of lockout when the IED is in the Non-auto operating mode. The reset lockout methods are summarised in the following table:

Reset Lockout Method	When Available?
User Interface via the Clear key. Note: This will also reset all other protection flags	Always
User interface via CB CONTROL command Lockout Reset	Always
Opto-input Reset lockout Always	
Following a successful manual close if CB CONTROL setting Reset Lockout by is set to CB Close	Only when set
By selecting Non-Auto mode, provided AUTORECLOSE setting Reset Lockout by is set to Select NonAuto	Only when set

7.10 SEQUENCE CO-ORDINATION

The **Sequence Co-ord** setting in the AUTORECLOSE menu allows sequence co-ordination with other protection devices, such as downstream pole-mounted reclosers.

The main protection start or SEF protection start signals indicate when fault current is present, advance the sequence count by one and start the dead time, whether the CB is open or closed. When the dead time is complete and the protection start inputs are low, the reclaim timer is initiated.

You should program both the upstream and downstream Autoreclose IEDs with the same number of shots to lockout and number of instantaneous trips before instantaneous protection is blocked. This will ensure that for a persistent downstream fault, both Autoreclose IEDs will be on the same sequence count and will block

instantaneous protection at the same time. When sequence co-ordination is disabled, the circuit breaker has to be tripped to start the dead time, and the sequence count is advanced by one.

When using sequence co-ordination for some applications such as downstream pole-mounted reclosers, it may be desirable to re-enable instantaneous protection when the recloser has locked out. When the downstream recloser has locked out there is no need for discrimination. This allows you to have instantaneous, then IDMT, then instantaneous trips again during an Autoreclose cycle. Instantaneous protection may be blocked or not blocked for each trip in an Autoreclose cycle using the *Trip (n) Main* and *Trip (n) SEF* settings, where n is the number of the trip in the autoreclose cycle.

7.11 SYSTEM CHECKS FOR FIRST RECLOSE

The **SysChk on Shot 1** setting in the SYSTEM CHECKS sub menu of the AUTORECLOSE column is used to enable or disable system checks for the first reclose attempt in an Autoreclose cycle. This may be preferred when high speed Autoreclose is applied, to avoid the extra time for a synchronism check. Subsequent reclose attempts in a multishot cycle will, however, still require a synchronism check.

8 SETTING GUIDELINES

8.1 NUMBER OF SHOTS

There are no clear cut rules for defining the number of shots for a particular application. Generally medium voltage systems use only two or three shot Autoreclose schemes. However, in certain countries, for specific applications, a four-shot scheme is used. A four-shot scheme has the advantage that the final dead time can be set sufficiently long to allow any thunderstorms to pass before reclosing for the final time. This arrangement prevents unnecessary lockout for consecutive transient faults.

Typically, the first trip, and sometimes the second, will result from instantaneous protection. Since most faults are transient, the subsequent trips will be time delayed, all with increasing dead times to clear semi-permanent faults.

An important consideration is the ability of the circuit breaker to perform several trip-close operations in quick succession and the affect of these operations on the circuit maintenance period.

On EHV transmission circuits with high fault levels, only one re-closure is normally applied, because of the damage that could be caused by multiple re-closures.

8.2 DEAD TIMER SETTING

The choice of dead time is dependent on the system. The main factors that can influence the choice of dead time are:

- Stability and synchronism requirements
- Operational convenience
- Load
- The type of circuit breaker
- Fault deionising time
- The protection reset time

8.2.1 STABILITY AND SYNCHRONISM REQUIREMENTS

It may be that the power transfer level on a specific feeder is such that the systems at either end of the feeder could quickly fall out of synchronism if the feeder is opened. If this is the case, it is usually necessary to reclose the feeder as quickly as possible to prevent loss of synchronism. This is called high speed autoreclosing (HSAR). In this situation, the dead time setting should be adjusted to the minimum time necessary. This time setting should comply with the minimum dead time limitations imposed by the circuit breaker and associated protection, which should be enough to allow complete deionisation of the fault path and restoration of the full voltage withstand level. Typical HSAR dead time values are between 0.3 and 0.5 seconds.

On a closely interconnected transmission system, where alternative power transfer paths usually hold the overall system in synchronism even when a specific feeder opens, or on a radial supply system where there are no stability implications, it is often preferred to leave a feeder open for a few seconds after fault clearance. This allows the system to stabilise, and reduces the shock to the system on re-closure. This is called slow or delayed autoreclosing (DAR). The dead time setting for DAR is usually selected for operational convenience.

8.2.2 OPERATIONAL CONVENIENCE

When HSAR is not required, the dead time chosen for the first re-closure following a fault trip is not critical. It should be long enough to allow any resulting transients resulting to decay, but not so long as to cause major inconvenience to consumers who are affected by the loss of the feeder. The setting chosen often depends on service experience with the specific feeder.

Typical first shot dead time settings on 11 kV distribution systems are 5 to 10 seconds. In situations where two parallel circuits from one substation are carried on the same towers, it is often arranged for the dead times on the

two circuits to be staggered, e.g. one at 5 seconds and the other at 10 seconds, so that the two circuit breakers do not reclose simultaneously following a fault affecting both circuits.

For multi-shot Autoreclose cycles, the second shot and subsequent shot dead times are usually longer than the first shot, to allow time for semi-permanent faults to burn clear, and for the CB to recharge. Typical second and third shot dead time settings are 30 seconds and 60 seconds respectively.

8.2.3 LOAD REQUIREMENTS

Some types of electrical load might have specific requirements for minimum and/or maximum dead time, to prevent damage and minimise disruption. For example, synchronous motors are only capable of tolerating extremely short supply interruptions without losing synchronism. In practise it is desirable to disconnect the motor from the supply in the event of a fault; the dead time would normally be sufficient to allow a controlled shutdown. Induction motors, on the other hand, can withstand supply interruptions up to typically 0.5 seconds and reaccelerate successfully.

8.2.4 CIRCUIT BREAKER

For HSAR, the minimum dead time of the power system will depend on the minimum time delays imposed by the circuit breaker during a tripping and reclose operation.

After tripping, time must be allowed for the mechanism to reset before applying a closing pulse, otherwise the circuit breaker might fail to close correctly. This resetting time will vary depending on the circuit breaker, but is typically 0.1 seconds.

Once the mechanism has reset, a CB Close signal can be applied. The time interval between energising the closing mechanism and making the contacts is called the closing time. A solenoid closing mechanism may take up to 0.3 seconds. A spring-operated breaker, on the other hand, can close in less than 0.1 seconds.

Where HSAR is required, for the majority of medium voltage applications, the circuit breaker mechanism reset time itself dictates the minimum dead time. This would be the mechanism reset time plus the CB closing time. A solenoid mechanism is not suitable for high speed Autoreclose as the closing time is generally too long.

For most circuit breakers, after one reclosure, it is necessary to recharge the closing mechanism energy source before a further reclosure can take place. Therefore the dead time for second and subsequent shots in a multi-shot sequence must be set longer than the spring or gas pressure recharge time.

8.2.5 FAULT DE-IONISATION TIME

For HSAR, the fault deionising time may be the most important factor when considering the dead time. This is the time required for ionised air to disperse around the fault position so that the insulation level of the air is restored. You cannot accurately predict this, but you can obtain an approximation from the following formula:

Deionising time = (10.5 + ((system voltage in kV)/34.5)))/frequency

Examples:

At 66 kV 50 Hz, the deionising time is approximately 0.25 s

At 132 kV 60 Hz, the deionising time is approximately 0.29 s

8.2.6 PROTECTION RESET TIME

It is essential that any time-graded protection fully resets during the dead time, so that correct time discrimination will be maintained after reclosing on to a fault. For HSAR, instantaneous reset of protection is required. However at distribution level, where the protection is predominantly made up of overcurrent and earth fault devices, the protection reset time may not be instantaneous. In the event that the circuit breaker recloses on to a fault and the protection has not fully reset, discrimination may be lost with the downstream protection. To avoid this condition the dead time must be set in excess of the slowest reset time of either the local device or any downstream protection.

Typical 11/33 kV dead time settings are as follows:

1st dead time = 5 - 10 seconds

2nd dead time = 30 seconds

3rd dead time = 60 - 180 seconds

4th dead time = 1 - 30 minutes

8.3 RECLAIM TIMER SETTING

A number of factors influence the choice of the reclaim timer:

- Supply continuity: Large reclaim times can result in unnecessary lockout for transient faults.
- Fault incidence/Past experience: Small reclaim times may be required where there is a high incidence of lightning strikes to prevent unnecessary lockout for transient faults.
- Spring charging time: For HSAR the reclaim time may be set longer than the spring charging time to ensure there is sufficient energy in the circuit breaker to perform a trip-close-trip cycle. For delayed Autoreclose there is no need as the dead time can be extended by an extra CB healthy check window time if there is insufficient energy in the CB. If there is insufficient energy after the check window time the IED will lockout.
- Switchgear maintenance: Excessive operation resulting from short reclaim times can mean shorter maintenance periods. A minimum reclaim time of more than 5 seconds may be needed to allow the circuit breaker time to recover after a trip and close before it can perform another trip-close-trip cycle. This time will depend on the circuit breaker's duty rating.

The reclaim time must be long enough to allow any time-delayed protection initiating Autoreclose to operate. Failure to do so would result in premature resetting of the Autoreclose scheme and re-enabling of instantaneous protection. If this condition arose, a permanent fault would effectively look like a number of transient faults, resulting in continuous autoreclosing, unless additional measures are taken such as excessive fault frequency lockout protection.

Sensitive earth fault protection is applied to detect high resistance earth faults and usually has a long time delay, typically 10 - 15 seconds. This longer time may have to be taken into consideration, if autoreclosing from SEF protection. High resistance earth faults are rarely transient and may be a danger to the public. It is therefore common practise to block Autoreclose by operation of sensitive earth fault protection and lockout the circuit breaker.

A typical 11/33 kV reclaim time is 5 - 10 seconds. This prevents unnecessary lockout during thunderstorms. However, reclaim times of up to 60 - 180 seconds may be used elsewhere in the world.

CHAPTER 14

MONITORING AND CONTROL

1 CHAPTER OVERVIEW

As well as providing a range of protection functions, the product includes comprehensive monitoring and control functionality.

This chapter contains the following sections:

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2 EVENT RECORDS

General Electric devices record events in an event log. This allows you to establish the sequence of events that led up to a particular situation. For example, a change in a digital input signal or protection element output signal would cause an event record to be created and stored in the event log. This could be used to analyse how a particular power system condition was caused. These events are stored in the IED's non-volatile memory. Each event is time tagged.

The event records can be displayed on an IED's front panel but it is easier to view them through the settings application software. This can extract the events log from the device and store it as a single .evt file for analysis on a PC.

The event records are detailed in the VIEW RECORDS column. The first event (0) is always the latest event. After selecting the required event, you can scroll through the menus to obtain further details.

If viewing the event with the settings application software, simply open the extracted event file. All the events are displayed chronologically. Each event is summarised with a time stamp (obtained from the *Time & Date* cell) and a short description relating to the event (obtained from the *Event Text* cell. You can expand the details of the event by clicking on the + icon to the left of the time stamp.

The following table shows the correlation between the fields in the setting application software's event viewer and the cells in the menu database.

Field in Event Viewer	Equivalent cell in menu DB	Cell reference	User settable?
Left hand column header	VIEW RECORDS → Time & Date	01 03	No
Right hand column header	VIEW RECORDS → Event Text	01 04	No
Description	SYSTEM DATA → Description	00 04	Yes
Plant reference	SYSTEM DATA → Plant Reference	00 05	Yes
Model number	SYSTEM DATA → Model Number	00 06	No
Address	Displays the Courier address relating to the event	N/A	No
Event type	VIEW RECORDS → Menu Cell Ref	01 02	No
Event Value	VIEW RECORDS → Event Value	01 05	No
Evt Unique Id	VIEW RECORDS → Evt Unique ID	01 FE	No

The **Select Event** setting allows access to individual event records, with the latest event stored at position 0. This setting also defines the maximum number of records available.

In addition to the event log, there are two logs which contain duplicates of the last 5 maintenance records and the last 5 fault records. The purpose of this is to provide convenient access to the most recent fault and maintenance events.

2.1 EVENT TYPES

There are several different types of event:

- Opto-input events (Change of state of opto-input)
- Contact events (Change of state of output relay contact)
- Alarm events
- Fault record events
- Standard events
- Security events

Standard events are further sub-categorised internally to include different pieces of information. These are:

- Protection events (starts and trips)
- Maintenance record events
- Platform events

Note:

The first event in the list (event 0) is the most recent event to have occurred.

2.1.1 OPTO-INPUT EVENTS

If one or more of the opto-inputs has changed state since the last time the protection algorithm ran (which runs at several times per cycle), a new event is created, which logs the logic states of all opto-inputs. You can tell which opto-input has changed state by comparing the new event with the previous one.

The description of this event type, as shown in the **Event Text** cell is always Logic Inputs # where # is the batch number of the opto-inputs. This is '1', for the first batch of opto-inputs and '2' for the second batch of opto-inputs (if applicable).

The event value shown in the *Event Value* cell for this type of event is a binary string. This shows the logical states of the opto-inputs, where the Least Significant Bit (LSB), on the right corresponds to the first opto-input *Input L1*.

The same information is also shown in the *Opto I/P Status* cell in the *SYSTEM DATA* column. This information is updated continuously, whereas the information in the event log is a snapshot at the time when the event was created.

2.1.2 CONTACT EVENTS

If one or more of the output relays (also known as output contacts) has changed state since the last time the protection algorithm ran (which runs at several times per cycle), a new event is created, which logs the logic states of all output relays. You can tell which output relay has changed state by comparing the new event with the previous one.

The description of this event type, as shown in the *Event Text* cell is always *Output Contacts #* where # is the batch number of the output relay contacts. This is '1', for the first batch of output contacts and '2' for the second batch of output contacts (if applicable).

The event value shown in the **Event Value** cell for this type of event is a binary string. This shows the logical states of the output relays, where the LSB (on the right) corresponds to the first output contact Output R1.

The same information is also shown in the *Relay O/P Status* cell in the *SYSTEM DATA* column. This information is updated continuously, whereas the information in the event log is a snapshot at the time when the event was created.

2.1.3 ALARM EVENTS

The IED monitors itself on power up and continually thereafter. If it notices any problems, it will register an alarm event.

The description of this event type, as shown in the **Event Text** cell is cell dependent on the type of alarm and will be one of those shown in the following tables, followed by OFF or ON.

The event value shown in the **Event Value** cell for this type of event is a 32 bit binary string. There are one or more banks 32 bit registers, depending on the device model. These contain all the alarm types and their logic states (ON or OFF).

The same information is also shown in the *Alarm Status (n)* cells in the *SYSTEM DATA* column. This information is updated continuously, whereas the information in the event log is a snapshot at the time when the event was created.

2.1.4 FAULT RECORD EVENTS

An event record is created for every fault the IED detects. This is also known as a fault record.

The event type description shown in the *Event Text* cell for this type of event is always *Fault Recorded*.

The IED contains a separate register containing the latest fault records. This provides a convenient way of viewing the latest fault records and saves searching through the event log. You access these fault records using the **Select Fault** setting, where fault number 0 is the latest fault.

A fault record is triggered by the *Fault REC TRIG* signal DDB, which is assigned in the PSL. The fault recorder records the values of all parameters associated with the fault for the duration of the fault. These parameters are stored in separate Courier cells, which become visible depending on the type of fault.

The fault recorder stops recording only when:

The Start signal is reset AND the undercurrent is ON OR the Trip signal is reset, as shown below:

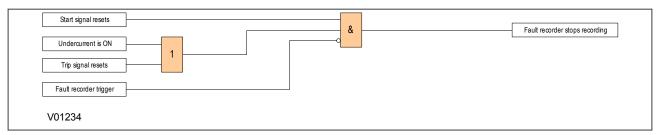


Figure 173: Fault recorder stop conditions

The event is logged as soon as the fault recorder stops. The time stamp assigned to the fault corresponds to the start of the fault. The timestamp assigned to the fault record event corresponds to the time when the fault recorder stops.

Note:

We recommend that you do not set the triggering contact to latching. This is because if you use a latching contact, the fault record would not be generated until the contact has been fully reset.

2.1.5 MAINTENANCE EVENTS

Internal failures detected by the self-test procedures are logged as maintenance records. Maintenance records are special types of standard events.

The event type description shown in the *Event Text* cell for this type of event is always *Maint Recorded*.

The **Event Value** cell also provides a unique binary code.

The IED contains a separate register containing the latest maintenance records. This provides a convenient way of viewing the latest maintenance records and saves searching through the event log. You access these fault records using the *Select Maint* setting.

The maintenance record has a number of extra menu cells relating to the maintenance event. These parameters are *Maint Text*, *Maint Type* and *Maint Data*. They contain details about the maintenance event selected with the *Select Maint* cell.

2.1.6 PROTECTION EVENTS

The IED logs protection starts and trips as individual events. Protection events are special types of standard events.

The event type description shown in the *Event Text* cell for this type of event is dependent on the protection event that occurred. Each time a protection event occurs, a DDB signal changes state. It is the name of this DDB signal followed by 'ON' or 'OFF' that appears in the *Event Text* cell.

The **Event Value** cell for this type of event is a 32 bit binary string representing the state of the relevant DDB signals. These binary strings can also be viewed in the *COMMISSION TESTS* column in the relevant DDB batch cells.

Not all DDB signals can generate an event. Those that can are listed in the *RECORD CONTROL* column. In this column, you can set which DDBs generate events.

2.1.7 SECURITY EVENTS

An event record is generated each time a setting that requires an access level is executed.

The event type description shown in the *Event Text* cell displays the type of change.

2.1.8 PLATFORM EVENTS

Platform events are special types of standard events.

The event type description shown in the *Event Text* cell displays the type of change.

3 DISTURBANCE RECORDER

The disturbance recorder feature allows you to record selected current and voltage inputs to the protection elements, together with selected digital signals. The digital signals may be inputs, outputs, or internal DDB signals. The disturbance records can be extracted using the disturbance record viewer in the settings application software. The disturbance record file can also be stored in the COMTRADE format. This allows the use of other packages to view the recorded data.

The integral disturbance recorder has an area of memory specifically set aside for storing disturbance records. The number of records that can be stored is dependent on the recording duration. The minimum duration is 0.1 s and the maximum duration is 10.5 s.

When the available memory is exhausted, the oldest records are overwritten by the newest ones.

Each disturbance record consists of a number of analogue data channels and digital data channels. The relevant CT and VT ratios for the analogue channels are also extracted to enable scaling to primary quantities.

The fault recording times are set by a combination of the *Duration* and *Trigger Position* cells. The *Duration* cell sets the overall recording time and the *Trigger Position* cell sets the trigger point as a percentage of the duration. For example, the default settings show that the overall recording time is set to 1.5 s with the trigger point being at 33.3% of this, giving 0.5 s pre-fault and 1 s post fault recording times.

With the *Trigger Mode* set to *Single*, if further triggers occurs whilst a recording is taking place, the recorder will ignore the trigger. However, with the *Trigger Mode* set to *Extended*, the post trigger timer will be reset to zero, extending the recording time.

You can select any of the IED's analogue inputs as analogue channels to be recorded. You can also map any of the opto-inputs output contacts to the digital channels. In addition, you may also map a number of DDB signals such as Starts and LEDs to digital channels.

You may choose any of the digital channels to trigger the disturbance recorder on either a low to high or a high to low transition, via the *Input Trigger* cell. The default settings are such that any dedicated trip output contacts will trigger the recorder.

It is not possible to view the disturbance records locally via the front panel LCD. You must extract these using suitable setting application software such as MiCOM S1 Agile.

4 MEASUREMENTS

4.1 MEASURED QUANTITIES

The device measures directly and calculates a number of system quantities, which are updated every second. You can view these values in the relevant MEASUREMENT columns or with the Measurement Viewer in the settings application software. Depending on the model, the device may measure and display some or more of the following quantities:

- Measured and calculated analogue current and voltage values
- Power and energy quantities
- Peak, fixed and rolling demand values
- Frequency measurements
- Thermal measurements

4.1.1 MEASURED AND CALCULATED CURRENTS

The device measures phase-to-phase and phase-to-neutral current values. The values are produced by sampling the analogue input quantities, converting them to digital quantities to present the magnitude and phase values. Sequence quantities are produced by processing the measured values. These are also displayed as magnitude and phase angle values.

These measurements are contained in the MEASUREMENTS 1 column.

4.1.2 MEASURED AND CALCULATED VOLTAGES

The device measures phase-to-phase and phase-to-neutral voltage values. The values are produced by sampling the analogue input quantities, converting them to digital quantities to present the magnitude and phase values. Sequence quantities are produced by processing the measured values. These are also displayed as magnitude and phase angle values.

These measurements are contained in the MEASUREMENTS 1 column.

4.1.3 POWER AND ENERGY OUANTITIES

Using the measured voltages and currents the device calculates the apparent, real and reactive power quantities. These are produced on a phase by phase basis together with three-phase values based on the sum of the three individual phase values. The signing of the real and reactive power measurements can be controlled using the measurement mode setting. The four options are defined in the following table:

Measurement Mode	Parameter	Signing
0	Export Power Import Power	+
(Default)	Lagging Vars Leading VArs	+
1	Export Power Import Power Lagging Vars Leading VArs	- + + -
2	Export Power Import Power Lagging Vars Leading VArs	+ - - +

Measurement Mode	Parameter	Signing
	Export Power	_
7	Import Power	+
3	Lagging Vars Leading VArs	_
	Leading VArs	+

The device also calculates the per-phase and three-phase power factors.

These power values increment the total real and total reactive energy measurements. Separate energy measurements are maintained for the total exported and imported energy. The energy measurements are incremented up to maximum values of 1000 GWhr or 1000 GVARhr at which point they reset to zero. It is possible to reset these values using the menu or remote interfaces using the Reset demand cell.

These measurements are contained in the MEASUREMENTS 2 column.

4.1.4 DEMAND VALUES

The device produces fixed, rolling, and peak demand values. You reset these quantities using the *Reset demand* cell

The fixed demand value is the average value of a quantity over the specified interval. Values are produced for three phase real and reactive power. The fixed demand values displayed are those for the previous interval. The values are updated at the end of the fixed demand period according to the *Fix Dem Period* setting in the *MEASURE'T SETUP* column.

The rolling demand values are similar to the fixed demand values, but a sliding window is used. The rolling demand window consists of a number of smaller sub-periods. The resolution of the sliding window is the sub-period length, with the displayed values being updated at the end of each of the sub-periods according to the *Roll Sub Period* setting in the *MEASURE'T SETUP* column.

Peak demand values are produced for each phase current and the real and reactive power quantities. These display the maximum value of the measured quantity since the last reset of the demand values.

These measurements are contained in the MEASUREMENTS 2 column.

4.1.5 FREQUENCY MEASUREMENTS

The device produces a range of frequency statistics and measurements relating to the Frequency Protection function. These include Check synchronisation and Slip frequency measurements found in the *MEASUREMENTS 1* column, Rate of Change of Frequency measurements found in the *MEASUREMENTS 3* column, and Frequency Protection statistics found in the *FREQUENCY STAT*. column.

The device produces the slip frequency measurement by measuring the rate of change of phase angle between the bus and line voltages, over a one-cycle period. The slip frequency measurement assumes the bus voltage to be the reference phasor.

4.1.6 OTHER MEASUREMENTS

Depending on the model, the device produces a range of other measurements such as thermal measurements.

These measurements are contained in the MEASUREMENTS 3 column.

4.2 MEASUREMENT SETUP

You can define the way measurements are set up and displayed using the *MEASURE'T SETUP* column and the measurements are shown in the relevant MEASUREMENTS tables.

4.3 FAULT LOCATOR

Some models provide fault location functionality. It is possible to identify the fault location by measuring the fault voltage and current magnitude and phases and presenting this information to a Fault Locator function. The fault locator is triggered whenever a fault record is generated, and the subsequent fault location data is included as part of the fault record. This information is also displayed in the *Fault Location* cell in the *VIEW RECORDS* column. This cell will display the fault location in metres, miles ohms or percentage, depending on the chosen units in the *Fault Location* cell of the *MEASURE'T SETUP* column.

The Fault Locator uses pre-fault and post-fault analogue input signals to calculate the fault location. The result is included it in the fault record. The pre-fault and post-fault voltages are also presented in the fault record.

4.3.1 FAULT LOCATOR SETTINGS EXAMPLE

Assuming the following data for the protected line:

Parameter	Value
CT Ratio	1200/5
VT Ratio	230000/115
Line Length	10 km
Positive sequence line impedance ZL1 (per km)	0.089+j0.476 Ohms/km
Zero sequence line impedance ZLO	0.34+j1.03 ohms/km
Zero sequence mutual impedance ZM0	0.1068+j0.5712 Ohms/km

The line impedance magnitude and angle settings are calculated as follows:

- Ratio of secondary to primary impedance = CT ratio/VT ratio = 0.12
- Positive sequence line impedance ZL1 (total) = $0.12 \times 10(0.484 \angle 79.4^{\circ}) = 0.58 \angle 79.4^{\circ}$
- Therefore set line length = 0.58
- Line angle = 79°

The residual impedance compensation magnitude and angle are calculated using the following formula:

$$KZn = \frac{ZL0 - ZL1}{3ZL1} = \frac{(0.34 + j1.03) - (0.089 + j0.476)}{3(0.484 \angle 79.4^{\circ})} = \frac{0.6 \angle 65.2^{\circ}}{1.45 \angle 79.4^{\circ}} = 0.41 \angle -14.2^{\circ}$$

Therefore the settings are:

- KZN Residual = 0.41
- KZN Res Angle = -14

4.4 OPTO-INPUT TIME STAMPING

Each opto-input sample is time stamped within a tolerance of +/- 1 ms with respect to the Real Time Clock. These time stamps are used for the opto event logs and for the disturbance recording. The device needs to be synchronised accurately to an external clock source such as an IRIG-B signal or a master clock signal provided in the relevant data protocol.

For both the filtered and unfiltered opto-inputs, the time stamp of an opto-input change event is the sampling time at which the change of state occurred. If multiple opto-inputs change state at the same sampling interval, these state changes are reported as a single event.

5 CB CONDITION MONITORING

The device records various statistics related to each circuit breaker trip operation, allowing an accurate assessment of the circuit breaker condition to be determined. The circuit breaker condition monitoring counters are incremented every time the device issues a trip command.

These statistics are available in the *CB CONDITION* column. The menu cells are counter values only, and cannot be set directly. The counters may be reset, however, during maintenance. This is achieved with the setting *Reset CB Data*.

Note:

When in Commissioning test mode the CB condition monitoring counters are not updated.

5.1 APPLICATION NOTES

5.1.1 SETTING THE THRESHOLDS FOR THE TOTAL BROKEN CURRENT

Where power lines use oil circuit breakers (OCBs), changing of the oil accounts for a significant proportion of the switchgear maintenance costs. Often, oil changes are performed after a fixed number of CB fault operations. However, this may result in premature maintenance where fault currents tend to be low, because oil degradation may be slower than would normally be expected. The Total Current Accumulator (I^ counter) cumulatively stores the total value of the current broken by the circuit breaker providing a more accurate assessment of the circuit breaker condition.

The dielectric withstand of the oil generally decreases as a function of I²t, where 'I' is the broken fault current and 't' is the arcing time within the interrupter tank. The arcing time cannot be determined accurately, but is generally dependent on the type of circuit breaker being used. Instead, you set a factor (*Broken I*^) with a value between 1 and 2, depending on the circuit breaker.

Most circuit breakers would have this value set to '2', but for some types of circuit breaker, especially those operating on higher voltage systems, a value of 2 may be too high. In such applications **Broken I^** may be set lower, typically 1.4 or 1.5.

The setting range for **Broken I^** is variable between 1.0 and 2.0 in 0.1 steps.

Note:

Any maintenance program must be fully compliant with the switchgear manufacturer's instructions.

5.1.2 SETTING THE THRESHOLDS FOR THE NUMBER OF OPERATIONS

Every circuit breaker operation results in some degree of wear for its components. Therefore routine maintenance, such as oiling of mechanisms, may be based on the number of operations. Suitable setting of the maintenance threshold will allow an alarm to be raised, indicating when preventative maintenance is due. Should maintenance not be carried out, the device can be set to lockout the autoreclose function on reaching a second operations threshold (*No. CB ops Lock*). This prevents further reclosure when the circuit breaker has not been maintained to the standard demanded by the switchgear manufacturer's maintenance instructions.

Some circuit breakers, such as oil circuit breakers (OCBs) can only perform a certain number of fault interruptions before requiring maintenance attention. This is because each fault interruption causes carbonising of the oil, degrading its dielectric properties. The maintenance alarm threshold (setting *No. CB Ops Maint*) may be set to indicate the requirement for oil dielectric testing, or for more comprehensive maintenance. Again, the lockout threshold *No. CB Ops Lock* may be set to disable autoreclosure when repeated further fault interruptions could not be guaranteed. This minimises the risk of oil fires or explosion.

5.1.3 SETTING THE THRESHOLDS FOR THE OPERATING TIME

Slow CB operation indicates the need for mechanism maintenance. Alarm and lockout thresholds (*CB Time Maint* and *CB Time Lockout*) are provided to enforce this. They can be set in the range of 5 to 500 ms. This time relates to the interrupting time of the circuit breaker.

5.1.4 SETTING THE THRESHOLDS FOR EXCESSSIVE FAULT FREQUENCY

Persistent faults will generally cause autoreclose lockout, with subsequent maintenance attention. Intermittent faults such as clashing vegetation may repeat outside of any reclaim time, and the common cause might never be investigated. For this reason it is possible to set a frequent operations counter, which allows the number of operations *Fault Freq Count* over a set time period *Fault Freq Time* to be monitored. A separate alarm and lockout threshold can be set.

6 CB STATE MONITORING

CB State monitoring is used to verify the open or closed state of a circuit breaker. Most circuit breakers have auxiliary contacts through which they transmit their status (open or closed) to control equipment such as IEDs. These auxiliary contacts are known as:

- 52A for contacts that follow the state of the CB
- 52B for contacts that are in opposition to the state of the CB

This device can be set to monitor both of these types of circuit breaker state indication. If the state is unknown for some reason, an alarm can be raised.

Some CBs provide both sets of contacts. If this is the case, these contacts will normally be in opposite states. Should both sets of contacts be open, this would indicate one of the following conditions:

- Auxiliary contacts/wiring defective
- Circuit Breaker (CB) is defective
- CB is in isolated position

Should both sets of contacts be closed, only one of the following two conditions would apply:

- Auxiliary contacts/wiring defective
- Circuit Breaker (CB) is defective

If any of the above conditions exist, an alarm will be issued after a 5 s time delay. An output contact can be assigned to this function via the programmable scheme logic (PSL). The time delay is set to avoid unwanted operation during normal switching duties.

In the CB CONTROL column there is a setting called *CB Status Input*. This cell can be set at one of the following four options:

- None
- 52A
- 52B
- Both 52A and 52B

Where *None* is selected no CB status is available. Where only 52A is used on its own then the device will assume a 52B signal opposite to the 52A signal. Circuit breaker status information will be available in this case but no discrepancy alarm will be available. The above is also true where only a 52B is used. If both 52A and 52B are used then status information will be available and in addition a discrepancy alarm will be possible, according to the following table:

Auxiliary Co	ntact Position	CB State Detected	Action
52A	52B		
Open	Closed	Breaker open	Circuit breaker healthy
Closed	Open	Breaker closed	Circuit breaker healthy
Closed	Closed	CB failure	Alarm raised if the condition persists for greater than 5 s
Open	Open	State unknown	Alarm raised if the condition persists for greater than 5 s

6.1 CB STATE MONITORING LOGIC

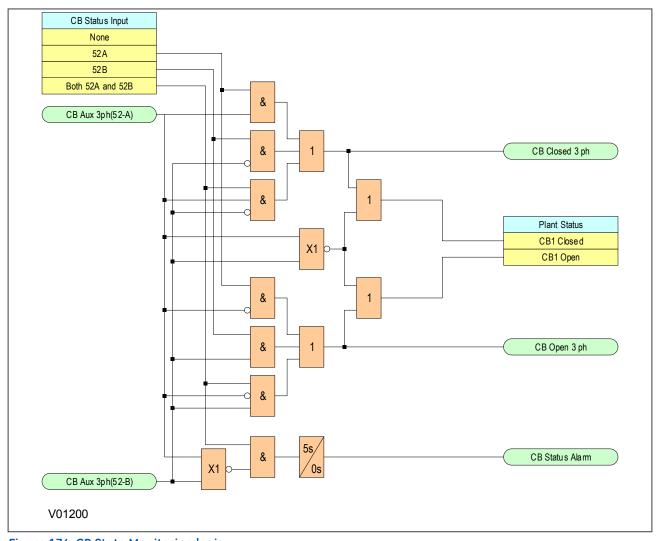


Figure 174: CB State Monitoring logic

7 CIRCUIT BREAKER CONTROL

Although some circuit breakers do not provide auxiliary contacts, most provide auxiliary contacts to reflect the state of the circuit breaker. These are:

- CBs with 52A contacts (where the auxiliary contact follows the state of the CB)
- CBs with 52B contacts (where the auxiliary contact is in the opposite state from the state of the CB)
- CBs with both 52A and 52B contacts

Circuit Breaker control is only possible if the circuit breaker in question provides auxiliary contacts. The *CB Status Input* cell in the *CB CONTROL* column must be set to the type of circuit breaker. If no CB auxiliary contacts are available then this cell should be set to *None*, and no CB control will be possible.

For local control, the *CB control by* cell should be set accordingly.

The output contact can be set to operate following a time delay defined by the setting *Man Close Delay*. One reason for this delay is to give personnel time to safely move away from the circuit breaker following a CB close command.

The control close cycle can be cancelled at any time before the output contact operates by any appropriate trip signal, or by activating the **Reset Close Dly** DDB signal.

The length of the trip and close control pulses can be set via the *Trip Pulse Time* and *Close Pulse Time* settings respectively. These should be set long enough to ensure the breaker has completed its open or close cycle before the pulse has elapsed.

If an attempt to close the breaker is being made, and a protection trip signal is generated, the protection trip command overrides the close command.

The **Reset Lockout by** setting is used to enable or disable the resetting of lockout automatically from a manual close after the time set by **Man Close RstDly**.

If the CB fails to respond to the control command (indicated by no change in the state of CB Status inputs) an alarm is generated after the relevant trip or close pulses have expired. These alarms can be viewed on the LCD display, remotely, or can be assigned to output contacts using the programmable scheme logic (PSL).

Note:

The **CB Healthy Time** and **Sys Check time** set under this menu section are applicable to manual circuit breaker operations only. These settings are duplicated in the AUTORECLOSE menu for autoreclose applications.

The **Lockout Reset** and **Reset Lockout by** settings are applicable to CB Lockouts associated with manual circuit breaker closure, CB Condition monitoring (Number of circuit breaker operations, for example) and autoreclose lockouts.

The device includes the following options for control of a single circuit breaker:

- The IED menu (local control)
- The Hotkeys (local control)
- The function keys (local control)
- The opto-inputs (local control)
- SCADA communication (remote control)

7.1 CB CONTROL USING THE IED MENU

You can control manual trips and closes with the *CB Trip/Close* command in the *SYSTEM DATA* column. This can be set to *No Operation*, *Trip*, or *Close* accordingly.

For this to work you have to set the *CB control by* cell to option 1 *Local*, option 3 *Local* + *Remote*, option 5 *Opto+Local*, or option 7 *Opto+Local+Remote* in the *CB CONTROL* column.

7.2 CB CONTROL USING THE HOTKEYS

The hotkeys allow you to manually trip and close the CB without the need to enter the SYSTEM DATA column. For this to work you have to set the CB control by cell to option 1 Local, option 3 Local+Remote, option 5 Opto+Local+Remote in the CB CONTROL column.

CB control using the hotkey is achieved by pressing the right-hand button directly below LCD screen. This button is only enabled if:

- The CB Control by setting is set to one of the options where local control is possible (option 1,3,5, or 7)
- The CB Status Input is set to '52A', '52B', or 'Both 52A and 52B'

If the CB is currently closed, the command text on the bottom right of the LCD screen will read Trip. Conversely, if the CB is currently open, the command text will read Close.

If you execute a Trip, a screen with the CB status will be displayed once the command has been completed. If you execute a Close, a screen with a timing bar will appear while the command is being executed. This screen also gives you the option to cancel or restart the close procedure. The time delay is determined by the Man Close Delay setting in the CB CONTROL menu. When the command has been executed, a screen confirming the present status of the circuit breaker is displayed. You are then prompted to select the next appropriate command or exit.

If no keys are pressed for a period of 5 seconds while waiting for the command confirmation, the device will revert to showing the CB Status. If no key presses are made for a period of 25 seconds while displaying the CB status screen, the device will revert to the default screen.

To avoid accidental operation of the trip and close functionality, the hotkey CB control commands are disabled for 10 seconds after exiting the hotkey menu.

The hotkey functionality is summarised graphically below:

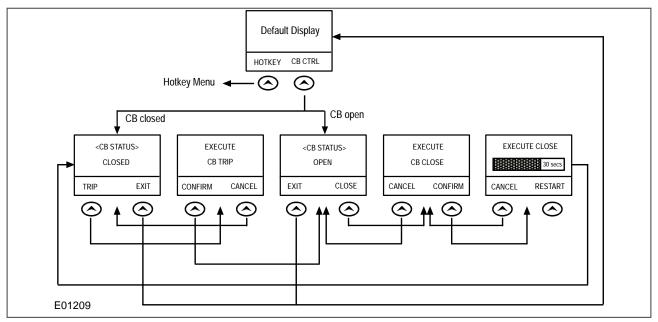


Figure 175: Hotkey menu navigation

7.3 CB CONTROL USING THE FUNCTION KEYS

For most models, you can also use the function keys to allow direct control of the circuit breaker. This has the advantage over hotkeys, that the LEDs associated with the function keys can indicate the status of the CB. The

default PSL is set up such that Function key 2 initiates a trip and Function key 3 initiates a close. For this to work you have to set the CB control by cell to option 5 Opto+Loca1, or option 7 Opto+Loca1+Remote in the CB CONTROL column.

As shown below, function keys 2 and 3 have already been assigned to CB control in the default PSL.

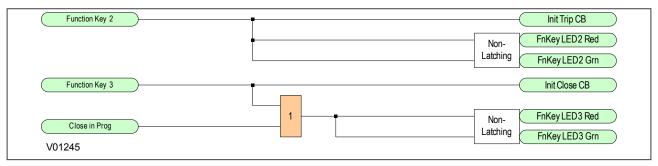


Figure 176: Default function key PSL

The programmable function key LEDs have been mapped such that they will indicate yellow whilst the keys are activated.

Note: Not all models provide function keys.

7.4 CB CONTROL USING THE OPTO-INPUTS

Certain applications may require the use of push buttons or other external signals to control the various CB control operations. It is possible to connect such push buttons and signals to opto-inputs and map these to the relevant DDB signals.

For this to work, you have to set the *CB control by* cell to option 4 opto, option 5 Opto+Local, option 6 Opto+Remote, or option 7 Opto+Local+Remote in the *CB CONTROL* column.

7.5 REMOTE CB CONTROL

Remote CB control can be achieved by setting the *CB Trip/Close* cell in the *SYSTEM DATA* column to trip or close by using a command over a communication link.

For this to work, you have to set the *CB control by* cell to option 2 *Remote*, option 3 *Local+Remote*, option 6 *Opto+remote*, or option 7 *Opto+Local+Remote* in the *CB CONTROL* column.

We recommend that you allocate separate relay output contacts for remote CB control and protection tripping. This allows you to select the control outputs using a simple local/remote selector switch as shown below. Where this feature is not required the same output contact(s) can be used for both protection and remote tripping.

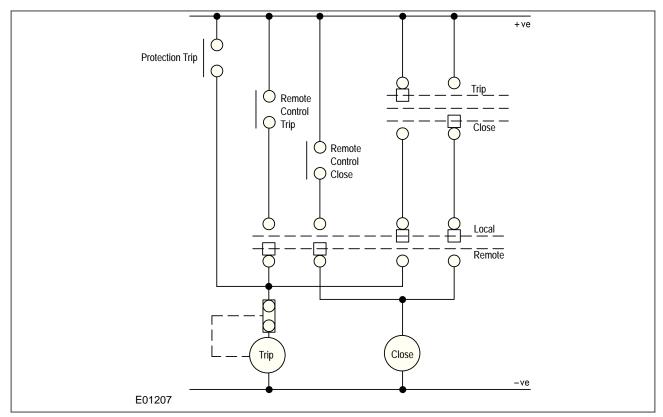


Figure 177: Remote Control of Circuit Breaker

CB Control Disabled Opto Local Opto+Local 1 Enable opto-initiated CB trip and close Opto+Remote Local+Remote Opto+Rem+Local HMI Trip Control Trip Trip pulse Init Trip CB Q & Man CB Trip Fail Init close CB Close in Prog Delayed control close time HMI Close Control Close AR In Progress Auto Close Pulsed output latched in HMI CB Cls Fail AR models only Reset Close Dly Trip Command In Ext. Trip 3ph Control Trip CB Open 3 ph CB Closed 3 ph CB health y window Man CB Unhealthy CB Healthy C/S window Voltage models only Man No Checksync Man Check Synch V01208

7.6 CB CONTROL LOGIC

Figure 178: CB Control logic

7.7 SYNCHRONISATION CHECK

Where the check synchronism function is set, this can be enabled to supervise manual circuit breaker Close commands. A circuit breaker Close command will only be issued if the Check Synchronisation criteria are satisfied. A time delay can be set with the setting *Sys Check time*. If the Check Synchronisation criteria are not satisfied within the time period following a Close command the device will lockout and alarm.

7.8 CB HEALTHY CHECK

A CB Healthy check is available if required. This facility accepts an input to one of the opto-inputs to indicate that the breaker is capable of closing (e.g. that it is fully charged). A time delay can be set with the setting *CB Healthy Time*. If the CB does not indicate a healthy condition within the time period following a Close command, the device will lockout and alarm.

8 POLE DEAD FUNCTION

The Pole Dead Logic is used to determine and indicate that one or more phases of the line are not energised. A Pole Dead condition is determined either by measuring:

- the line currents and/or voltages, or
- by monitoring the status of the circuit breaker auxiliary contacts, as shown by dedicated DDB signals.

It can also be used to block operation of underfrequency and undervoltage elements where applicable.

8.1 POLE DEAD LOGIC

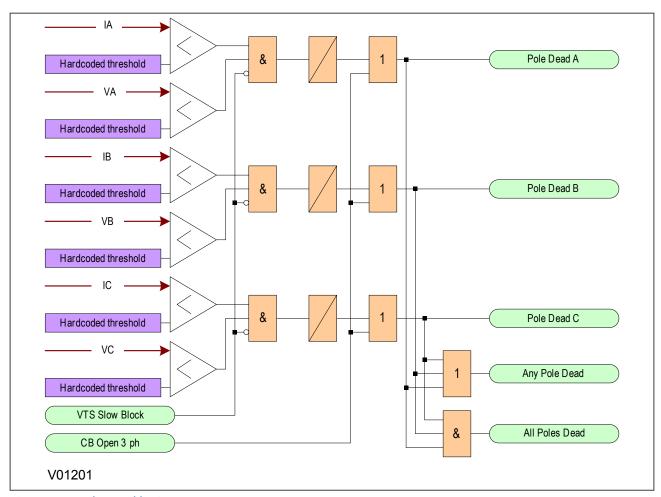


Figure 179: Pole Dead logic

If both the line current and voltage fall below certain thresholds, the device will initiate a Pole Dead condition. The undervoltage (V<) and undercurrent (I<) thresholds are hardcoded internally.

If one or more poles are dead, the device will indicate which phase is dead and will also assert the **Any Pole Dead** DDB signal. If all phases are dead the **Any Pole Dead** signal would be accompanied by the **All Poles Dead** signal.

If a VT fails, a **VTS Slow Block** signal is generated to block the Pole Dead indications that would be generated by the undervoltage and undercurrent thresholds. However, the VTS logic will not block the Pole Dead indications if they are initiated by a **CB Open 3 ph** signal. A **CB Open 3 ph** signal automatically initiates a Pole Dead condition regardless of the current and voltage measurement.

9 SYSTEM CHECKS

In some situations it is possible for both "bus" and "line" sides of a circuit breaker to be live when a circuit breaker is open - for example at the ends of a feeder that has a power source at each end. Therefore, it is normally necessary to check that the network conditions on both sides are suitable, before closing the circuit breaker. This applies to both manual circuit breaker closing and autoreclosing. If a circuit breaker is closed when the line and bus voltages are both live, with a large phase angle, frequency or magnitude difference between them, the system could be subjected to an unacceptable shock, resulting in loss of stability, and possible damage to connected machines.

The System Checks functionality involves monitoring the voltages on both sides of a circuit breaker, and if both sides are live, performing a synchronisation check to determine whether any differences in voltage magnitude, phase angle or frequency are within permitted limits.

The pre-closing system conditions for a given circuit breaker depend on the system configuration, and for autoreclosing, on the selected autoreclose program. For example, on a feeder with delayed autoreclosing, the circuit breakers at the two line ends are normally arranged to close at different times. The first line end to close usually has a live bus and a dead line immediately before reclosing. The second line end circuit breaker now sees a live bus and a live line.

If there is a parallel connection between the ends of the tripped feeder the frequencies will be the same, but any increased impedance could cause the phase angle between the two voltages to increase. Therefore just before closing the second circuit breaker, it may be necessary to perform a synchronisation check, to ensure that the phase angle between the two voltages has not increased to a level that would cause unacceptable shock to the system when the circuit breaker closes.

If there are no parallel interconnections between the ends of the tripped feeder, the two systems could lose synchronism altogether and the frequency at one end could "slip" relative to the other end. In this situation, the second line end would require a synchronism check comprising both phase angle and slip frequency checks.

If the second line-end busbar has no power source other than the feeder that has tripped; the circuit breaker will see a live line and dead bus assuming the first circuit breaker has re-closed. When the second line end circuit breaker closes the bus will charge from the live line (dead bus charge).

9.1 SYSTEM CHECKS IMPLEMENTATION

The System Checks function provides *Live/Dead Voltage Monitoring*, two stages of *Check Synchronisation* and *System Split* indication.

The System Checks function is enabled or disabled by the **System Checks** setting in the **CONFIGURATION** column. If **System Checks** is disabled, the **SYSTEM CHECKS** menu becomes invisible, and a **SysChks Inactive** DDB signal is set.

9.1.1 VT CONNECTIONS

The device provides inputs for a three-phase "Main VT" and at least one single-phase VT for check synchronisation. Depending on the primary system arrangement, the Main VT may be located on either the line-side of the busbarside of the circuit breaker, with the Check Sync VT on the other. Normally, the Main VT is located on the line-side (as per the default setting), but this is not always the case. For this reason, a setting is provided where you can define this. This is the *Main VT Location* setting, which is found in the *CT AND VT RATIOS* column.

The Check Sync VT may be connected to one of the phase-to-phase voltages or phase-to-neutral voltages. This needs to be defined using the *CS Input* setting in the *CT AND VT RATIOS* column. Options are, A-B, B-C, C-A, A-N, B-N, or C-N.

9.1.2 **VOLTAGE MONITORING**

The settings in the *VOLTAGE MONITORS* sub-heading in the *SYSTEM CHECKS* column allow you to define the threshold at which a voltage is considered live, and a threshold at which the voltage is considered dead. These thresholds apply to both line and bus sides. If the measured voltage falls below the *Dead Voltage* setting, a DDB

signal is generated (*Dead Bus*, or *Dead Line*, depending on which side is being measured). If the measured voltage exceeds the *Live Voltage* setting, a DDB signal is generated (*Live Bus*, or *Live Line*, depending on which side is being measured).

9.1.3 CHECK SYNCHRONISATION

The device provides two stages of Check Synchronisation. The first stage (CS1) is intended for use in synchronous systems. This means, where the frequencies and phase angles of both sides are compared and if the difference is within set limits, the circuit breaker is allowed to close. The second stage (CS2) is similar to stage, but has an additional adaptive setting. The second stage CS2 is intended for use in asynchronous systems, i.e. where the two sides are out of synchronism and one frequency is slipping continuously with respect to another. If the closing time of the circuit breaker is known, the CB Close command can be issued at a definite point in the cycle such that the CB closes at the point when both sides are in phase.

In situations where it is possible for the voltages on either side of a circuit breaker to be either synchronous or asynchronous, both CS1 and CS2 can be enabled to provide a CB Close signal if either set of permitted closing conditions is satisfied.

Each stage can also be set to inhibit circuit breaker closing if selected blocking conditions such as overvoltage, undervoltage or excessive voltage magnitude difference are detected. CS2 requires the phase angle difference to be decreasing in magnitude before permitting the circuit breaker to close. CS2 has an optional "Adaptive" closing feature, which issues the permissive close signal when the predicted phase angle difference immediately prior to the instant of circuit breaker main contacts closing (i.e. after CB Close time) is as close as practicable to zero.

Slip frequency is the rate of change of phase between each side of the circuit breaker, which is measured by the difference between the voltage signals on either side of the circuit breaker.

Having two system synchronism check stages available allows the circuit breaker closing to be enabled under different system conditions (for example, low slip / moderate phase angle, or moderate slip / small phase angle).

The settings specific to Check Synchronisation are found under the sub-heading CHECK SYNC in the SYSTEM CHECKS column. The only difference between the CS1 settings and the CS2 settings is that **CS2 Slip Control** setting has an option for predictive closure of CB (Freq + CB Comp).

9.1.4 CHECK SYNCRONISATION VECTOR DIAGRAM

The following vector diagram represents the conditions for the System Check functionality. The Dead Volts setting is represented as a circle around the origin whose radius is equal to the maximum voltage magnitude, whereby the voltage can be considered dead. The nominal line voltage magnitude is represented by a circle around the origin whose radius is equal to the nominal line voltage magnitude. The minimum voltage magnitude at which the system can be considered as Live, is the magnitude difference between the bus and line voltages.

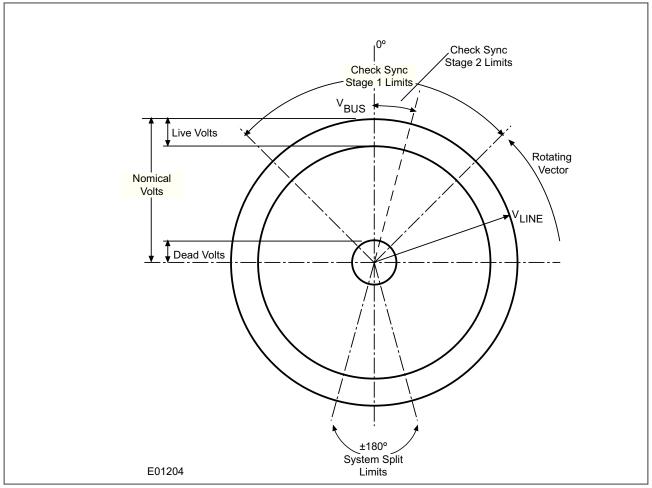


Figure 180: Check Synchronisation vector diagram

9.1.5 SYSTEM SPLIT

If the line side and bus side are of the same frequency (i.e. in synchronism) but have a large phase angle between them $(180^{\circ} + / -$ the set limits), the system is said to be 'Split'. If this is the case, the device will detect this and issue an alarm signal indicating this.

The settings specific to System Split functionality are found under the sub-heading SYSTEM SPLIT in the SYSTEM CHECKS column.

9.2 SYSTEM CHECK LOGIC

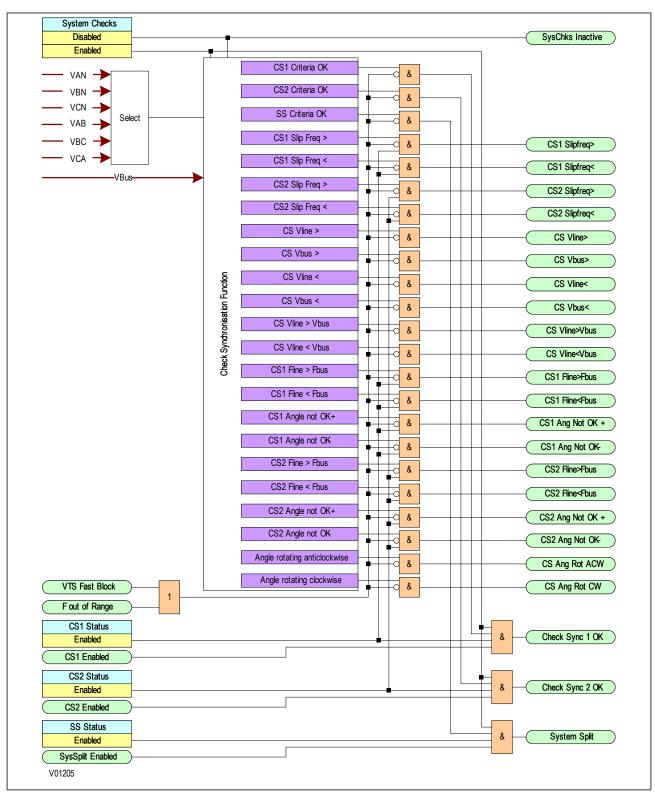


Figure 181: System Check logic

9.3 SYSTEM CHECK PSL

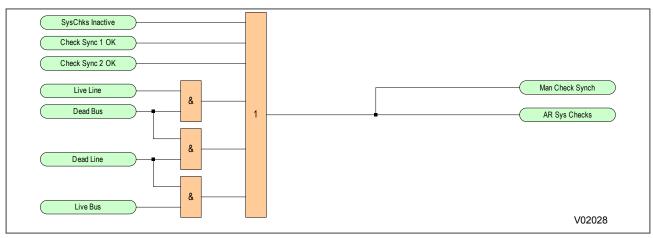


Figure 182: System Check PSL

9.4 APPLICATION NOTES

9.4.1 SLIP CONTROL

Slip control can be achieved by timer, by frequency or by both. The settings CS1 Slip Control and CS2 Slip Control are used to determine which type of slip control is to be used. As the device supports direct measurement of frequency, you would normally use frequency.

If you are using Slip Control by Timer, the combination of Phase Angle and Timer settings determines an effective maximum slip frequency, calculated as:

2A/360T - for CS1 A/360T - for CS2

where:

- A = Phase Angle setting in degrees
- T = Slip Timer setting in seconds

Examples

For CS1, where the Phase Angle setting is 30° and the Timer setting is 3.3 s, the "slipping" vector has to remain within \pm 30° of the reference vector for at least 3.3 seconds. Therefore a synchronisation check output will not be given if the slip is greater than 2 × 30° in 3.3 seconds.

Therefore, the maximum slip frequency = 2x30/360x3.3 = 0.0505 hz.

For CS2, where the Phase Angle setting is 10° and the Timer setting is 0.1 sec., the slipping vector has to remain within 10° of the reference vector, with the angle decreasing, for 0.1 sec. When the angle passes through zero and starts to increase, the synchronisation check output is blocked. Therefore an output will not be given if the slip is greater than 10° in 0.1 second.

Therefore, the maximum slip frequency = $10/360 \times 0.1 = 0.278$ Hz.

Slip control by Timer is not practical for "large slip/small phase angle" applications, because the timer settings required are very small, sometimes less than 0.1 seconds. For these situations, slip control by frequency is better.

If Slip Control by Frequency + Timer is selected, for an output to be given, the slip frequency must be less than BOTH the set Slip Freq. value and the value determined by the Phase Angle and Timer settings.

9.4.2 USE OF CHECK SYNC 2 AND SYSTEM SPLIT

Check Sync 2 (CS2) and System Split functions are included for situations where the maximum permitted slip frequency and phase angle for synchronism checks can change due to adverse system conditions. A typical application is on a closely interconnected system, where synchronism is normally retained when a feeder is tripped. But under some circumstances, with parallel interconnections out of service, the feeder ends can drift out of synchronism when the feeder is tripped. Depending on the system and machine characteristics, the conditions for safe circuit breaker closing could be, for example:

Condition 1: For synchronized systems, with zero or very small slip:

• Slip <50 mHz; phase angle <30°

Condition 2: For unsynchronized systems, with significant slip:

• Slip < 250 mHz; phase angle <10° and decreasing

By enabling both CS1 and CS2, the device can be configured to allow CB closure if either of the two conditions is detected.

For manual circuit breaker closing with synchronism check, some utilities might prefer to arrange the logic to check initially for condition 1 only. However, if a System Split is detected before the condition 1 parameters are satisfied, the device will switch to checking for condition 2 parameters instead, based on the assumption that a significant degree of slip must be present when system split conditions are detected. This can be arranged by suitable PSL logic, using the System Check DDB signals.

9.4.3 PREDICTIVE CLOSURE OF CIRCUIT BREAKER

The setting *CS2 Slip Control* setting contains an option (freq + CB comp) for compensating the time taken to close the CB. When set to provide CB Close Time compensation, a predictive approach is used to close the circuit breaker ensuring that closing occurs at close to 0° therefore minimising the impact to the power system. The actual closing angle is subject to the constraints of the existing product architecture, i.e. the protection task runs twice per power system cycle, based on frequency tracking over the frequency range of 40 Hz to 70 Hz.

9.4.4 VOLTAGE AND PHASE ANGLE CORRECTION

For the Check Synchronisation function, the device needs to convert measured secondary voltages into primary voltages. In some applications, VTs either side of the circuit breaker may have different VT Ratios. In such cases, a magnitude correction factor is required.

There are some applications where the main VT is on the HV side of a transformer and the Check Sync VT is on the LV side, or vice-versa. If the vector group of the transformer is not "0", the voltages are not in phase, so phase correction is also necessary.

The correction factors are as follows and are located in the CT AND VT RATIOS column:

- C/S V kSM, where kSM is the voltage correction factor.
- C/S Phase kSA, where kSA is the angle correction factor.

Assuming C/S input setting is A-N, then:

The line and bus voltage magnitudes are matched if $V_{a \text{ sec}} = V_{cs \text{ sec}} \times C/S \vee kSA$

The line and bus voltage angles are matched if $\angle V_{a \text{ sec}} = \angle V_{cs \text{ sec}} + \text{C/S Phase kSA}$

The following application scenarios show where the voltage and angular correction factors are applied to match different VT ratios:

Scenario	Physical Ratios (ph-N Values)			Setting Ratios				CS Correction Factors		
	Main VT Ratio CS		CS V1	「Ratio	Main VT Ratio (ph- ph) Always		CS VT Ratio		kSM	kSA
	Pri (kV)	Sec (V)	Pri (kV)	Sec (V)	Pri (kV)	Sec (V)	Pri (kV)	Sec (V)		
1	220/√3	110/√3	132/√3	100/√3	220	110	132	100	1.1	30°
2	220/√3	110/√3	220/√3	110	220	110	127	110	0.577	0°
3	220/√3	110/√3	220/√3	110/3	220	110	381	110	1.732	0°

10 SWITCH STATUS AND CONTROL

All P14x products support Switch Status and Control for up to 8 switchgear elements. This is available for IEC60870-5-103 and IEC61850 protocols. The device is able to monitor the status of and control up to eight switches. The types of switch that can be controlled are:

- Load Break switch
- Disconnector
- Earthing Switch
- High Speed Earthing Switch

Consider the following feeder bay:

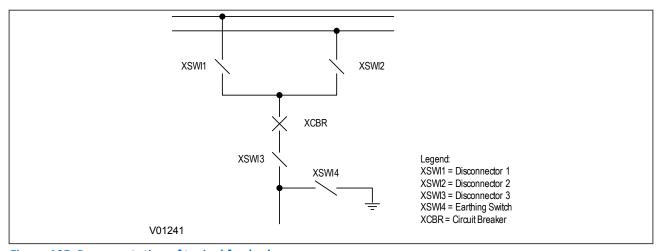


Figure 183: Representation of typical feeder bay

This bay shows four switches of the type LN XSWI and one circuit breaker of type LN XCBR. In this example, the switches XSWI1 – XSWI3 are disconnectors and XCSWI4 is an earthing switch.

For the device to be able to control the switches, the switches must provide auxiliary contacts to indicate the switch status. For convenience, the device settings refer to the auxiliary contacts as 52A and 52B, even though they are not circuit breakers.

There are eight sets of settings in the SWITCH CONTROL column, which allow you to set up the Switch control, one set for each switch. These settings are as follows:

SWITCH1 Type

This setting defines the type of switch. It can be a load breaking switch, a disconnector, an earthing switch or a high speed earthing switch.

SWI1 Status Inpt

This setting defines the type of auxiliary contacts that will be used for the control logic. For convenience, the device settings refer to the auxiliary contacts as 52A and 52B, even though they are not circuit breakers. "A" contacts match the status of the primary contacts, whilst "B" contacts are of the opposite polarity.

SWI1 Control by

This setting determines how the switch is to be controlled. This can be Local (using the device directly) remote (using a communications link), or both.

SWI1Trip/Close

This is a command to directly trip or close the switch.

SWI1 Trp Puls T and SWI1 Cls Puls T

These settings allow you to control the width of the open and close pulses.

SWI1 Sta Alrm T

This setting allows you to define the duration of wait timer before the relay raises a status alarm.

SWI1 Trp Fail T and SWI1 Cls Fail T

These settings allow you to control the delay of the open and close alarms when the final switch status is not in line with expected status.

SWI1 Operations

This is a data cell, which displays the number of switch operations that have taken place. It is an accumulator, which you can reset using the *Reset SWI1 Data* setting

Reset SWI1 Data

This setting resets the switch monitoring data.

Note

Settings for switch 1 are shown, but settings for all other switch elements are the same.

10.1 SWITCH STATUS LOGIC

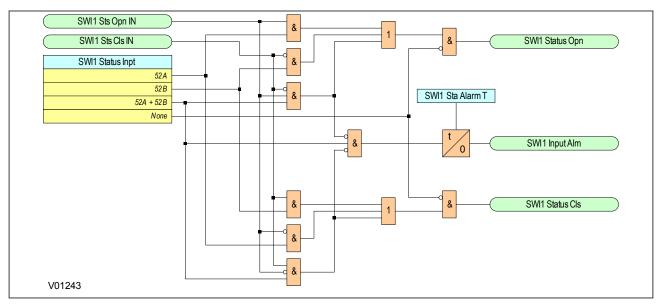


Figure 184: Switch Status logic

10.2 SWITCH CONTROL LOGIC

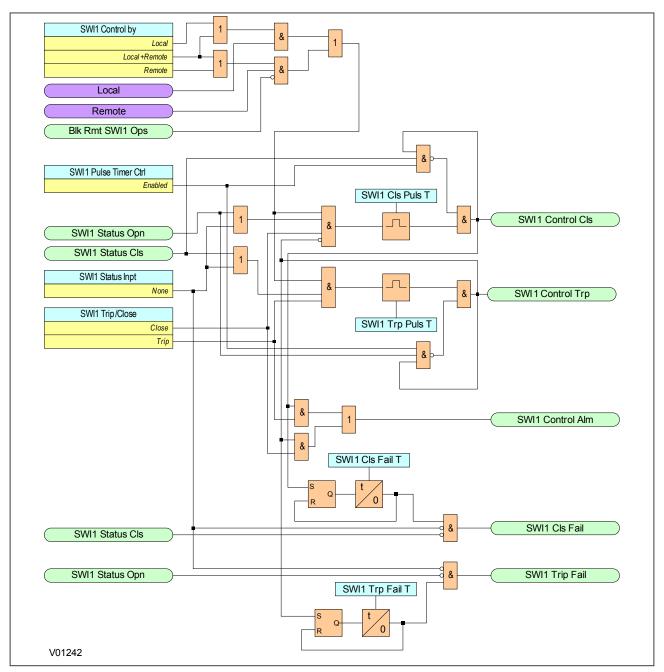


Figure 185: Switch Control logic

CHAPTER 15

SUPERVISION

Chapter 15 - Supervision

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			functions.

This chapter contains the following sections:

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2 VOLTAGE TRANSFORMER SUPERVISION

The Voltage Transformer Supervision (VTS) function is used to detect failure of the AC voltage inputs to the protection. This may be caused by voltage transformer faults, overloading, or faults on the wiring, which usually results in one or more of the voltage transformer fuses blowing.

If there is a failure of the AC voltage input, the IED could misinterpret this as a failure of the actual phase voltages on the power system, which could result in unnecessary tripping of a circuit breaker.

The VTS logic is designed to prevent such a situation by detecting voltage input failures, which are NOT caused by power system phase voltage failure, and automatically blocking associated voltage dependent protection elements. A time-delayed alarm output is available to warn of a VTS condition.

The following scenarios are possible with respect to the failure of the VT inputs.

- Loss of one or two-phase voltages
- Loss of all three-phase voltages under load conditions
- Absence of three-phase voltages upon line energisation

2.1 LOSS OF ONE OR TWO PHASE VOLTAGES

If the power system voltages are healthy, no Negative Phase Sequence (NPS) current will be present. If however, one or two of the AC voltage inputs are missing, there will be Negative Phase Sequence voltage present, even if the actual power system phase voltages are healthy. VTS works by detecting Negative Phase Sequence (NPS) voltage without the presence of Negative Phase Sequence current. So if there is NPS voltage present, but no NPS current, it is certain that there is a problem with the voltage transformers and a VTS block should be applied to voltage dependent protection functions to prevent maloperation. The use of negative sequence quantities ensures correct operation even where three-limb or V-connected VTs are used.

2.2 LOSS OF ALL THREE PHASE VOLTAGES

If all three voltage inputs are lost, there will be no Negative Phase Sequence quantities present, but the device will see that there is no voltage input. If this is caused by a power system failure, there will be a step change in the phase currents. However, if this is not caused by a power system failure, there will be no change in any of the phase currents. So if there is no measured voltage on any of the three phases and there is no change in any of the phase currents, this indicates that there is a problem with the voltage transformers and a VTS block should be applied to voltage dependent protection functions to prevent maloperation.

2.3 ABSENCE OF ALL THREE PHASE VOLTAGES ON LINE ENERGISATION

On line energization there should be a change in the phase currents as a result of loading or line charging current. Under this condition we need an alternative method of detecting three-phase VT failure.

If there is no measured voltage on all three phases during line energization, two conditions might apply:

- A three-phase VT failure
- A close-up three-phase fault.

The first condition would require VTS to block the voltage-dependent functions.

In the second condition, voltage dependent functions should not be blocked, as tripping is required.

To differentiate between these two conditions overcurrent level detectors are used (*VTS I> Inhibit* and *VTS I2> Inhibit*). These prevent a VTS block from being issued in case of a genuine fault. These elements should be set in excess of any non-fault based currents on line energisation (load, line charging current, transformer inrush current if applicable), but below the level of current produced by a close-up three-phase fault.

If the line is closed where a three-phase VT failure is present, the overcurrent detector will not operate and a VTS block will be applied. Closing onto a three-phase fault will result in operation of the overcurrent detector and prevent a VTS block being applied.

2.4 VTS IMPLEMENTATION

VTS is implemented in the SUPERVISION column of the relevant settings group.

The following settings are relevant for VT Supervision:

- VTS Status: determines whether the VTS Operate output will be a blocking output or an alarm indication only
- VTS PickupThresh: determines the threshold at which the phase voltage detectors pick up
- VTS Reset Mode: determines whether the Reset is to be manual or automatic
- VTS Time delay: determines the operating time delay
- VTS I> Inhibit: inhibits VTS operation in the case of a phase overcurrent fault
- VTS I2> Inhibit: inhibits VTS operation in the case of a negative sequence overcurrent fault

VTS is only enabled during a live line condition (as indicated by the pole dead logic) to prevent operation under dead system conditions.

2.5 VTS LOGIC

This logic will only be enabled during a live line condition (as indicated by the pole dead logic) to prevent operation under dead system conditions (i.e. where no voltage will be present and the **VTS I> Inhibit** overcurrent element will not be picked up).

Chapter 15 - Supervision P14x

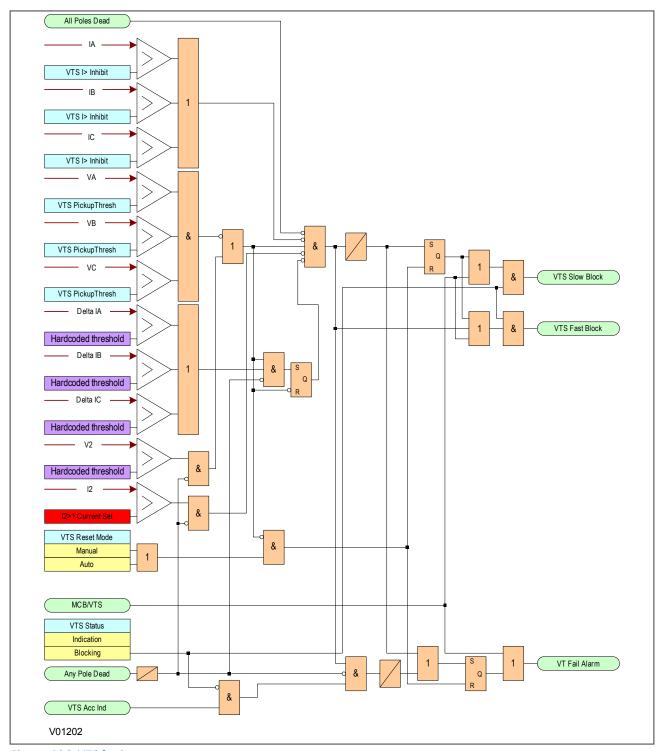


Figure 186: VTS logic

As can be seen from the diagram, the VTS function is inhibited if:

- An **All Poles Dead** DDB signal is present
- Any phase overcurrent condition exists
- A Negative Phase Sequence current exists
- If the phase current changes over the period of 1 cycle

2.6 VTS ACCELERATION INDICATION LOGIC Trip Command In V02001

Figure 187: VTS Acceleration Indication Logic

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3 CURRENT TRANSFORMER SUPERVISION

The Current Transformer Supervision function (CTS) is used to detect failure of the AC current inputs to the protection. This may be caused by internal current transformer faults, overloading, or faults on the wiring. If there is a failure of the AC current input, the protection could misinterpret this as a failure of the actual phase currents on the power system, which could result in maloperation. Also, interruption in the AC current circuits can cause dangerous CT secondary voltages to be generated.

3.1 CTS IMPLEMENTATION

If the power system currents are healthy, no zero sequence voltage are derived. However, if one or more of the AC current inputs are missing, a zero sequence current would be derived, even if the actual power system phase currents are healthy. Standard CTS works by detecting a derived zero sequence current where there is no corresponding derived zero sequence voltage.

The voltage transformer connection used must be able to refer zero sequence voltages from the primary to the secondary side. Therefore, this element should only be enabled where the VT is of a five-limb construction, or comprises three single-phase units with the primary star point earthed.

The CTS function is implemented in the SUPERVISION column of the relevant settings group, under the sub-heading CT SUPERVISION.

The following settings are relevant for CT Supervision:

- CTS Status: to disable or enable CTS
- CTS VN < Inhibit: inhibits CTS if the zero sequence voltage exceeds this setting
- CTS IN> Set: determines the level of zero sequence current
- CTS Time Delay: determines the operating time delay

3.2 CTS LOGIC

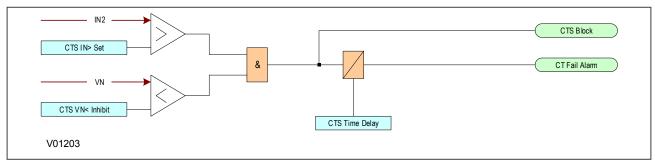


Figure 188: CTS logic diagram

If the derived earth fault current (zero sequence current) exceeds the threshold set by *CTS IN> Set*, a CTS block DDB signal is produced, provided it is not inhibited. the signal is inhibited if the residual voltage is less than the threshold set by *CTS VN< Inhibit*. A CTS alarm is generated after a short time delay defined by the setting *CTS Time Delay*.

3.3 APPLICATION NOTES

3.3.1 SETTING GUIDELINES

The residual voltage setting, *CTS VN< Inhibit* and the residual current setting, *CTS IN> Set*, should be set to avoid unwanted operation during healthy system conditions. For example:

- CTS VN < Inhibit should be set to 120% of the maximum steady state residual voltage.
- CTS IN> Set will typically be set below minimum load current.
- CTS Time Delay is generally set to 5 seconds.

Where the magnitude of residual voltage during an earth fault is unpredictable, the element can be disabled to prevent protection elements being blocked during fault conditions.

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4 TRIP CIRCUIT SUPERVISION

In most protection schemes, the trip circuit extends beyond the IED enclosure and passes through components such as links, relay contacts, auxiliary switches and other terminal boards. Such complex arrangements may require dedicated schemes for their supervision.

There are two distinctly separate parts to the trip circuit; the trip path, and the trip coil. The trip path is the path between the IED enclosure and the CB cubicle. This path contains ancillary components such as cables, fuses and connectors. A break in this path is possible, so it is desirable to supervise this trip path and to raise an alarm if a break should appear in this path.

The trip coil itself is also part of the overall trip circuit, and it is also possible for the trip coil to develop an open-circuit fault.

This product supports a number of trip circuit supervision (TCS) schemes.

4.1 TRIP CIRCUIT SUPERVISION SCHEME 1

This scheme provides supervision of the trip coil with the CB open or closed, however, it does not provide supervision of the trip path whilst the breaker is open. The CB status can be monitored when a self-reset trip contact is used. However, this scheme is incompatible with latched trip contacts, as a latched contact will short out the opto-input for a time exceeding the recommended Delayed Drop-off (DDO) timer setting of 400 ms, and therefore does not support CB status monitoring. If you require CB status monitoring, further opto-inputs must be used.

Note:

A 52a CB auxiliary contact follows the CB position. A 52b auxiliary contact is the opposite.

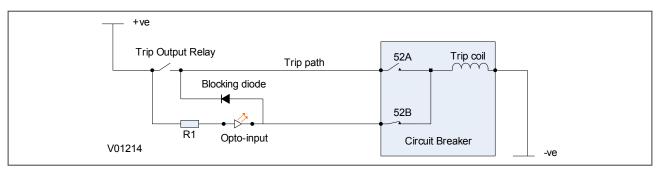


Figure 189: TCS Scheme 1

When the CB is closed, supervision current passes through the opto-input, blocking diode and trip coil. When the CB is open, supervision current flows through the opto-input and into the trip coil via the 52b auxiliary contact. This means that *Trip Coil* supervision is provided when the CB is either closed or open, however *Trip Path* supervision is only provided when the CB is closed. No supervision of the trip path is provided whilst the CB is open (pre-closing supervision). Any fault in the trip path will only be detected on CB closing, after a 400 ms delay.

4.1.1 RESISTOR VALUES

The supervision current is a lot less than the current required by the trip coil to trip a CB. The opto-input limits this supervision current to less than 10 mA. If the opto-input were to be short-circuited however, it could be possible for the supervision current to reach a level that could trip the CB. For this reason, a resistor R1 is often used to limit the current in the event of a short-circuited opto-input. This limits the current to less than 60mA. The table below shows the appropriate resistor value and voltage setting for this scheme.

Trip Circuit Voltage	Opto Voltage Setting with R1 Fitted	Resistor R1 (ohms)
48/54	24/27	1.2k

Trip Circuit Voltage	Opto Voltage Setting with R1 Fitted	Resistor R1 (ohms)
110/125	48/54	2.7k
220/250	110/125	5.2k



Warning:

This Scheme is not compatible with Trip Circuit voltages of less than 48 V.

4.1.2 PSL FOR TCS SCHEME 1

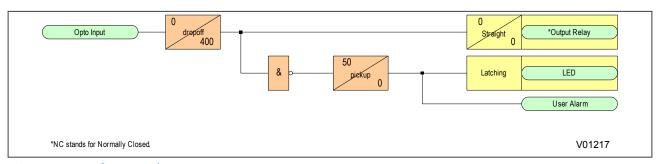


Figure 190: PSL for TCS Scheme 1

The opto-input can be used to drive a Normally Closed Output Relay, which in turn can be used to drive alarm equipment. The signal can also be inverted to drive a latching programmable LED and a user alarm DDB signal.

The DDO timer operates as soon as the opto-input is energised, but will take 400 ms to drop off/reset in the event of a trip circuit failure. The 400 ms delay prevents a false alarm due to voltage dips caused by faults in other circuits or during normal tripping operation when the opto-input is shorted by a self-reset trip contact. When the timer is operated the NC (normally closed) output relay opens and the LED and user glarms are reset.

The 50 ms delay on pick-up timer prevents false LED and user alarm indications during the power up time, following a voltage supply interruption.

4.2 TRIP CIRCUIT SUPERVISION SCHEME 2

This scheme provides supervision of the trip coil with the breaker open or closed but does not provide pre-closing supervision of the trip path. However, using two opto-inputs allows the IED to correctly monitor the circuit breaker status since they are connected in series with the CB auxiliary contacts. This is achieved by assigning one opto-input to the 52a contact and another opto-input to the 52b contact. Provided the *CB Status* setting in the *CB CONTROL* column is set to *Both 52A and 52B*, the IED will correctly monitor the status of the breaker. This scheme is also fully compatible with latched contacts as the supervision current will be maintained through the 52b contact when the trip contact is closed.

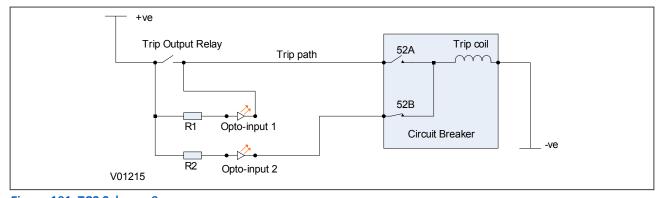


Figure 191: TCS Scheme 2

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When the breaker is closed, supervision current passes through opto input 1 and the trip coil. When the breaker is open current flows through opto input 2 and the trip coil. No supervision of the trip path is provided whilst the breaker is open. Any fault in the trip path will only be detected on CB closing, after a 400 ms delay.

4.2.1 RESISTOR VALUES

Optional resistors R1 and R2 can be added to prevent tripping of the CB if either opto-input is shorted. The table below shows the appropriate resistor value and voltage setting for this scheme.

Trip Circuit Voltage	Opto Voltage Setting with R1 Fitted	Resistor R1 and R2 (ohms)
48/54	24/27	1.2k
110/125	48/54	2.7k
220/250	110/125	5.2k



Warning:

This Scheme is not compatible with Trip Circuit voltages of less than 48 V.

4.2.2 PSL FOR TCS SCHEME 2

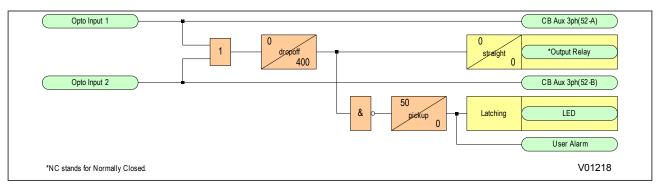


Figure 192: PSL for TCS Scheme 2

In TCS scheme 2, both opto-inputs must be low before a trip circuit fail alarm is given.

4.3 TRIP CIRCUIT SUPERVISION SCHEME 3

TCS Scheme 3 is designed to provide supervision of the trip coil with the breaker open or closed. It provides preclosing supervision of the trip path. Since only one opto-input is used, this scheme is not compatible with latched trip contacts. If you require CB status monitoring, further opto-inputs must be used.

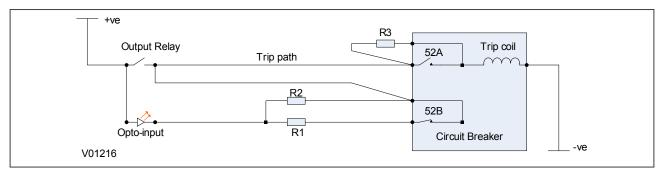


Figure 193: TCS Scheme 3

When the CB is closed, supervision current passes through the opto-input, resistor R2 and the trip coil. When the CB is open, current flows through the opto-input, resistors R1 and R2 (in parallel), resistor R3 and the trip coil. The

supervision current is maintained through the trip path with the breaker in either state, therefore providing preclosing supervision.

4.3.1 RESISTOR VALUES

Resistors R1 and R2 are used to prevent false tripping, if the opto-input is accidentally shorted. However, unlike the other two schemes. This scheme is dependent upon the position and value of these resistors. Removing them would result in incomplete trip circuit monitoring. The table below shows the resistor values and voltage settings required for satisfactory operation.

Trip Circuit Voltage	Opto Voltage Setting with R1 Fitted	Resistor R1 & R2 (ohms)	Resistor R3 (ohms)
48/54	24/27	1.2k	600
110/250	48/54	2.7k	1.2k
220/250	110/125	5.0k	2.5k



Warning:

This Scheme is not compatible with Trip Circuit voltages of less than 48 V.

4.3.2 PSL FOR TCS SCHEME 3

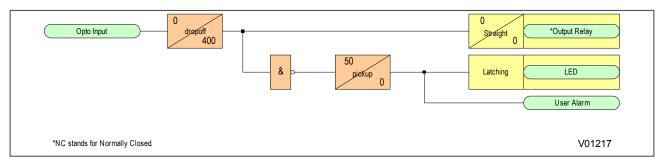


Figure 194: PSL for TCS Scheme 3

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P14x

CHAPTER 16

DIGITAL I/O AND PSL CONFIGURATION

1 CHAPTER OVERVIEW

This chapter introduces the PSL (Programmable Scheme Logic) Editor, and describes the configuration of the digital inputs and outputs. It provides an outline of scheme logic concepts and the PSL Editor. This is followed by details about allocation of the digital inputs and outputs, which require the use of the PSL Editor. A separate "Settings Application Software" document is available that gives a comprehensive description of the PSL, but enough information is provided in this chapter to allow you to allocate the principal digital inputs and outputs.

This chapter contains the following sections:

Chapter Overview	363
Configuring Digital Inputs and Outputs	364
Scheme Logic	365
Configuring the Opto-Inputs	367
Assigning the Output Relays	368
Fixed Function LEDs	369
Configuring Programmable LEDs	370
Function Keys	372
Control Inputs	373

2 CONFIGURING DIGITAL INPUTS AND OUTPUTS

Configuration of the digital inputs and outputs in this product is very flexible. You can use a combination of settings and programmable logic to customise them to your application. You can access some of the settings using the keypad on the front panel, but you will need a computer running the settings application software to fully interrogate and configure the properties of the digital inputs and outputs.

The settings application software includes an application called the PSL Editor (Programmable Scheme Logic Editor). The PSL Editor lets you allocate inputs and outputs according to your specific application. It also allows you to apply attributes to some of the signals such as a drop-off delay for an output contact.

In this product, digital inputs and outputs that are configurable are:

- Optically isolated digital inputs (opto-inputs). These can be used to monitor the status of associated plant.
- Output relays. These can be used for purposes such as initiating the tripping of circuit breakers, providing alarm signals, etc..
- Programmable LEDs. The number and colour of the programmable LEDs varies according to the particular product being applied.
- Function keys and associated LED indications. These are not provided on all products, but where they are, each function key has an associated tri-colour LED.
- IEC 61850 GOOSE inputs and outputs. These are only provided on products that have been specified for connection to an IEC61850 system, and the details of the GOOSE are presented in the documentation on IEC61850.
- InterMiCOM inputs and outputs. These are not used by all products. If your product is equipped with an InterMiCOM feature, you will find details of allocation and configuration in the chapter dedicated to the InterMiCOM function.

3 SCHEME LOGIC

The product is supplied with pre-loaded Fixed Scheme Logic (FSL) and Programmable Scheme Logic (PSL).

The Scheme Logic is a functional module within the IED, through which all mapping of inputs to outputs is handled. The scheme logic can be split into two parts; the Fixed Scheme Logic (FSL) and the Programmable Scheme Logic (PSL). It is built around a concept called the digital data bus (DDB). The DDB encompasses all of the digital signals (DDBs) which are used in the FSL and PSL. The DDBs included digital inputs, outputs, and internal signals.

The FSL is logic that has been hard-coded in the product. It is fundamental to correct interaction between various protection and/or control elements. It is fixed and cannot be changed.

The PSL gives you a facility to develop custom schemes to suit your application if the factory-programmed default PSL schemes do not meet your needs. Default PSL schemes are programmed before the product leaves the factory. These default PSL schemes have been designed to suit typical applications and if these schemes suit your requirements, you do not need to take any action. However, if you want to change the input-output mappings, or to implement custom scheme logic, you can change these, or create new PSL schemes using the PSL editor.

The PSL consists of components such as logic gates and timers, which combine and condition DDB signals.

The logic gates can be programmed to perform a range of different logic functions. The number of inputs to a logic gate are not limited. The timers can be used either to create a programmable delay or to condition the logic outputs. Output contacts and programmable LEDs have dedicated conditioners.

The PSL logic is event driven. Only the part of the PSL logic that is affected by the particular input change that has occurred is processed. This minimises the amount of processing time used by the PSL ensuring industry leading performance.

The following diagram shows how the scheme logic interacts with the rest of the IED.

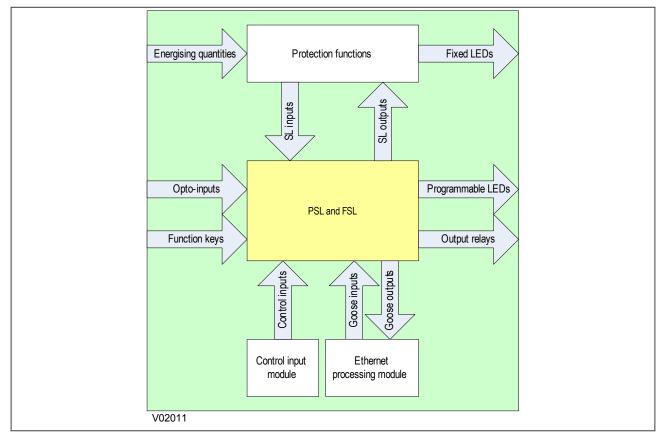


Figure 195: Scheme Logic Interfaces

3.1 PSL EDITOR

The Programmable Scheme Logic (PSL) is a module of programmable logic gates and timers in the IED, which can be used to create customised logic to qualify how the product manages its response to system conditions. The IED's digital inputs are combined with internally generated digital signals using logic gates, timers, and conditioners. The resultant signals are then mapped to digital outputs signals including output relays and LEDs.

The PSL Editor is a tool in the settings application software that allows you to create and edit scheme logic diagrams. You can use the default scheme logic which has been designed to suit most applications, but if it does not suit your application you can change it. If you create a different scheme logic with the software, you need to upload it to the device to apply it.

3.2 PSL SCHEMES

Your product is shipped with default scheme files. These can be used without modification for most applications, or you can choose to use them as a starting point to design your own scheme. You can also create a new scheme from scratch. To create a new scheme, or to modify an existing scheme, you will need to launch the settings application software. You then need to open an existing PSL file, or create a new one, for the particular product that you are using, and then open a PSL file. If you want to create a new PSL file, you should select **File** then **New** then **Blank scheme...** This action opens a default file appropriate for the device in question, but deletes the diagram components from the default file to leave an empty diagram with configuration information loaded. To open an existing file, or a default file, simply double-click on it.

3.3 PSL SCHEME VERSION CONTROL

To help you keep track of the PSL loaded into products, a version control feature is included. The user interface contains a *PSL DATA* column, which can be used to track PSL modifications. A total of 12 cells are contained in the *PSL DATA* column; 3 for each setting group.

Grp(n) PSL Ref: When downloading a PSL scheme to an IED, you will be prompted to enter the relevant group number and a reference identifier. The first 32 characters of the reference identifier are displayed in this cell. The horizontal cursor keys can scroll through the 32 characters as the LCD display only displays 16 characters.

Example:

Grp(n) PSL Ref

Date/time: This cell displays the date and time when the PSL scheme was downloaded to the IED.

Example:

18 Nov 2002 08:59:32.047

Grp(n) PSL ID: This cell displays a unique ID number for the downloaded PSL scheme.

Example:

Grp(n) PSL ID ID - 2062813232

4 CONFIGURING THE OPTO-INPUTS

The number of optically isolated status inputs (opto-inputs) depends on the specific model supplied. The use of the inputs will depend on the application, and their allocation is defined in the programmable scheme logic (PSL). In addition to the PSL assignment, you also need to specify the expected input voltage. Generally, all opto-inputs will share the same input voltage range, but if different voltage ranges are being used, this device can accommodate them.

In the OPTO CONFIG column there is a global nominal voltage setting. If all opto-inputs are going to be energised from the same voltage range, you select the appropriate value in the setting. If you select Custom in the setting, then the cells **Opto Input 1**, **Opto Input 2**, etc. become visible. You use these cells to set the voltage ranges for each individual opto-input.

Within the *OPTO CONFIG* column there are also settings to control the filtering applied to the inputs, as well as the pick-up/drop-off characteristic.

The filter control setting provides a bit string with a bit associated with all opto-inputs. Setting the bit to '1' means that a half-cycle filter is applied to the inputs. This helps to prevent incorrect operation in the event of power system frequency interference on the wiring. Setting the field to '0' removes the filter and provides for faster operation.

The *Characteristic* setting is a single setting that applies to all the opto-inputs. It is used to set the pick-up/drop-off ratios of the input signals. As standard it is set to 80% pick-up and 60% drop-off, but you can change it to other available thresholds if that suits your operational requirements.

5 ASSIGNING THE OUTPUT RELAYS

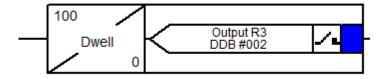
Relay contact action is controlled using the PSL. DDB signals are mapped in the PSL and drive the output relays. The driving of an output relay is controlled by means of a relay output conditioner. Several choices are available for how output relay contacts are conditioned. For example, you can choose whether operation of an output relay contact is latched, has delay on pick-up, or has a delay on drop-off. You make this choice in the **Contact Properties** window associated with the output relay conditioner.

To map an output relay in the PSL you should use the Contact Conditioner button in the toolbar to import it. You then condition it according to your needs. The output of the conditioner respects the attributes you have assigned.

The toolbar button for a Contact Conditioner looks like this:



The PSL contribution that it delivers looks like this:



Note:

Contact Conditioners are only available if they have not all been used. In some default PSL schemes, all Contact Conditioners might have been used. If that is the case, and you want to use them for something else, you will need to re-assign them.

On the toolbar there is another button associated with the relay outputs. The button looks like this:



This is the "Contact Signal" button. It allows you to put replica instances of a conditioned output relay into the PSL, preventing you having to make cross-page connections which might detract from the clarity of the scheme.

6 FIXED FUNCTION LEDS

Four fixed-function LEDs on the left-hand side of the front panel indicate the following conditions.

- Trip (Red) switches ON when the IED issues a trip signal. It is reset when the associated fault record is cleared from the front display. Also the trip LED can be configured as self-resetting.
- Alarm (Yellow) flashes when the IED registers an alarm. This may be triggered by a fault, event or maintenance record. The LED flashes until the alarms have been accepted (read), then changes to constantly ON. When the alarms are cleared, the LED switches OFF.
- Out of service (Yellow) is ON when the IED's functions are unavailable.
- Healthy (Green) is ON when the IED is in correct working order, and should be ON at all times. It goes OFF if
 the unit's self-tests show there is an error in the hardware or software. The state of the healthy LED is
 reflected by the watchdog contacts at the back of the unit.

6.1 TRIP LED LOGIC

When a trip occurs, the trip LED is illuminated. It is possible to reset this with a number of ways:

- Directly with a reset command (by pressing the Clear Key)
- With a reset logic input
- · With self-resetting logic

You enable the automatic self-resetting with the **Sys Fn Links** cell in the SYSTEM DATA column. A '0' disables self resetting and a '1' enables self resetting.

The reset occurs when the circuit is reclosed and the *Any Pole Dead* signal has been reset for three seconds providing the *Any Start* signal is inactive. The reset is prevented if the *Any Start* signal is active after the breaker closes.

The Trip LED logic is as follows:

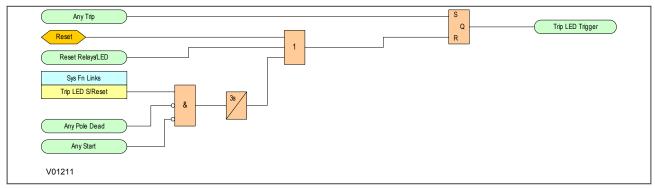


Figure 196: Trip LED logic

7 CONFIGURING PROGRAMMABLE LEDS

There are three types of programmable LED signals which vary according to the model being used. These are:

- Single-colour programmable LED. These are red when illuminated.
- Tri-colour programmable LED. These can be illuminated red, green, or amber.
- Tri-colour programmable LED associated with a Function Key. These can be illuminated red, green, or amber.

DDB signals are mapped in the PSL and used to illuminate the LEDs. For single-coloured programmable LEDs there is one DDB signal per LED. For tri-coloured LEDs there are two DDB signals associated with the LED. Asserting *LED # Grn* will illuminate the LED green. Asserting *LED # Red* will illuminate the LED red. Asserting both DDB signals will illuminate the LED amber.

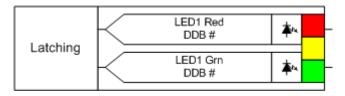
The illumination of an LED is controlled by means of a conditioner. Using the conditioner, you can decide whether the LEDs reflect the real-time state of the DDB signals, or whether illumination is latched pending user intervention.

To map an LED in the PSL you should use the LED Conditioner button in the toolbar to import it. You then condition it according to your needs. The output(s) of the conditioner respect the attribute you have assigned.

The toolbar button for a tri-colour LED looks like this:



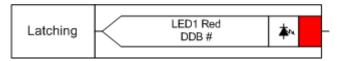
The PSL contribution that it delivers looks like this:



The toolbar button for a single-colour LED looks like this:



The PSL contribution that it delivers looks like this.



Note:

LED Conditioners are only available if they have not all been used up, and in some default PSL schemes they might be. If that is the case and you want to use them for something else, you will need to re-assign them.

On the toolbar there is another button associated with the LEDs. For a tri-coloured LED the button looks like this:



For a single-colour LED it looks like this:



It is the "LED Signal" button. It allows you to put replica instances of a conditioned LED into the PSL, preventing you having to make cross-page connections which might detract from the clarity of the scheme.

Note:

All LED DDB signals are always shown in the PSL Editor. However, the actual number of LEDs depends on the device hardware. For example, if a small 20TE device has only 4 programmable LEDs, LEDs 5-8 will not take effect even if they are mapped in the PSL.

8 FUNCTION KEYS

For most models, a number of programmable function keys are available. This allows you to assign function keys to control functionality via the programmable scheme logic (PSL). Each function key is associated with a programmable tri-colour LED, which you can program to give the desired indication on activation of the function key.

These function keys can be used to trigger any function that they are connected to as part of the PSL. The function key commands are found in the *FUNCTION KEYS* column.

Each function key is associated with a DDB signal as shown in the DDB table. You can map these DDB signals to any function available in the PSL.

The *Fn Key Status* cell displays the status (energised or de-energised) of the function keys by means of a binary string, where each bit represents a function key starting with bit 0 for function key 1.

Each function key has three settings associated with it, as shown:

- Fn Key (n), which enables or disables the function key
- Fn Key (n) Mode, which allows you to configure the key as toggled or normal
- Fn Key (n) label, which allows you to define the function key text that is displayed

The Fn Key (n) cell is used to enable (unlock) or disable (unlock) the function key signals in PSL. The Lock setting has been provided to prevent further activation on subsequent key presses. This allows function keys that are set to Toggled mode and their DDB signal active 'high', to be locked in their active state therefore preventing any further key presses from deactivating the associated function. Locking a function key that is set to the "Normal" mode causes the associated DDB signals to be permanently off. This safety feature prevents any inadvertent function key presses from activating or deactivating critical functions.

When the **Fn Key (n) Mode** cell is set to Toggle, the function key DDB signal output will remain in the set state until a reset command is given. In the Normal mode, the function key DDB signal will remain energised for as long as the function key is pressed and will then reset automatically. In this mode, a minimum pulse duration can be programmed by adding a minimum pulse timer to the function key DDB output signal.

The *Fn Key Label* cell makes it possible to change the text associated with each individual function key. This text will be displayed when a function key is accessed in the function key menu, or it can be displayed in the PSL.

The status of all function keys are recorded in non-volatile memory. In case of auxiliary supply interruption their status will be maintained.

Note:

All function key DDB signals are always shown in the PSL Editor. However, the actual number of function keys depends on the device hardware. For example, if a small 20TE device has no function keys, the function key DDBs mapped in the PSL will not take effect.

9 CONTROL INPUTS

The control inputs are software switches, which can be set or reset locally or remotely. These inputs can be used to trigger any PSL function to which they are connected. There are three setting columns associated with the control inputs: CONTROL INPUTS, CTRL I/P CONFIG and CTRL I/P LABELS. These are listed in the Settings and Records appendix at the end of this manual.

CHAPTER 17

ELECTRICAL TELEPROTECTION

1 CHAPTER OVERVIEW	
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Teleprotection Scheme Principles	379

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Application Notes 384

2 INTRODUCTION

Electrical Teleprotection is an optional feature that uses communications links to create protection schemes. It can be used to replace hard wiring between dedicated relay output contacts and digital input circuits. Two products equipped with electrical teleprotection can connect and exchange commands using a communication link. It is typically used to implement teleprotection schemes.

Using full duplex communications, eight binary command signals can be sent in each direction between connected products. The communication connection complies with the EIA(RS)232 standard. Ports may be connected directly, or using modems. Alternatively EIA(RS)232 converters can be used for connecting to other media such as optical fibres.

Communications statistics and diagnostics enable you to monitor the integrity of the communications link, and a loopback feature is available to help with testing.

3 TELEPROTECTION SCHEME PRINCIPLES

Teleprotection schemes use signalling to convey a trip command to remote circuit breakers to isolate circuits. Three types of teleprotection commands are commonly encountered:

- Direct Tripping
- Permissive Tripping
- Blocking Scheme

3.1 DIRECT TRIPPING

In direct tripping applications (often described by the generic term: "intertripping"), teleprotection signals are sent directly to a master trip device. Receipt of a command causes circuit breaker operation without any further qualification. Communication must be reliable and secure because any signal detected at the receiving end causes a trip of the circuit at that end. The communications system must be designed so that interference on the communication circuit does not cause spurious trips. If a spurious trip occurs, the primary system might be unnecessarily isolated.

3.2 PERMISSIVE TRIPPING

Permissive trip commands are monitored by a protection device. The circuit breaker is tripped when receipt of the command coincides with a 'start' condition being detected by the protection at the receiving. Requirements for the communications channel are less onerous than for direct tripping schemes, since receipt of an incorrect signal must coincide with a 'start' of the receiving end protection for a trip operation to take place. Permissive tripping is used to speed up tripping for faults occurring within a protected zone.

4 IMPLEMENTATION

Electrical InterMiCOM is configured using a combination of settings in the *INTERMICOM COMMS* column, settings in the *INTERMICOM CONF* column, and the programmable scheme logic (PSL).

The eight command signals are mapped to DDB signals within the product using the PSL.

Signals being sent to a remote terminal are referenced in the PSL as *InterMiCOM out 1 - InterMiCOM out 8*. Signals received from the remote terminal are referenced as *InterMiCOM in 1 - InterMiCOM in 8*.

5 CONFIGURATION

Electrical Teleprotection is compliant with IEC 60834-1:1999. For your application, you can customise individual command signals to the differing requirements of security, speed, and dependability as defined in this standard.

You customise the command signals using the *IM# Cmd Type* cell in the *INTERMICOM CONF* column.

Any command signal can be configured for:

- Direct intertripping by selecting 'Direct'. (this is the most secure signalling but incurs a time delay to deliver the security).
- Blocking applications by selecting 'Blocking'. (this is the fastest signalling)
- Permissive intertripping applications by selecting 'Permissive. (this is dependable signalling that balances speed and security)

You can also select to 'Disable' the command.

Note:

When used in the context of a setting, '#' specifies which command signal (1-8) bit is being configured.

To ensure that command signals are processed only by their intended recipient, the command signals are packaged into a message (sometimes referred to as a telegram) which contains an address field. A sending device sets a pattern in this field. A receiving device must be set to match this pattern in the address field before the commands will be acted upon. 10 patterns have been carefully chosen for maximum security. You need to choose which ones to use, and set them using the *Source Address* and *Receive Address* cells in the *INTERMICOM COMMS* column.

The value set in the **Source Address** of the transmitting device should match that set in the **Receive Address** of the receiving device. For example set **Source Address** to 1 at a local terminal and set **Receive Address** to 1 at the remote terminal.

The Source Address and Receive Address settings in the device should be set to different values to avoid false operation under inadvertent loopback conditions.

Where more than one pair of devices is likely to share a communication link, you should set each pair to use a different pair of address values.

Electrical InterMiCOM has been designed to be resilient to noise on communications links, but during severe noise conditions, the communication may fail. If this is the case, an alarm is raised and you can choose how the input signals are managed using the *IM# FallBackMode* cell in the *INTERMICOM CONF* column:

- If you choose *Latched*, the last valid command to be received can be maintained until a new valid message is received.
- If you choose *Default*, the signal will revert to a default value after the period defined in the *IM#*FrameSyncTim setting has expired. You choose the default value using the *IM# DefaultValue* setting.

Subsequent receipt of a full valid message will reset the alarm, and the new command signals will be used.

As well as the settings described above, you will need to assign input and output signals in the Programmable Scheme Logic (PSL). Use the 'Integral Tripping' buttons to create the logic you want to apply. A typical example is shown below.

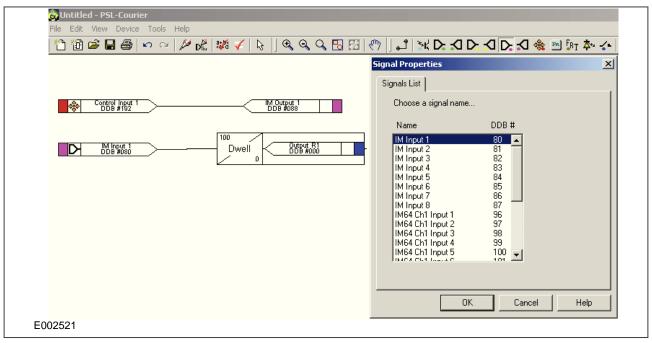


Figure 197: Example assignment of InterMiCOM signals within the PSL

Note:

When an Electrical InterMiCOM signal is sent from a local terminal, only the remote terminal will react to the command. The local terminal will only react to commands initiated at the remote terminal.

6 CONNECTING TO ELECTRICAL INTERMICOM

Electrical InterMiCOM uses EIA(RS)232 communication presented on a 9-pin 'D' type connector. The connector is labelled SK5 and is located at the bottom of the 2nd Rear communication board. The port is configured as standard DTE (Data Terminating Equipment).

6.1 SHORT DISTANCE

EIA(RS)232 is suitable for short distance connections only - less than 15m. Where this limitation is not a problem, direct connection between devices is possible. For this case, inter-device connections should be made as shown below the figure below.

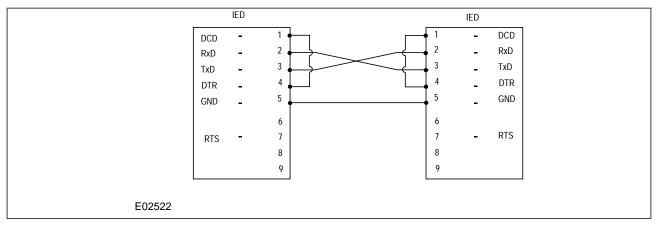


Figure 198: Direct connection

For direct connection, the maximum baud rate can generally be used.

6.2 LONG DISTANCE

EIA(RS)232 is suitable for short distance connections only - less than 15m. Where this limitation is a problem, direct connection between devices is not possible. For this case, inter-device connections should be made as shown below the figure below.

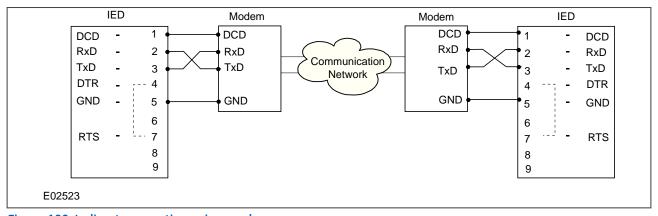


Figure 199: Indirect connection using modems

This type of connection should be used when connecting to devices that have the ability to control the DCD line. The baud rate should be chosen to be suitable for the communications network. If the Modem does not support the DCD function, the DCD terminal on the IED should be connected to the DTR terminal.

7 APPLICATION NOTES

Electrical InterMiCOM settings are contained within two columns; INTERMICOM COMMS and INTERMICOM CONF. The INTERMICOM COMMS column contains all the settings needed to configure the communications, as well as the channel statistics and diagnostic facilities. The INTERMICOM CONF column sets the mode of each command signal and defines how they operate in case of signalling failure.

Short metallic direct connections and connections using fire-optic converters will generally be set to have the highest signalling speed of 19200b/s. Due to this high signalling rate, the difference in operating time between the direct, permissive, and blocking type signals is small. This means you can select the most secure signalling command type ('Direct' intertrip) for all commands. You do this with the *IM# Cmd Type* settings. For these applications you should set the *IM# Fallback Mode* to Default. You should also set a minimal intentional delay by setting *IM# FrameSyncTim* to 10 msecs. This ensures that whenever two consecutive corrupt messages are received, the command will immediately revert to the default value until a new valid message is received.

For applications that use Modem and/or multiplexed connections, the trade-off between speed, security, and dependability is more critical. Choosing the fastest baud rate (data rate) to achieve maximum speed may appear attractive, but this is likely to increase the cost of the telecommunications equipment. Also, telecommunication services operating at high data rates are more prone to interference and suffer from longer re-synchronisation times following periods of disruption. Taking into account these factors we recommend a maximum baud rate setting of 9600 bps. As baud rates decrease, communications become more robust with fewer interruptions, but overall signalling times increase.

At slower baud rates, the choice of signalling mode becomes significant. You should also consider what happens during periods of noise when message structure and content can be lost.

- In 'Blocking' mode, the likelihood of receiving a command in a noisy environment is high. In this case, we recommend you set IM# Fallback Mode to Default, with a reasonably long IM# FrameSyncTim setting.
 Set IM# DefaultValue to '1'. This provides a substitute for a received blocking signal, applying a failsafe for blocking schemes.
- In 'Direct' mode, the likelihood of receiving commands in a noisy environment is small. In this case, we recommend you set IM# Fallback Mode to Default with a short IM# FrameSyncTim setting. Set IM# DefaultValue to '0'. This means that if a corrupt message is received, InterMiCOM will use the default value. This provides a substitute for the intertrip signal not being received, applying a failsafe for direct intertripping schemes.
- In 'Permissive' mode, the likelihood of receiving a valid command under noisy communications conditions is somwhere between that of the 'Blocking' mode and the 'Direct' intertrip mode. In this case, we recommended you set *IM# Fallback Mode* to *Latched*.

The table below presents recommended *IM# FrameSyncTim* settings for the different signalling modes and baud rates:

	Minimum Recommended "IN			
Baud Rate	Direct Intertrip Mode	Blocking Mode	Minimum Setting (ms)	Maximum Setting (ms)
600	100	250	100	1500
1200	50	130	50	1500
2400	30	70	30	1500
4800	20	40	20	1500
9600	10	20	10	1500
19200	10	10	10	1500

Note:

As we have recommended Latched operation, the table does not contain recommendations for 'Permissive' mode. However, if you do select 'Default' mode, you should set **IM# FrameSyncTim** greater than those listed above. If you set **IM# FrameSyncTim** lower than the minimum setting listed above, the device could interpret a valid change in a message as a corrupted message.

We recommend a setting of 25% for the communications failure alarm.

CHAPTER 18

COMMUNICATIONS

1 CHAPTER OVERVIEW

This product supports Substation Automation System (SAS), and Supervisory Control and Data Acquisition (SCADA) communication. The support embraces the evolution of communications technologies that have taken place since microprocessor technologies were introduced into protection, control, and monitoring devices which are now ubiquitously known as Intelligent Electronic Devices for the substation (IEDs).

As standard, all products support rugged serial communications for SCADA and SAS applications. By option, any product can support Ethernet communications for more advanced SCADA and SAS applications.

This chapter contains the following sections:

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Standard Ethernet Communication	394	
Redundant Ethernet Communication	395	
Simple Network Management Protocol (SNMP)		
Data Protocols		
Read Only Mode		
Time Synchronisation	456	

2 COMMUNICATION INTERFACES

The products have a number of standard and optional communication interfaces. The standard and optional hardware and protocols are summarised below:

Port	Availability	Physical layer	Use	Data Protocols
Front	Standard	RS232	Local settings	Courier
Rear Port 1 (RP1 copper)	Standard	RS232 / RS485 / K- Bus	SCADA Remote settings	Courier, MODBUS, IEC60870-5-103, DNP3.0 (order option)
Rear Port 1 (RP1 fibre)	Optional	Fibre	SCADA Remote settings	Courier, MODBUS, IEC60870-5-103, DNP3.0 (order option)
Rear Port 2 (RP2)	Optional	RS232 / RS485 / K- Bus	SCADA Remote settings	SK4: Courier only SK5: InterMicom only
Ethernet	Optional	Ethernet	IEC 61850 or DNP3 Remote settings	IEC 61850, Courier (tunnelled) or DNP3.0 (order option)

Note:

Optional communications boards are always fitted into slot A.

Note:

It is only possible to fit one optional communications board, therefore RP2 and Ethernet communications are mutually exclusive.

3 SERIAL COMMUNICATION

The physical layer standards that are used for serial communications for SCADA purposes are:

- EIA(RS)485 (often abbreviated to RS485)
- K-Bus (a proprietary customization of RS485)

EIA(RS)232 is used for local communication with the IED (for transferring settings and downloading firmware updates).

RS485 is similar to RS232 but for longer distances and it allows daisy-chaining and multi-dropping of IEDs.

K-Bus is a proprietary protocol quite similar to RS485, but it cannot be mixed on the same link as RS485. Unlike RS485, K-Bus signals applied across two terminals are not polarised.

It is important to note that these are not data protocols. They only describe the physical characteristics required for two devices to communicate with each other.

For a description of the K-Bus standard see K-Bus (on page 392) and General Electric's K-Bus interface guide reference R6509.

A full description of the RS485 is available in the published standard.

3.1 EIA(RS)232 BUS

The EIA(RS)232 interface uses the IEC 60870-5 FT1.2 frame format.

The device supports an IEC 60870-5 FT1.2 connection on the front-port. This is intended for temporary local connection and is not suitable for permanent connection. This interface uses a fixed baud rate of 19200 bps, 11-bit frame (8 data bits, 1 start bit, 1 stop bit, even parity bit), and a fixed device address of '1'.

EIA(RS)232 interfaces are polarised.

3.2 EIA(RS)485 BUS

The RS485 two-wire connection provides a half-duplex, fully isolated serial connection to the IED. The connection is polarized but there is no agreed definition of which terminal is which. If the master is unable to communicate with the product, and the communication parameters match, then it is possible that the two-wire connection is reversed.

The RS485 bus must be terminated at each end with $120 \Omega 0.5$ W terminating resistors between the signal wires.

The RS485 standard requires that each device be directly connected to the actual bus. Stubs and tees are forbidden. Loop bus and Star topologies are not part of the RS485 standard and are also forbidden.

Two-core screened twisted pair cable should be used. The final cable specification is dependent on the application, although a multi-strand 0.5 mm² per core is normally adequate. The total cable length must not exceed 1000 m. It is important to avoid circulating currents, which can cause noise and interference, especially when the cable runs between buildings. For this reason, the screen should be continuous and connected to ground at one end only, normally at the master connection point.

The RS485 signal is a differential signal and there is no signal ground connection. If a signal ground connection is present in the bus cable then it must be ignored. At no stage should this be connected to the cable's screen or to the product's chassis. This is for both safety and noise reasons.

It may be necessary to bias the signal wires to prevent jabber. Jabber occurs when the signal level has an indeterminate state because the bus is not being actively driven. This can occur when all the slaves are in receive mode and the master is slow to turn from receive mode to transmit mode. This may be because the master is waiting in receive mode, in a high impedance state, until it has something to transmit. Jabber causes the receiving device(s) to miss the first bits of the first character in the packet, which results in the slave rejecting the message and consequently not responding. Symptoms of this are; poor response times (due to retries), increasing message error counts, erratic communications, and in the worst case, complete failure to communicate.

3.2.1 EIA(RS)485 BIASING REQUIREMENTS

Biasing requires that the signal lines be weakly pulled to a defined voltage level of about 1 V. There should only be one bias point on the bus, which is best situated at the master connection point. The DC source used for the bias must be clean to prevent noise being injected.

Note:

Some devices may be able to provide the bus bias, in which case external components would not be required.

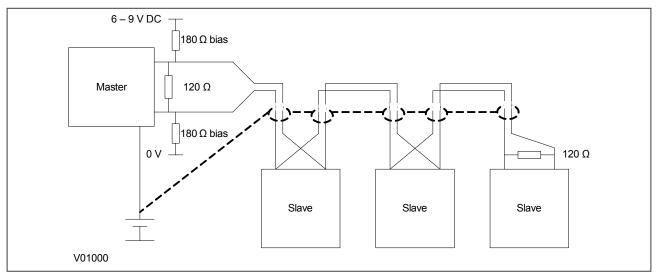


Figure 200: RS485 biasing circuit



Warning:

It is extremely important that the 120 Ω termination resistors are fitted. Otherwise the bias voltage may be excessive and may damage the devices connected to the bus.

3.3 K-BUS

K-Bus is a robust signalling method based on RS485 voltage levels. K-Bus incorporates message framing, based on a 64 kbps synchronous HDLC protocol with FM0 modulation to increase speed and security.

The rear interface is used to provide a permanent connection for K-Bus, which allows multi-drop connection.

A K-Bus spur consists of up to 32 IEDs connected together in a multi-drop arrangement using twisted pair wiring. The K-Bus twisted pair connection is non-polarised.

It is not possible to use a standard EIA(RS)232 to EIA(RS)485 converter to convert IEC 60870-5 FT1.2 frames to K-Bus. A protocol converter, namely the KITZ101, KITZ102 or KITZ201, must be used for this purpose. Please consult General Electric for information regarding the specification and supply of KITZ devices. The following figure demonstrates a typical K-Bus connection.

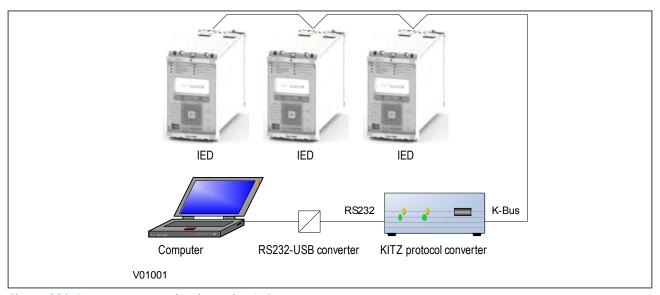


Figure 201: Remote communication using K-Bus

Note:

An RS232-USB converter is only needed if the local computer does not provide an RS232 port.

Further information about K-Bus is available in the publication R6509: K-Bus Interface Guide, which is available on request.

4 STANDARD ETHERNET COMMUNICATION

The type of Ethernet board depends on the chosen model. The available boards and their features are described in the Hardware Design chapter of this manual.

The Ethernet interface is required for either IEC 61850 or DNP3 over Ethernet (protocol must be selected at time of order). With either of these protocols, the Ethernet interface also offers communication with the settings application software for remote configuration and record extraction.

Fibre optic connection is recommended for use in permanent connections in a substation environment, as it offers advantages in terms of noise rejection. The fibre optic port provides 100 Mbps communication and uses type BFOC 2.5 (ST) connectors. Fibres should be suitable for 1300 nm transmission and be multimode $50/125 \, \mu m$ or $62.5/125 \, \mu m$.

Connection can also be made to a 10Base-T or a 100Base-TX Ethernet switch using the RJ45 port.

4.1 HOT-STANDBY ETHERNET FAILOVER

This is used for products which are fitted with a standard Ethernet board. The standard Ethernet board has one fibre and one copper interface. If there is a fault on the fibre channel it can switch to the copper channel, or vice versa.

When this function detects a link failure, it generates the NIC Fail Alarm. The failover timer then starts, which has a settable timeout. During this time, the Hot Standby Failover function continues to check the status of the other channel. If the link failure recovers before the failover timer times out, the channels are not swapped over. If there is still a fail when the failover timer times out and the other channel status is ok, the channels are swapped over. The Ethernet controller is then reconfigured and the link is renegotiated.

To set the function, use the IEC 61850 Configurator tool in the Settings Application Software.

5 REDUNDANT ETHERNET COMMUNICATION

Redundancy is required where a single point of failure cannot be tolerated. It is required in critical applications such as substation automation. Redundancy acts as an insurance policy, providing an alternative route if one route fails.

Ethernet communication redundancy is available for most General Electric products, using a Redundant Ethernet Board (REB). The REB is a Network Interface Card (NIC), which incorporates an integrated Ethernet switch. The board provides two Ethernet transmitter/receiver pairs.

By ordering option, a number of different protocols are available to provide the redundancy according to particular system requirements.

In addition to the two Ethernet transmitter/receiver pairs, the REB provides link activity indication in the form of LEDs, link fail indication in the form of watchdog contacts, and a dedicated time synchronisation input.

The dedicated time synchronisation input is designed to connect to an IRIG-B signal. Both modulated and unmodulated IRIG-B formats are supported according to the selected option. Simple Network Time Protocol (SNTP) is supported over the Ethernet communications.

5.1 SUPPORTED PROTOCOLS

A range of Redundant Ethernet Boards are available to support different protocols for different requirements. One of the key requirements of substation redundant communications is "bumpless" redundancy. This means the ability to transfer from one communication path to another without noticeable consequences. Standard protocols of the time could not meet the demanding requirements of network availability for substation automation solutions. Switch-over times were unacceptably long. For this reason, companies developed proprietary protocols. More recently, however, standard protocols, which support bumpless redundancy (namely PRP and HSR) have been developed and ratified.

As well as supporting standard non-bumpless protocols such as RSTP, the REB was originally designed to support bumpless redundancy, using proprietary protocols (SHP, DHP) before the standard protocols became available. Since then, variants have been produced for the newer standard protocols.

REB variants for each of the following protocols are available:

- PRP (Parallel Redundancy Protocol)
- HSR (High-availability Seamless Redundancy)
- RSTP (Rapid Spanning Tree Protocol)
- SHP (Self-Healing Protocol)
- DHP (Dual Homing Protocol)

PRP and HSR are open standards, so their implementation is compatible with any standard PRP or HSR device respectively. PRP provides "bumpless" redundancy. RSTP is also an open standard, so its implementation is compatible with any standard RSTP devices. RSTP provides redundancy, however, it is not "bumpless".

SHP and DHP are proprietary protocols intended for use with specific General Electric products:

- SHP is compatible with the C264-SWR212 as well as H35x multimode switches.
- DHP is compatible with the C264-SWD212 as well as H36x multimode switches.

Both SHP and DHP provide "bumpless" redundancy.

Note:

The protocol you require must be selected at the time of ordering.

5.2 PARALLEL REDUNDANCY PROTOCOL

PRP (Parallel Reundancy Protocol) is defined in IEC 62439-3. PRP provides bumpless redundancy and meets the most demanding needs of substation automation. The PRP implementation of the REB is compatible with any standard PRP device.

PRP uses two independent Ethernet networks operating in parallel. PRP systems are designed so that there should be no common point of failure between the two networks, so the networks have independent power sources and are not connected together directly.

Devices designed for PRP applications have two ports attached to two separate networks and are called Doubly Attached Nodes (DAN). A DAN has two ports, one MAC address and one IP address.

The sending node replicates each frame and transmits them over both networks. The receiving node processes the frame that arrives first and discards the duplicate. Therefore there is no distinction between the working and backup path. The receiving node checks that all frames arrive in sequence and that frames are correctly received on both ports.

Devices such as printers that have a single Ethernet port can be connected to either of the networks but will not directly benefit from the PRP principles. Such devices are called Singly Attached Nodes (SAN). For devices with a single Ethernet port that need to connect to both LANs, this can be achieved by employing Ethernet Redundancy Boxes (sometimes abbreviated to RedBox). Devices with a single Ethernet port that connect to both LANs by means of a RedBox are known as Virtual DAN (VDAN).

The figure below summarises DAN, SAN, VDAN, LAN, and RedBox connectivity.

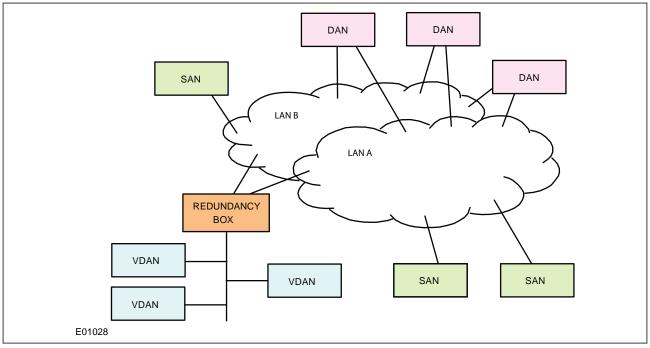


Figure 202: IED attached to separate LANs

In a DAN, both ports share the same MAC address so it does not affect the way devices talk to each other in an Ethernet network (Address Resolution Protocol at layer 2). Every data frame is seen by both ports.

When a DAN sends a frame of data, the frame is duplicated on both ports and therefore on both LAN segments. This provides a redundant path for the data frame if one of the segments fails. Under normal conditions, both LAN segments are working and each port receives identical frames.

MiCOM H382 DS Agile gateways H600 switch H600 switch

5.2.1 PRP APPLICATION IN THE SUBSTATION

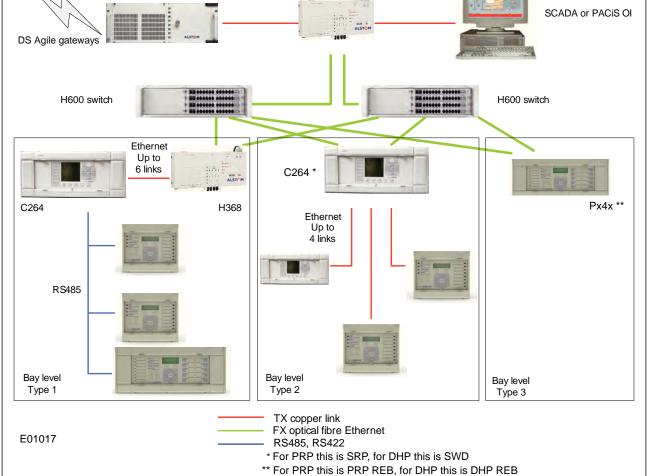


Figure 203: PRP application in the substation

5.3 HIGH-AVAILABILITY SEAMLESS REDUNDANCY (HSR)

HSR is standardized in IEC 62439-3 (clause 5) for use in ring topology networks. Similar to PRP, HSR provides bumpless redundancy and meets the most demanding needs of substation automation. HSR has become the reference standard for ring-topology networks in the substation environment. The HSR implementation of the redundancy Ethernet board (REB) is compatible with any standard HSR device.

HSR works on the premise that each device connected in the ring is a doubly attached node running HSR (referred to as DANH). Similar to PRP, singly attached nodes such as printers are connected via Ethernet Redundancy Boxes (RedBox).

5.3.1 HSR MULTICAST TOPOLOGY

When a DANH is sending a multicast frame, the frame (C frame) is duplicated (A frame and B frame), and each duplicate frame A/B is tagged with the destination MAC address and the sequence number. The frames A and B differ only in their sequence number, which is used to identify one frame from the other. Each frame is sent to the network via a separate port. The destination DANH receives two identical frames, removes the HSR tag of the first frame received and passes this (frame D) on for processing. The other duplicate frame is discarded. The nodes forward frames from one port to the other unless it was the node that injected it into the ring.

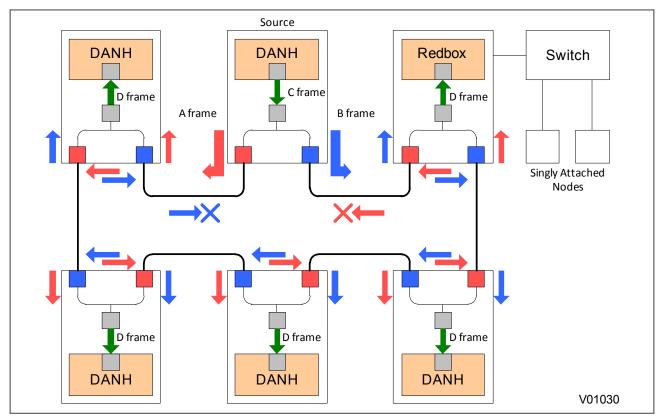


Figure 204: HSR multicast topology

Only about half of the network bandwidth is available in HSR for multicast or broadcast frames because both duplicate frames A & B circulate the full ring.

5.3.2 HSR UNICAST TOPOLOGY

With unicast frames, there is just one destination and the frames are sent to that destination alone. All non-recipient devices simply pass the frames on. They do not process them in any way. In other words, D frames are produced only for the receiving DANH. This is illustrated below.

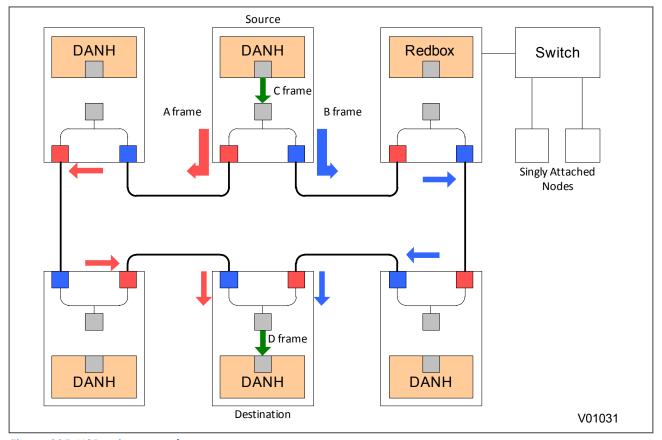


Figure 205: HSR unicast topology

For unicast frames, the whole bandwidth is available as both frames A & B stop at the destination node.

5.3.3 HSR APPLICATION IN THE SUBSTATION

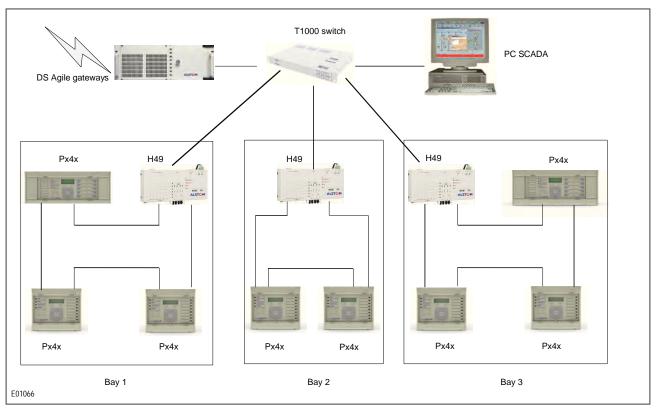


Figure 206: HSR application in the substation

5.4 RAPID SPANNING TREE PROTOCOL

RSTP is a standard used to quickly reconnect a network fault by finding an alternative path. It stops network loops whilst enabling redundancy. It can be used in star or ring connections as shown in the following figure.

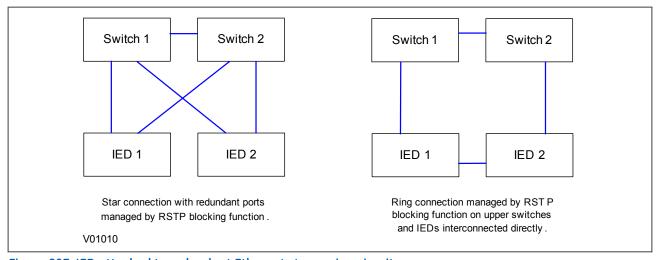


Figure 207: IED attached to redundant Ethernet star or ring circuit

The RSTP implementation in this product is compatible with any devices that use RSTP.

RSTP can recover network faults quickly, but the fault recovery time depends on the number of devices on the network and the network topology. A typical figure for the fault recovery time is 300ms. Therefore, RSTP cannot achieve the "bumpless" redundancy that some other protocols can.

Refer to IEEE 802.1D 2004 standard for detailed information about the opration of the protocol.

5.5 SELF HEALING PROTOCOL

The Self-Healing Protocol (SHP) implemented in the REB is a proprietary protocol that responds to the constraints of critical time applications such as the GOOSE messaging of IEC 61850.

It is designed, primarily, to be used on PACiS Substation Automation Systems that employ the C264-SWR212 and/or H35x switches.

SHP is applied to double-ring network topologies. If adjacent devices detect a break in the ring, then they re-route communication traffic to restore communication as outlined in the figure below.

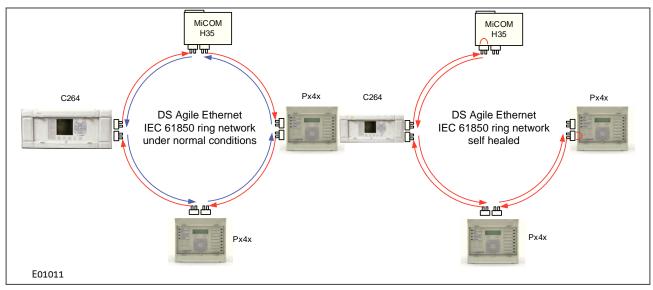


Figure 208: IED, bay computer and Ethernet switch with self healing ring facilities

A Self-Healing Management function (SHM) manages the ring.

Under healthy conditions, frames are sent on the main ring (primary fibre) in one direction, with short check frames being sent every 5 µs in the opposite direction on the back-up ring (secondary fibre).

If the main ring breaks, the SHMs at either side of the break start the network self-healing. On one side of the break, received messages are no longer sent to the main ring, but are sent to the back-up ring instead. On the other side of the break, messages received on the back-up ring are sent to the main ring and communications are re-established. This takes place in less than 1 ms and can be described as "bumpless".

The principle of SHP is outlined in the figures below.

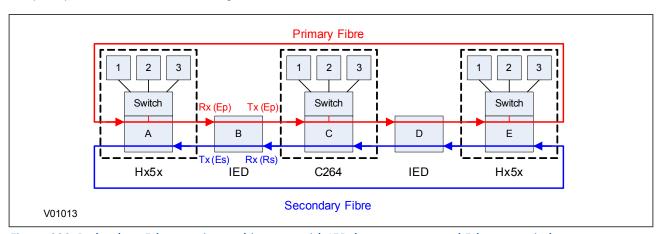


Figure 209: Redundant Ethernet ring architecture with IED, bay computer and Ethernet switches

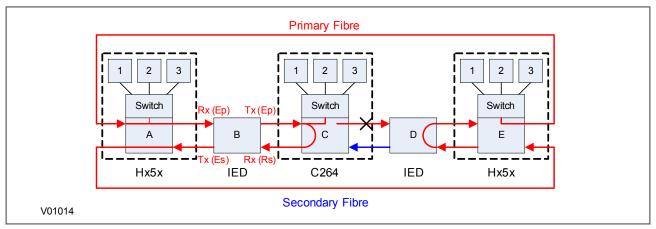


Figure 210: Redundant Ethernet ring architecture with IED, bay computer and Ethernet switches after failure

5.6 DUAL HOMING PROTOCOL

The Dual Homing Protocol (DHP) implemented in the REB is a proprietary protocol. It is designed, primarily to be used on PACiS systems that employ the C264-SWD212 and/or H36x multimode switches.

DHP addresses the constraints of critical time applications such as the GOOSE messaging of IEC 61850.

DHP is applied to double-star network topologies. If a connection between two devices is broken, the network continues to operate correctly.

The Dual Homing Manager (DHM) handles topologies where a device is connected to two independent networks, one being the "main" path, the other being the "backup" path. Both are active at the same time.

Internet frames from a sending device are sent by the DHM to both networks. Receiving devices apply a "duplicate discard" principle. This means that when both networks are operational, the REB receives two copies of the same Ethernet frame. If both links are healthy, frames are received on both, and the DHM uses the first frame received. The second frame is discarded. If one link fails, frames received on the healthy link are used.

DHP delivers a typical recovery time of less than 1 ms. The mechanism is outlined in the figures below.

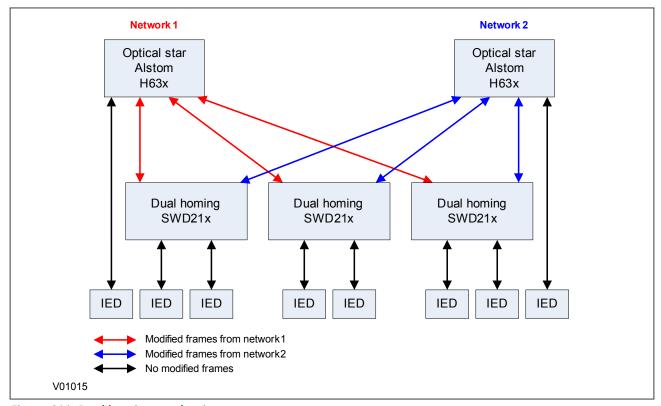


Figure 211: Dual homing mechanism

The H36x is a repeater with a standard 802.3 Ethernet switch, plus the DHM.

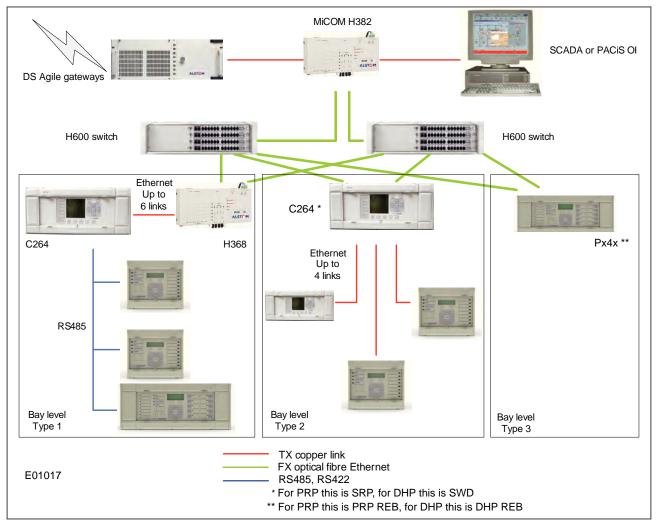


Figure 212: Application of Dual Homing Star at substation level

5.7 CONFIGURING IP ADDRESSES

An IP address is a logical address assigned to devices in a computer network that uses the Internet Protocol (IP) for communication between nodes. IP addresses are stored as binary numbers but they are represented using Decimal Dot Notation, where four sets of decimal numbers are separated by dots as follows:

XXX.XXX.XXX

For example:

10.86.254.85

An IP address in a network is usually associated with a subnet mask. The subnet mask defines which network the device belongs to. A subnet mask has the same form as an IP address.

For example:

255.255.255.0

Both the IED and the REB each have their own IP address. The following diagram shows the IED as IP1 and the REB as IP2.

Note:

IP1 and IP2 are different but use the same subnet mask.

The switch IP address must be configured through the Ethernet network.

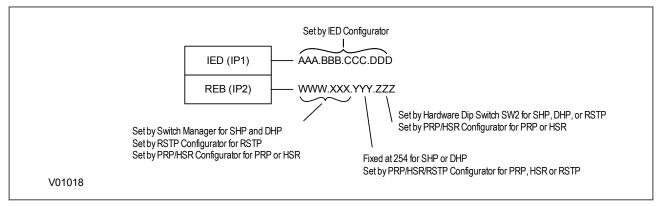


Figure 213: IED and REB IP address configuration

5.7.1 CONFIGURING THE IED IP ADDRESS

If you are using IEC 61850, set the IED IP address using the IEC 61850 Configurator software. In the IEC 61850 Configurator, set **Media** to **Single Copper or Redundant Fibre**.

If you are using DNP3 over Ethernet, set the IED IP address by editing the DNP3 file, using the DNP3 Configurator software. In the DNP3 Configurator, set **Ethernet Media** to **Copper**, even though the redundant Ethernet network uses fibre optic cables.

5.7.2 CONFIGURING THE REB IP ADDRESS

The board IP address must be configured before connecting the IED to the network to avoid an IP address conflict. The way you configure the IP address depends on the redundancy protocol you have chosen.

PRP/HSR

If using PRP or HSR, you configure the REB IP address using the PRP/HSR Configurator software.

RSTP

If using RSTP, you configure the REB IP address using the PRP/HSR Configurator software.

SHP or DHP

If using SHP or DHP the first two octets are set by the Switch Manager software or an SNMP MIB browser. The third octet is fixed at 254 (FE hex, 11111110 binary), and the fourth octet is set by the on-board dip switch.

Note:

An H35 (SHP) or H36 (DHP) network device is needed in the network to configure the REB IP address if you are using SNMP.

5.7.2.1 CONFIGURING THE LAST OCTET (SHP, DHP, RSTP)

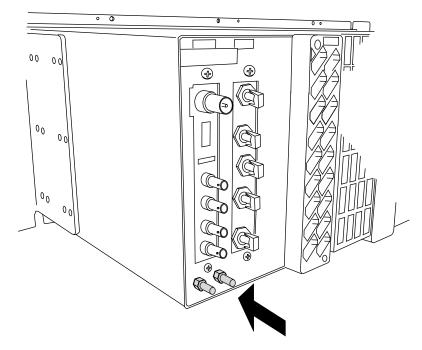
If using SHP or DHP, the last octet is configured using board address switch SW2 on the board. Remove the IED front cover to gain access to the board address switch.

Warning:

Configure the hardware settings before the device is installed.

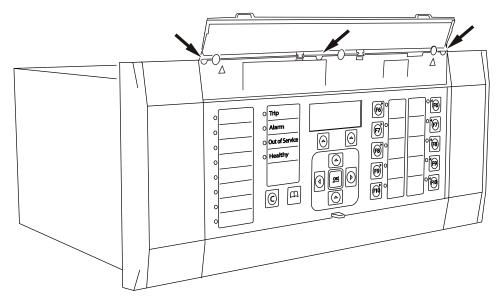
- 1. Refer to the safety section of the IED.
- 2. Switch off the IED. Disconnect the power and all connections.

- 3. Before removing the front cover, take precautions to prevent electrostatic discharge damage according to the ANSI/ESD-20.20 -2007 standard.
- 4. Wear a 1 $M\Omega$ earth strap and connect it to the earth (ground) point on the back of the IED.



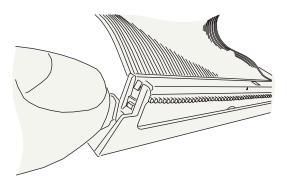
E01019

5. Lift the upper and lower flaps. Remove the six screws securing the front panel and pull the front panel outwards.



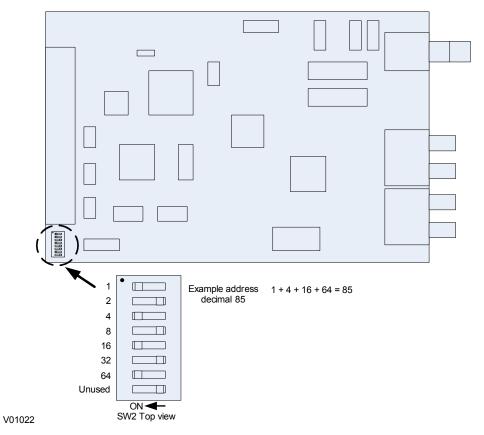
E01020

6. Press the levers either side of the connector to disconnect the ribbon cable from the front panel.



E01021

7. Remove the redundant Ethernet board. Set the last octet of IP address using the DIP switches. The available range is 1 to 127.



8. Once you have set the IP address, reassemble the IED, following theses instructions in the reverse order.

Warning:

Take care not to damage the pins of the ribbon cable connector on the front panel when reinserting the ribbon cable.

6 SIMPLE NETWORK MANAGEMENT PROTOCOL (SNMP)

Simple Network Management Protocol (SNMP) is a network protocol designed to manage devices in an IP network. The MiCOM P40 Modular products can provide up to two SNMP interfaces on Ethernet models; one to the IED's Main Processor for device level status information, and another directly to the redundant Ethernet board (where applicable) for specific Ethernet network level information.

Two versions of SNMP are supported: Version 2c, and a secure implementation of version 3 that includes cybersecurity. Only the Main Processor SNMP interface supports Version 3.

6.1 SNMP MANAGEMENT INFORMATION BASES

SNMP uses a Management Information Base (MIB), which contains information about parameters to supervise. The MIB format is a tree structure, with each node in the tree identified by a numerical Object Identifier (OID). Each OID identifies a variable that can be read using SNMP with the appropriate software. The information in the MIB is standardized.

Each device in a network (workstation, server, router, bridge, etc.) maintains a MIB that reflects the status of the managed resources on that system, such as the version of the software running on the device, the IP address assigned to a port or interface, the amount of free hard drive space, or the number of open files. The MIB does not contain static data, but is instead an object-oriented, dynamic database that provides a logical collection of managed object definitions. The MIB defines the data type of each managed object and describes the object.

6.2 MAIN PROCESSOR MIBS STRUCTURE

The Main Processor MIB uses a private OID with a specific Alstom Grid number assigned by the IANA. Some items in this MIB also support SNMP traps (where indicated). These are items that can automatically notify a host without being read.

					P	Addre	ss				Name	Trigger Trap?
0											ROOT NODE	
	1										ISO	
		3									Org	
			6								DOD	
				1							Internet	
					4						Private	
						1					Enterprise	
							43534				Alstom Grid (IANA No)	
								1			Px4x	
									1		System Data	
										1	Description	YES
										2	Plant Reference	YES
										3	Model Number	NO
										4	Serial Number	NO
										5	Frequency	NO
										6	Plant Status	YES
										7	Active Group	YES
										8	Software Ref.1	NO
										9	Software Ref.2	NO
										10	Access Level (UI)	YES
									2		Date and Time	

	Address			Name	Trigger Trap?
			1	Date Time	NO
			2	IRIG-B Status	YES
			3	Battery Status	YES
			4	Active Sync source	YES
			5	SNTP Server 1	NO
			6	SNTP Server 2	NO
			7	SNTP Status	YES
			8	PTP Status	YES
		3		System Alarms	
			1	Invalid Message Format	YES
			2	Main Protection Fail	YES
			3	Comms Changed	YES
			4	Max Prop. Alarm	YES
			5	9-2 Sample Alarm	YES
			6	9-2LE Cfg Alarm	YES
			7	Battery Fail	YES
			8	Rear Communication Fail	YES
			9	GOOSE IED Missing	YES
			10	Intermicom loopback	YES
			11	Intermicom message fail	YES
			12	Intermicom data CD fail	YES
			13	Intermicom Channel fail	YES
			14	Backup setting fail	YES
			15	User Curve commit to flash failure	YES
			16	SNTP time Sync fail	YES
			17	PTP failure alarm	YES
		4		Device Mode	
			1	IED Mod/Beh	YES
			2	Simulation Mode of Subscription	YES

6.3 REDUNDANT ETHERNET BOARD MIB STRUCTURE

The Redundant Ethernet board MIB uses three types of OID:

- sysDescr
- sysUpTime
- sysName

MIB structure for RSTP, DHP and SHP

		Name							
0									CCITT
	1								ISO
		3							Org
			6						DOD
				1					Internet

			Address	3						Name
			2							mgmt
				1						Mib-2
					1					sys
						1				sysDescr
						3				sysUpTime
						4				sysName
Remote	Monitoring	 ·								
					16					RMON
						1				statistics
							1			etherstat
								1		etherStatsEntry
									9	etherStatsUndersizePkts
									10	etherStatsOversizePkts
									12	etherStatsJabbers
									13	etherStatsCollisions
									14	etherStatsPkts64Octets
									15	etherStatsPkts65to127Octets
									16	etherStatsPkts128to255Octets
									17	etherStatsPkts256to511Octets
									18	etherStatsPkts512to1023Octets

MIB structure for PRP/HSR

					A	ddress	S					Name
0												ITU
	1											ISO
		0										Standard
			62439									IECHighavailibility
				3								PRP
					1							linkRedundancyEntityObjects
						0						IreConfiguration
							0					IreConfigurationGeneralGroup
								1				IreManufacturerName
								2				IreInterfaceCount
							1					IreConfigurationInterfaceGroup
								0				IreConfigurationInterfaces
									1			IreInterfaceConfigTable
										1		IreInterfaceConfigEntry
											1	IreInterfaceConfigIndex
											2	IreRowStatus
											3	IreNodeType
											4	IreNodeName
											5	IreVersionName
											6	IreMacAddressA

			Ad	ldress						Name
									7	IreMacAddressB
									8	 IreAdapterAdminStateA
									9	 IreAdapterAdminStateB
									10	
									11	 IreLinkStatusB
									12	 IreDuplicateDiscard
									13	 IreTransparentReception
									14	IreHsrLREMode
									15	lreSwitchingEndNode
									16	IreRedBoxIdentity
									17	IreSanA
									18	IreSanB
									19	 IreEvaluateSupervision
									20	 IreNodesTableClear
									21	 IreProxyNodeTableClear
				1						IreStatistics
					1					 IreStatisticsInterfaceGroup
						0				IreStatisticsInterfaces
							1			
									1	IreInterfaceStatsIndex
									2	IreCntTotalSentA
									3	IreCntTotalSentB
									4	IreCntErrWrongLANA
									5	IreCntErrWrongLANB
									6	IreCntReceivedA
									7	IreCntReceivedB
									8	IreCntErrorsA
									9	IreCntErrorsB
									10	IreCntNodes
									11	IreOwnRxCntA
									12	IreOwnRxCntB
							3			IreProxyNodeTable
								1		IreProxyNodeEntry
									1	reProxyNodeIndex
									2	reProxyNodeMacAddress
3										Org
	6									Dod
		1								Internet
			2							mgmt
				1						mib-2
					1					System
						1				sysDescr
						3				sysUpTime

5 sysName sysServices 2 interfaces 2 interfaces 2 iffable 1 ifEntry 1 ifIndex 2 ifOperation 3 ifType 4 ifMtu 5 ifSpeed 6 ifPhysAddress 7 ifAdminStatus 8 ifOpenStatus 9 ifLastChange 10 ifInOctets 11 ifInUcastPkts 12 ifInNUcastPkts 13 ifInDiscards 14 ifInErrors 15 ifInUknownProtos 16 ifOutOctets 17 ifOutUcastPkts 18 ifOutIocastPkts 18 ifOutIocastPkts 19 ifOutIocastPkts 19 ifOutIocastPkts 19 ifOutIocastPkts 17 ifOutUcastPkts 18 ifOutIocastPkts 18 ifOutIocastPkts 19 ifOu	
7 sysServices	
2 interfaces	
2 ifTable 1 ifEntry 1 ifIndex 2 ifDescr 3 ifType 3 ifType 4 ifMtu ifSpeed 6 ifPhysAddress 7 ifAdminStatus 8 ifOpenStatus 9 ifLastChange 10 ifInOctets 11 ifInUcastPkts 12 ifInNUcastPkts 13 ifInDiscards 14 ifInErrors 15 ifInUnknownProtos 16 ifOutOctets 17 ifOutUcastPkts 18 ifOutNucastPkts 18 ifOutNucastPkts 18 ifOutNucastPkts 19 ifOutDiscards 19 ifOutDiscards 19 ifOutDiscards 19 ifOutDiscards 19 ifOutDiscards 19 ifOutDiscards 19 ifOutDiscards 19 ifOutDiscards 19 ifOutDiscards 19 ifOutDiscards 19 ifOutDiscards 19 ifOutDiscards 19 ifOutDiscards 19 ifOutDiscards 19 ifOutDiscards 19 ifOutDiscards 10 ifOutDiscards	
1 ifEntry 1 ifIndex 2 ifDescr 3 ifType 4 ifMtu 5 ifSpeed 6 ifPhysAddress 7 ifAdminStatus 8 ifOpenStatus 9 ifLastChange 10 ifInOctets 11 ifInUcastPkts 12 ifInNUcastPkts 13 ifInDiscards 14 ifInErrors 15 ifInUnknownProtos 16 ifOutOctets 17 ifOutUcastPkts 18 ifOutNUcastPkts 19 ifOutDiscards 10 ifOutDiscards 11 ifInUcastPkts 12 ifOutDiscards 13 ifOutDiscards 14 ifInUcastPkts 15 ifOutDiscards 16 ifOutDiscards 17 ifOutDiscards 18 ifOutDiscards 19 ifOutDiscards 10 ifOutDiscards 11 ifInUcastPkts 12 ifOutDiscards 13 ifOutDiscards 14 ifInUcastPkts 15 ifOutDiscards 16 ifOutDiscards 17 ifOutDiscards 18 ifOutDiscards 18	
1 ifIndex 2 ifDescr 3 ifType 4 ifMtu 5 ifSpeed 6 ifPhysAddress 7 ifAdminStatus 8 ifOpenStatus 9 ifLastChange 10 ifInOctets 11 ifInUcastPkts 12 ifInNUcastPkts 13 ifInDiscards 14 ifInErrors 15 ifInUnknownProtos 16 ifOutOctets 17 ifOutUcastPkts 18 ifOutNUcastPkts 19 ifOutDiscards	
2 ifDescr 3 ifType 4 ifMtu 5 ifSpeed 6 ifPhysAddress 7 ifAdminStatus 8 ifOpenStatus 9 ifLastChange 10 ifInOctets 11 ifInUcastPkts 12 ifInNUcastPkts 13 ifInDiscards 14 ifInErrors 15 ifInUknownProtos 16 ifOutOctets 17 ifOutUcastPkts 18 ifOutNUcastPkts 19 ifOutDiscards 10 ifOutDiscards 11 ifOutDiscards 12 ifOutDiscards 13 ifOutDiscards 14 ifInErrors 15 ifOutDiscards 16 ifOutDiscards 17 ifOutDiscards 18 ifOutDiscards 19 ifOutDiscards 10 ifOutDiscards 11 ifOutDiscards 12 ifOutDiscards 13 ifOutDiscards 14 ifOutDiscards 15 ifOutDiscards 16 ifOutDiscards 17 ifOutDiscards 18 ifOutDiscards 19 ifOutDiscards 10 ifOutDiscards 11 ifOutDiscards 12 ifOutDiscards 13 ifOutDiscards 14 ifOutDiscards 15 ifOutDiscards 16 ifOutDiscards 17 ifOutDiscards 18 ifOutDiscar	
3 ifType	
4	
5 ifSpeed 6 ifPhysAddress 7 ifAdminStatus 8 ifOpenStatus 9 ifLastChange 10 ifInOctets 11 ifInUcastPkts 12 ifInNUcastPkts 13 ifInErrors 14 ifInErrors 15 ifInUnknownProtos 16 ifOutOctets 17 ifOutUcastPkts 18 ifOutNUcastPkts 19 ifOutDiscards	
6	
7	
8 ifOpenStatus 9 ifLastChange 10 iflnOctets 11 iflnUcastPkts 12 iflnNUcastPkts 13 iflnErrors 14 iflnErrors 15 iflnUnknownProtos 16 ifOutOctets 17 ifOutUcastPkts 18 ifOutNUcastPkts 19 ifOutDiscards	
9 ifLastChange 10 ifInOctets 11 ifInUcastPkts 12 ifInNUcastPkts 13 ifInDiscards 14 ifInErrors 15 ifInUnknownProtos 16 ifOutOctets 17 ifOutUcastPkts 18 ifOutNUcastPkts	
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11 iflnUcastPkts 12 iflnNUcastPkts 13 iflnDiscards 14 iflnErrors 15 iflnUnknownProtos 16 ifOutOctets 17 ifOutUcastPkts 18 ifOutNUcastPkts 19 ifOutDiscards 19 ifOutDiscards 19 ifOutDiscards 19 ifOutDiscards 19 ifOutDiscards 10	
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15 iflnUnknownProtos 16 ifOutOctets 17 ifOutUcastPkts 18 ifOutNUcastPkts 19 ifOutDiscards 15 ifOutDiscards 15 ifOutDiscards 15 ifOutDiscards 16 ifOutDiscards 17 ifOutDiscards 17 ifOutDiscards 17 ifOutDiscards 17 ifOutDiscards 18 ifOutDiscards 18 ifOutDiscards 18 ifOutDiscards 19 ifOutDiscards 19 ifOutDiscards 18 ifOutDiscards 19 ifOutDiscards 18 ifOutDiscards 18	
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17 ifOutUcastPkts 18 ifOutNUcastPkts 19 ifOutDiscards	
18 ifOutNUcastPkts 19 ifOutDiscards	
19 ifOutDiscards	
20 ifOutErrors	
21 ifOutQLen	
22 ifSpecific	
16 rmon	
1 statistics	
1 etherStatsTable	
1 etherStatsEntry	
1 etherStatsIndex	
2 etherStatsDataSource	
3 etherStatsDropEvents	
4 etherStatsOctets	
5 etherStatsPkts	
6 etherStatsBroadcastPkts	
7 etherStatsMulticastPkts	
8 etherStatsCRCAlignErrors	
9 etherStatsUndersizePkts	
10 etherStatsOversizePkts	
11 etherStatsFragments	
12 etherStatsJabbers	

Address									Name	
									13	etherStatsCollisions
									14	etherStatsPkts64Octets
									15	etherStatsPkts65to127Octets
									16	etherStatsPkts128to255Octets
									17	etherStatsPkts256to511Octets
									18	etherStatsPkts512to1023Octets
									19	etherStatsPkts1024to1518Octets
									20	etherStatsOwner
									21	etherStatsStatus

6.4 ACCESSING THE MIB

Various SNMP client software tools can be used. We recommend using an SNMP MIB browser, which can perform the basic SNMP operations such as GET, GETNEXT and RESPONSE.

Note:

There are two IP addresses visible when communicating with the Redundant Ethernet Card via the fibre optic ports: Use the one for the IED itself to the Main Processor SNMP interface, and use the one for the on-board Ethernet switch to access the Redundant Ethernet Board SNMP interface. See the configuration chapter for more information.

6.5 MAIN PROCESSOR SNMP CONFIGURATION

You configure the main processor SNMP interface using the HMI panel. Two different versions are available; SNMPv2c and SNMPv3:

To enable the main processor SNMP interface:

- 1. Select the COMMUNICATIONS column and scroll to the SNMP PARAMETERS heading
- 2. You can select either v2C, V3 or both. Selecting None will disable the main processor SNMP interface.

SNMP Trap Configuration

SNMP traps allow for unsolicited reporting between the IED and up to two SNMP managers with unique IP addresses. The device MIB details what information can be reported using Traps. To configure the SNMP Traps:

- 1. Move down to the cell *Trap Dest. IP 1* and enter the IP address of the first destination SNMP manager. Setting this cell to 0.0.0.0 disables the first Trap interface.
- 2. Move down to the cell *Trap Dest. IP 2* and enter the IP address of the second destination SNMP manager. Setting this cell to 0.0.0.0 disables the Second Trap interface.

SNMP V3 Security Configuration

SNMPv3 provides a higher level of security via authentication and privacy protocols. The IED adopts a secure SNMPv3 implementation with a user-based security model (USM).

Authentication is used to check the identity of users, privacy allows for encryption of SNMP messages. Both are optional, however you must enable authentication in order to enable privacy. To configure these security options:

- 1. If SNMPv3 has been enabled, set the **Security Level** setting. There are three levels; without authentication and without privacy (noAuthNoPriv), with authentication but without privacy (authNoPriv), and with authentication and with privacy (authPriv).
- 2. If Authentication is enabled, use the *Auth Protocol* setting to select the authentication type. There are two options: HMAC-MD5-96 or HMAC-SHA-96.
- 3. Using the **Auth Password** setting, enter the 8-character password to be used by the IED for authentication.
- 4. If privacy is enabled, use the *Encrypt Protocol* setting to set the 8-character password that will be used by the IED for encryption.

SNMP V2C Security Configuration

SNMPv2c implements authentication between the master and agent using a parameter called the *Community Name*. This is effectively the password but it is not encrypted during transmission (this makes it inappropriate for some scenarios in which case version 3 should be used instead). To configure the SNMP 2c security:

1. If SNMPv2c has been enabled, use the **Community Name** setting to set the password that will be used by the IED and SNMP manager for authentication. This may be between one and 8 characters.

7 DATA PROTOCOLS

The products supports a wide range of protocols to make them applicable to many industries and applications. The exact data protocols supported by a particular product depend on its chosen application, but the following table gives a list of the data protocols that are typically available.

SCADA data protocols

Data Protocol	Layer 1 protocol	Description
Courier	K-Bus, RS232, RS485, Ethernet	Standard for SCADA communications developed by General Electric.
MODBUS	RS485	Standard for SCADA communications developed by Modicon.
IEC 60870-5-103	RS485	IEC standard for SCADA communications
DNP 3.0	RS485, Ethernet	Standard for SCADA communications developed by Harris. Used mainly in North America.
IEC 61850	Ethernet	IEC standard for substation automation. Facilitates interoperability.

The relationship of these protocols to the lower level physical layer protocols are as follows:

	IEC 60870-5-103						
Data Protocols	MODBUS	IEC 61850					
Data Protocois	DNP3.0	DNP3.0					
	Courier	Courier	Courier	Courier			
Data Link Layer	EIA(RS)485	Ethernet	EIA(RS)232	K-Bus			
Physical Layer	Copper or Optical Fibre						

7.1 COURIER

This section should provide sufficient detail to enable understanding of the Courier protocol at a level required by most users. For situations where the level of information contained in this manual is insufficient, further publications (R6511 and R6512) containing in-depth details about the protocol and its use, are available on request.

Courier is an General Electric proprietary communication protocol. Courier uses a standard set of commands to access a database of settings and data in the IED. This allows a master to communicate with a number of slave devices. The application-specific elements are contained in the database rather than in the commands used to interrogate it, meaning that the master station does not need to be preconfigured. Courier also provides a sequence of event (SOE) and disturbance record extraction mechanism.

7.1.1 PHYSICAL CONNECTION AND LINK LAYER

Courier can be used with three physical layer protocols: K-Bus, EIA(RS)232 or EIA(RS)485.

Several connection options are available for Courier

- The front serial RS232 port (for connection to Settings application software on, for example, a laptop
- Rear Port 1 (RP1) for permanent SCADA connection via RS485 or K-Bus
- Optional fibre port (RP1 in slot A) for permanent SCADA connection via optical fibre
- Optional Rear Port 2 (RP2) for permanent SCADA connection via RS485, K-Bus, or RS232

For either of the rear ports, both the IED address and baud rate can be selected using the front panel menu or by the settings application software.

7.1.2 COURIER DATABASE

The Courier database is two-dimensional and resembles a table. Each cell in the database is referenced by a row and column address. Both the column and the row can take a range from 0 to 255 (0000 to FFFF Hexadecimal. Addresses in the database are specified as hexadecimal values, for example, 0A02 is column 0A row 02. Associated settings or data are part of the same column. Row zero of the column has a text string to identify the contents of the column and to act as a column heading.

The product-specific menu databases contain the complete database definition.

7.1.3 SETTINGS CATEGORIES

There are two main categories of settings in protection IEDs:

- Control and support settings
- Protection settings

With the exception of the Disturbance Recorder settings, changes made to the control and support settings are implemented immediately and stored in non-volatile memory. Changes made to the Protection settings and the Disturbance Recorder settings are stored in 'scratchpad' memory and are not immediately implemented. These need to be committed by writing to the *Save Changes* cell in the *CONFIGURATION* column.

7.1.4 SETTING CHANGES

Courier provides two mechanisms for making setting changes. Either method can be used for editing any of the settings in the database.

Method 1

This uses a combination of three commands to perform a settings change:

First, enter Setting mode: This checks that the cell is settable and returns the limits.

- 1. Preload Setting: This places a new value into the cell. This value is echoed to ensure that setting corruption has not taken place. The validity of the setting is not checked by this action.
- 2. Execute Setting: This confirms the setting change. If the change is valid, a positive response is returned. If the setting change fails, an error response is returned.
- 3. Abort Setting: This command can be used to abandon the setting change.

This is the most secure method. It is ideally suited to on-line editors because the setting limits are extracted before the setting change is made. However, this method can be slow if many settings are being changed because three commands are required for each change.

Method 2

The Set Value command can be used to change a setting directly. The response to this command is either a positive confirm or an error code to indicate the nature of a failure. This command can be used to implement a setting more rapidly than the previous method, however the limits are not extracted. This method is therefore most suitable for off-line setting editors such as MiCOM S1 Agile, or for issuing preconfigured control commands.

7.1.5 EVENT EXTRACTION

You can extract events either automatically (rear serial port only) or manually (either serial port). For automatic extraction, all events are extracted in sequential order using the Courier event mechanism. This includes fault and maintenance data if appropriate. The manual approach allows you to select events, faults, or maintenance data as desired.

7.1.5.1 AUTOMATIC EVENT RECORD EXTRACTION

This method is intended for continuous extraction of event and fault information as it is produced. It is only supported through the rear Courier port.

When new event information is created, the *Event* bit is set in the *Status* byte. This indicates to the Master device that event information is available. The oldest, non-extracted event can be extracted from the IED using the *Send Event* command. The IED responds with the event data.

Once an event has been extracted, the *Accept Event* command can be used to confirm that the event has been successfully extracted. When all events have been extracted, the *Event* bit is reset. If there are more events still to be extracted, the next event can be accessed using the *Send Event* command as before.

7.1.5.2 MANUAL EVENT RECORD EXTRACTION

The VIEW RECORDS column (location 01) is used for manual viewing of event, fault, and maintenance records. The contents of this column depend on the nature of the record selected. You can select events by event number and directly select a fault or maintenance record by number.

Event Record Selection ('Select Event' cell: 0101)

This cell can be set the number of stored events. For simple event records (Type 0), cells 0102 to 0105 contain the event details. A single cell is used to represent each of the event fields. If the event selected is a fault or maintenance record (Type 3), the remainder of the column contains the additional information.

Fault Record Selection ('Select Fault' cell: 0105)

This cell can be used to select a fault record directly, using a value between 0 and 4 to select one of up to five stored fault records. (0 is the most recent fault and 4 is the oldest). The column then contains the details of the fault record selected.

Maintenance Record Selection ('Select Maint' cell: 01F0)

This cell can be used to select a maintenance record using a value between 0 and 4. This cell operates in a similar way to the fault record selection.

If this column is used to extract event information, the number associated with a particular record changes when a new event or fault occurs.

Event Types

The IED generates events under certain circumstances such as:

- Change of state of output contact
- Change of state of opto-input
- Protection element operation
- Alarm condition
- Setting change
- Password entered/timed-out

Event Record Format

The IED returns the following fields when the Send Event command is invoked:

- Cell reference
- Time stamp
- Cell text
- Cell value

The Menu Database contains tables of possible events, and shows how the contents of the above fields are interpreted. Fault and Maintenance records return a Courier Type 3 event, which contains the above fields plus two additional fields:

- Event extraction column
- Event number

These events contain additional information, which is extracted from the IED using column B4. Row 01 contains a **Select Record** setting that allows the fault or maintenance record to be selected. This setting should be set to the event number value returned in the record. The extended data can be extracted from the IED by uploading the text and data from the column.

7.1.6 DISTURBANCE RECORD EXTRACTION

The stored disturbance records are accessible through the Courier interface. The records are extracted using column (B4).

The **Select Record** cell can be used to select the record to be extracted. Record 0 is the oldest non-extracted record. Older records which have been already been extracted are assigned positive values, while younger records are assigned negative values. To help automatic extraction through the rear port, the IED sets the **Disturbance** bit of the **Status** byte, whenever there are non-extracted disturbance records.

Once a record has been selected, using the above cell, the time and date of the record can be read from the *Trigger Time* cell (B402). The disturbance record can be extracted using the block transfer mechanism from cell B40B and saved in the COMTRADE format. The settings application software software automatically does this.

7.1.7 PROGRAMMABLE SCHEME LOGIC SETTINGS

The programmable scheme logic (PSL) settings can be uploaded from and downloaded to the IED using the block transfer mechanism.

The following cells are used to perform the extraction:

- **Domain** cell (B204): Used to select either PSL settings (upload or download) or PSL configuration data (upload only)
- Sub-Domain cell (B208): Used to select the Protection Setting Group to be uploaded or downloaded.
- Version cell (B20C): Used on a download to check the compatibility of the file to be downloaded.
- Transfer Mode cell (B21C): Used to set up the transfer process.
- Data Transfer cell (B120): Used to perform upload or download.

The PSL settings can be uploaded and downloaded to and from the IED using this mechanism. The settings application software must be used to edit the settings. It also performs checks on the validity of the settings before they are transferred to the IED.

7.1.8 TIME SYNCHRONISATION

The time and date can be set using the time synchronization feature of the Courier protocol. The device will correct for the transmission delay. The time synchronization message may be sent as either a global command or to any individual IED address. If the time synchronization message is sent to an individual address, then the device will respond with a confirm message. If sent as a global command, the (same) command must be sent twice. A time synchronization Courier event will be generated/produced whether the time-synchronization message is sent as a global command or to any individual IED address.

If the clock is being synchronized using the IRIG-B input then it will not be possible to set the device time using the Courier interface. An attempt to set the time using the interface will cause the device to create an event with the current date and time taken from the IRIG-B synchronized internal clock.

7.1.9 COURIER CONFIGURATION

To configure the device:

- 1. Select the CONFIGURATION column and check that the Comms settings cell is set to Visible.
- 2. Select the COMMUNICATIONS column.
- 3. Move to the first cell down (*RP1 protocol*). This is a non-settable cell, which shows the chosen communication protocol in this case *Courier*.

COMMUNICATIONS RP1 Protocol Courier

4. Move down to the next cell (*RP1 Address*). This cell controls the address of the RP1 port on thje device. Up to 32 IEDs can be connected to one spur. It is therefore necessary for each IED to have a unique address so that messages from the master control station are accepted by one IED only. Courier uses an integer number between 1 and 254 for the Relay Address. It is set to 255 by default, which has to be changed. It is important that no two IEDs share the same address.

COMMUNICATIONS RP1 Address 100

5. Move down to the next cell (*RP1 InactivTimer*). This cell controls the inactivity timer. The inactivity timer controls how long the IED waits without receiving any messages on the rear port before revoking any password access that was enabled and discarding any changes. For the rear port this can be set between 1 and 30 minutes.

COMMUNICATIONS RP1 Inactivtimer 10.00 mins.

6. If the optional fibre optic connectors are fitted, the *RP1 PhysicalLink* cell is visible. This cell controls the physical media used for the communication (Copper or Fibre optic).

COMMUNICATIONS RP1 PhysicalLink Copper

7. Move down to the next cell (*RP1 Card Status*). This cell is not settable. It displays the status of the chosen physical layer protocol for RP1.

COMMUNICATIONS RP1 Card Status K-Bus OK

8. Move down to the next cell (*RP1 Port Config*). This cell controls the type of serial connection. Select between K-Bus or RS485

COMMUNICATIONS RP1 Port Config K-Bus

9. If using EIA(RS)485, the next cell (*RP1 Comms Mode*) selects the communication mode. The choice is either IEC 60870 FT1.2 for normal operation with 11-bit modems, or 10-bit no parity. If using K-Bus this cell will not appear.

COMMUNICATIONS
RP1 Comms Mode
IEC 60870 FT1.2

10. If using EIA(RS)485, the next cell down controls the baud rate. Three baud rates are supported; 9600, 19200 and 38400. If using K-Bus this cell will not appear as the baud rate is fixed at 64 kbps.

COMMUNICATIONS RP1 Baud rate 19200

7.2 IEC 60870-5-103

The specification IEC 60870-5-103 (Telecontrol Equipment and Systems Part 5 Section 103: Transmission Protocols), defines the use of standards IEC 60870-5-1 to IEC 60870-5-5, which were designed for communication with protection equipment

This section describes how the IEC 60870-5-103 standard is applied to the Px40 platform. It is not a description of the standard itself. The level at which this section is written assumes that the reader is already familiar with the IEC 60870-5-103 standard

This section should provide sufficient detail to enable understanding of the standard at a level required by most users.

The IEC 60870-5-103 interface is a master/slave interface with the device as the slave device. The device conforms to compatibility level 2, as defined in the IEC 60870-5-103.standard.

The following IEC 60870-5-103 facilities are supported by this interface:

- Initialization (reset)
- Time synchronization
- Event record extraction
- General interrogation
- Cyclic measurements
- General commands
- Disturbance record extraction
- Private codes

7.2.1 PHYSICAL CONNECTION AND LINK LAYER

Two connection options are available for IEC 60870-5-103:

- Rear Port 1 (RP1) for permanent SCADA connection via RS485
- Optional fibre port (RP1 in slot A) for permanent SCADA connection via optical fibre

If the optional fibre optic port is fitted, a menu item appears in which the active port can be selected. However the selection is only effective following the next power up.

The IED address and baud rate can be selected using the front panel menu or by the settings application software.

7.2.2 INITIALISATION

Whenever the device has been powered up, or if the communication parameters have been changed a reset command is required to initialize the communications. The device will respond to either of the two reset commands; Reset CU or Reset FCB (Communication Unit or Frame Count Bit). The difference between the two commands is that the Reset CU command will clear any unsent messages in the transmit buffer, whereas the Reset FCB command does not delete any messages.

The device will respond to the reset command with an identification message ASDU 5. The Cause of Transmission (COT) of this response will be either Reset CU or Reset FCB depending on the nature of the reset command. The content of ASDU 5 is described in the IEC 60870-5-103 section of the Menu Database, available from General Electric separately if required.

In addition to the above identification message, it will also produce a power up event.

7.2.3 TIME SYNCHRONISATION

The time and date can be set using the time synchronization feature of the IEC 60870-5-103 protocol. The device will correct for the transmission delay as specified in IEC 60870-5-103. If the time synchronization message is sent as a send/confirm message then the device will respond with a confirm message. A time synchronization Class 1 event will be generated/produced whether the time-synchronization message is sent as a send confirm or a broadcast (send/no reply) message.

If the clock is being synchronized using the IRIG-B input then it will not be possible to set the device time using the IEC 60870-5-103 interface. An attempt to set the time via the interface will cause the device to create an event with the current date and time taken from the IRIG-B synchronized internal clock.

7.2.4 SPONTANEOUS EVENTS

Events are categorized using the following information:

- Function type
- Information Number

The IEC 60870-5-103 profile in the Menu Database contains a complete listing of all events produced by the device.

7.2.5 GENERAL INTERROGATION (GI)

The GI request can be used to read the status of the device, the function numbers, and information numbers that will be returned during the GI cycle. These are shown in the IEC 60870-5-103 profile in the Menu Database.

7.2.6 CYCLIC MEASUREMENTS

The device will produce measured values using ASDU 9 on a cyclical basis, this can be read from the device using a Class 2 poll (note ADSU 3 is not used). The rate at which the device produces new measured values can be controlled using the measurement period setting. This setting can be edited from the front panel menu or using MiCOM S1 Agile. It is active immediately following a change.

The device transmits its measurands at 2.4 times the rated value of the analogue value.

7.2.7 COMMANDS

A list of the supported commands is contained in the Menu Database. The device will respond to other commands with an ASDU 1, with a cause of transmission (COT) indicating 'negative acknowledgement'.

7.2.8 TEST MODE

It is possible to disable the device output contacts to allow secondary injection testing to be performed using either the front panel menu or the front serial port. The IEC 60870-5-103 standard interprets this as 'test mode'. An event will be produced to indicate both entry to and exit from test mode. Spontaneous events and cyclic measured data transmitted whilst the device is in test mode will have a COT of 'test mode'.

7.2.9 DISTURBANCE RECORDS

The disturbance records are stored in uncompressed format and can be extracted using the standard mechanisms described in IEC 60870-5-103.

Note:

IEC 60870-5-103 only supports up to 8 records.

7.2.10 COMMAND/MONITOR BLOCKING

The device supports a facility to block messages in the monitor direction (data from the device) and also in the command direction (data to the device). Messages can be blocked in the monitor and command directions using one of the two following methods

- The menu command **RP1 CS103Blcking** in the COMMUNICATIONS column
- The DDB signals Monitor Blocked and Command Blocked

7.2.11 IEC 60870-5-103 CONFIGURATION

To configure the device:

- 1. Select the CONFIGURATION column and check that the Comms settings cell is set to Visible.
- 2. Select the COMMUNICATIONS column.
- 3. Move to the first cell down (*RP1 protocol*). This is a non-settable cell, which shows the chosen communication protocol in this case IEC 60870–5–103.

COMMUNICATIONS
RP1 Protocol
IEC 60870-5-103

4. Move down to the next cell (*RP1 Address*). This cell controls the IEC 60870-5-103 address of the IED. Up to 32 IEDs can be connected to one spur. It is therefore necessary for each IED to have a unique address so that messages from the master control station are accepted by one IED only. IEC 60870-5-103 uses an integer number between 0 and 254 for the address. It is important that no two IEDs have the same IEC 60870 5 103 address. The IEC 60870-5-103 address is then used by the master station to communicate with the IED.

COMMUNICATIONS RP1 address 162

5. Move down to the next cell (*RP1 Baud Rate*). This cell controls the baud rate to be used. Two baud rates are supported by the IED, 9600 bits/s and 19200 bits/s. Make sure that the baud rate selected on the IED is the same as that set on the master station.

COMMUNICATIONS
RP1 Baud rate
9600 bits/s

6. Move down to the next cell (*RP1 Meas Period*). The next cell down controls the period between IEC 60870-5-103 measurements. The IEC 60870-5-103 protocol allows the IED to supply measurements at regular intervals. The interval between measurements is controlled by this cell, and can be set between 1 and 60 seconds.

COMMUNICATIONS
RP1 Meas Period
30.00 s

7. If the optional fibre optic connectors are fitted, the *RP1 PhysicalLink* cell is visible. This cell controls the physical media used for the communication (Copper or Fibre optic).

COMMUNICATIONS RP1 PhysicalLink Copper

8. The next cell down (*RP1 CS103Blcking*) can be used for monitor or command blocking.

COMMUNICATIONS RP1 CS103Blcking Disabled

9. There are three settings associated with this cell; these are:

Setting:	Description:
Disabled	No blocking selected.
Monitor Blocking	When the monitor blocking DDB Signal is active high, either by energising an opto input or control input, reading of the status information and disturbance records is not permitted. When in this mode the device returns a "Termination of general interrogation" message to the master station.
Command Blocking	When the command blocking DDB signal is active high, either by energising an opto input or control input, all remote commands will be ignored (i.e. CB Trip/Close, change setting group etc.). When in this mode the device returns a "negative acknowledgement of command" message to the master station.

7.3 DNP 3.0

This section describes how the DNP 3.0 standard is applied in the product. It is not a description of the standard itself. The level at which this section is written assumes that the reader is already familiar with the DNP 3.0 standard.

The descriptions given here are intended to accompany the device profile document that is included in the Menu Database document. The DNP 3.0 protocol is not described here, please refer to the documentation available from the user group. The device profile document specifies the full details of the DNP 3.0 implementation. This is the standard format DNP 3.0 document that specifies which objects; variations and qualifiers are supported. The device profile document also specifies what data is available from the device using DNP 3.0. The IED operates as a DNP 3.0 slave and supports subset level 2, as described in the DNP 3.0 standard, plus some of the features from level 3.

The DNP 3.0 protocol is defined and administered by the DNP Users Group. For further information on DNP 3.0 and the protocol specifications, please see the DNP website (www.dnp.org).

7.3.1 PHYSICAL CONNECTION AND LINK LAYER

DNP 3.0 can be used with two physical layer protocols: EIA(RS)485, or Ethernet.

Several connection options are available for DNP 3.0

- Rear Port 1 (RP1) for permanent SCADA connection via RS485
- Optional fibre port (RP1 in slot A) for permanent SCADA connection via optical fibre
- An RJ45 connection on an optional Ethernet board for permanent SCADA Ethernet connection
- A fibre connection on an optional Ethernet board for permanent SCADA Ethernet connection

The IED address and baud rate can be selected using the front panel menu or by the settings application software.

When using a serial interface, the data format is: 1 start bit, 8 data bits, 1 stop bit and optional configurable parity bit.

7.3.2 OBJECT 1 BINARY INPUTS

Object 1, binary inputs, contains information describing the state of signals in the IED, which mostly form part of the digital data bus (DDB). In general these include the state of the output contacts and opto-inputs, alarm signals, and protection start and trip signals. The 'DDB number' column in the device profile document provides the DDB numbers for the DNP 3.0 point data. These can be used to cross-reference to the DDB definition list. See the relevant Menu Database document. The binary input points can also be read as change events using Object 2 and Object 60 for class 1-3 event data.

7.3.3 OBJECT 10 BINARY OUTPUTS

Object 10, binary outputs, contains commands that can be operated using DNP 3.0. Therefore the points accept commands of type pulse on (null, trip, close) and latch on/off as detailed in the device profile in the relevant Menu Database document, and execute the command once for either command. The other fields are ignored (queue, clear, trip/close, in time and off time).

There is an additional image of the Control Inputs. Described as Alias Control Inputs, they reflect the state of the Control Input, but with a dynamic nature.

- If the Control Input DDB signal is already SET and a new DNP SET command is sent to the Control Input, the Control Input DDB signal goes momentarily to RESET and then back to SET.
- If the Control Input DDB signal is already RESET and a new DNP RESET command is sent to the Control Input, the Control Input DDB signal goes momentarily to SET and then back to RESET.

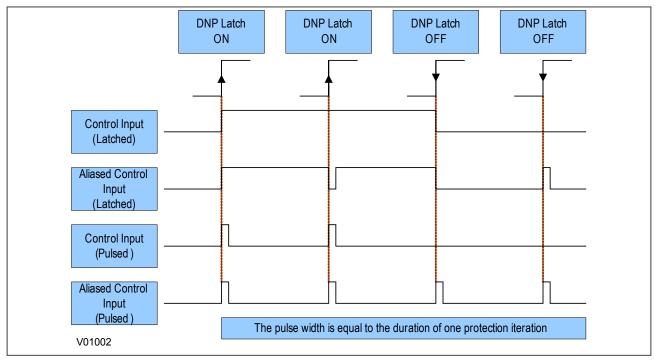


Figure 214: Control input behaviour

Many of the IED's functions are configurable so some of the Object 10 commands described in the following sections may not be available. A read from Object 10 reports the point as off-line and an operate command to Object 12 generates an error response.

Examples of Object 10 points that maybe reported as off-line are:

- Activate setting groups: Ensure setting groups are enabled
- CB trip/close: Ensure remote CB control is enabled
- Reset NPS thermal: Ensure NPS thermal protection is enabled
- Reset thermal O/L: Ensure thermal overload protection is enabled
- Reset RTD flags: Ensure RTD Inputs is enabled
- Control inputs: Ensure control inputs are enabled

7.3.4 OBJECT 20 BINARY COUNTERS

Object 20, binary counters, contains cumulative counters and measurements. The binary counters can be read as their present 'running' value from Object 20, or as a 'frozen' value from Object 21. The running counters of object 20 accept the read, freeze and clear functions. The freeze function takes the current value of the object 20 running counter and stores it in the corresponding Object 21 frozen counter. The freeze and clear function resets the Object 20 running counter to zero after freezing its value.

Binary counter and frozen counter change event values are available for reporting from Object 22 and Object 23 respectively. Counter change events (Object 22) only report the most recent change, so the maximum number of events supported is the same as the total number of counters. Frozen counter change events (Object 23) are generated whenever a freeze operation is performed and a change has occurred since the previous freeze command. The frozen counter event queues store the points for up to two freeze operations.

7.3.5 OBJECT 30 ANALOGUE INPUT

Object 30, analogue inputs, contains information from the IED's measurements columns in the menu. All object 30 points can be reported as 16 or 32-bit integer values with flag, 16 or 32-bit integer values without flag, as well as short floating point values.

Analogue values can be reported to the master station as primary, secondary or normalized values (which takes into account the IED's CT and VT ratios), and this is settable in the *COMMUNICATIONS* column in the IED. Corresponding deadband settings can be displayed in terms of a primary, secondary or normalized value. Deadband point values can be reported and written using Object 34 variations.

The deadband is the setting used to determine whether a change event should be generated for each point. The change events can be read using Object 32 or Object 60. These events are generated for any point which has a value changed by more than the deadband setting since the last time the data value was reported.

Any analogue measurement that is unavailable when it is read is reported as offline. For example, the frequency would be offline if the current and voltage frequency is outside the tracking range of the IED. All Object 30 points are reported as secondary values in DNP 3.0 (with respect to CT and VT ratios).

7.3.6 OBJECT 40 ANALOGUE OUTPUT

The conversion to fixed-point format requires the use of a scaling factor, which is configurable for the various types of data within the IED such as current, voltage, and phase angle. All Object 40 points report the integer scaling values and Object 41 is available to configure integer scaling quantities.

7.3.7 OBJECT 50 TIME SYNCHRONISATION

Function codes 1 (read) and 2 (write) are supported for Object 50 (time and date) variation 1. The DNP Need Time function (the duration of time waited before requesting another time sync from the master) is supported, and is configurable in the range 1 - 30 minutes.

If the clock is being synchronized using the IRIG-B input then it will not be possible to set the device time using the Courier interface. An attempt to set the time using the interface will cause the device to create an event with the current date and time taken from the IRIG-B synchronized internal clock.

7.3.8 DNP3 DEVICE PROFILE

This section describes the specific implementation of DNP version 3.0 within General Electric MiCOM P40 Agile IEDs for both compact and modular ranges.

The devices use the DNP 3.0 Slave Source Code Library version 3 from Triangle MicroWorks Inc.

This document, in conjunction with the DNP 3.0 Basic 4 Document Set, and the DNP Subset Definitions Document, provides complete information on how to communicate with the devices using the DNP 3.0 protocol.

This implementation of DNP 3.0 is fully compliant with DNP 3.0 Subset Definition Level 2. It also contains many Subset Level 3 and above features.

7.3.8.1 DNP3 DEVICE PROFILE TABLE

The following table provides the device profile in a similar format to that defined in the DNP 3.0 Subset Definitions Document. While it is referred to in the DNP 3.0 Subset Definitions as a "Document", it is just one component of a total interoperability guide. This table, in combination with the subsequent Implementation and Points List tables should provide a complete interoperability/configuration guide for the device.

The following table provides the device profile in a similar format to that defined in the DNP 3.0 Subset Definitions Document. While it is referred to in the DNP 3.0 Subset Definitions as a "Document", it is just one component of a total interoperability guide. This table, in combination with the subsequent Implementation and Points List tables should provide a complete interoperability/configuration guide for the device.

	DNP 3.0 Profile Document
Vendor Name:	General Electric
Device Name:	MiCOM P40Agile Protection Relays – compact and modular range

	DNP 3.0 rofile Document
Models Covered:	All models
Highest DNP Level Supported*: *This is the highest DNP level FULLY supported. Parts of level 3 are also supported	For Requests: Level 2 For Responses: Level 2
Device Function:	Slave

Notable objects, functions, and/or qualifiers supported in addition to the highest DNP levels supported (the complete list is described in the DNP 3.0 Implementation Table):

For static (non-change event) object requests, request qualifier codes 00 and 01 (start-stop), 07 and 08 (limited quantity), and 17 and 28 (index) are supported in addition to the request qualifier code 06 (no range (all points))

Static object requests sent with qualifiers 00, 01, 06, 07, or 08 will be responded with qualifiers 00 or 01 $^{\circ}$

Static object requests sent with qualifiers 17 or 28 will be responded with qualifiers 17 or 28

For change-event object requests, qualifiers 17 or 28 are always responded

16-bit and 32-bit analogue change events with time may be requested

The read function code for Object 50 (time and date) variation 1 is supported

Analogue Input Deadbands, Object 34, variations 1 through 3, are supported

Floating Point Analogue Output Status and Output Block Objects 40 and 41 are supported

Sequential file transfer, Object 70, variations 2 through 7, are supported

Device Attribute Object 0 is supported

Maximum Data Link Frame Size (octets):	Transmitted: 292 Received: 292
Maximum Application Fragment Size (octets)	Transmitted: Configurable (100 to 2048). Default 2048 Received: 249
Maximum Data Link Retries:	Fixed at 2
Maximum Application Layer Retries:	None
Requires Data Link Layer Confirmation:	Configurable to Never or Always
Requires Application Layer Confirmation:	When reporting event data (Slave devices only) When sending multi-fragment responses (Slave devices only)
Timeouts while waiting for:	
Data Link Confirm:	Configurable
Complete Application Fragment:	None
Application Confirm:	Configurable
Complete Application Response:	None
Others:	
Data Link Confirm Timeout:	Configurable from 0 (Disabled) to 120s, default 10s.
Application Confirm Timeout:	Configurable from 1 to 120s, default 2s.
Select/Operate Arm Timeout:	Configurable from 1 to 10s, default 10s.
Need Time Interval (Set IIN1-4):	Configurable from 1 to 30, default 10min.
Application File Timeout	60 s
Analog Change Event Scan Period:	Fixed at 0.5s
Counter Change Event Scan Period	Fixed at 0.5s
Frozen Counter Change Event Scan Period	Fixed at 1s
Maximum Delay Measurement Error:	2.5 ms
Time Base Drift Over a 10-minute Interval:	7 ms
Sends/Executes Control Operations:	
Write Binary Outputs:	Never
Select/Operate:	Always

	DNP 3.0
Device P	rofile Document
Direct Operate:	Always
Direct Operate - No Ack:	Always
Count > 1	Never
Pulse On	Always
Pulse Off	Sometimes
Latch On	Always
Latch Off	Always
Queue	Never
Clear Queue	Never
Note: Paired Control points will accept Pulse On/Trip and Pulse On/O	Close, but only single point will accept the Pulse Off control command.
Reports Binary Input Change Events when no specific variation requested:	Configurable to send one or the other
Reports time-tagged Binary Input Change Events when no specific variation requested:	Binary input change with time
Sends Unsolicited Responses:	Never
Sends Static Data in Unsolicited Responses:	Never No other options are permitted
Default Counter Object/Variation:	Configurable, Point-by-point list attached Default object: 20 Default variation: 1
Counters Roll Over at:	32 bits
Sends multi-fragment responses:	Yes
Sequential File Transfer Support:	
Append File Mode	No
Custom Status Code Strings	No
Permissions Field	Yes
File Events Assigned to Class	No
File Events Send Immediately	Yes
Multiple Blocks in a Fragment	No
Max Number of Files Open	1

7.3.8.2 DNP3 IMPLEMENTATION TABLE

The implementation table provides a list of objects, variations and control codes supported by the device:

	Object			Request (Library will parse)				Response (Library will respond with)			
Object Number	Variation Number	Description	Function Codes (dec)		Qualifier Codes (hex)		Function Codes (dec)		Qualifier Codes (hex)		
1	0	Binary Input (Variation 0 is used to request default variation)	1 22	(read) (assign class)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)					
l	1 (default - see note 1)	Binary Input	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(stort-stop) (index - see note 2)	
1	2	Binary Input with Flag	1	(read)	00, 01 06 07, 08 17, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)	

	O.b.	: -			Request				Resp	onse
	Ob	ject		(Libra	ry will p	arse)	(Library will respond with)			
Object Number	Variation Number	Description	Fund	ction Codes (dec)	()ualifier Codes (hex)	Fu	nction Codes (dec)	()ualifier Codes (hex)
2	0	Binary Input Change - Any Variation	1	(read)	06 07, 08	(no range, or all) (limited qty)				
2	1	Binary Input Change without Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
2	2	Binary Input Change with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
10	0	Binary Output Status - Any Variation	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)				
10	2 (default - see note 1)	Binary Output Status	1	(read)	00, 01 06 07, 08 17, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
12	1	Control Relay Output Block	3 4 5 6	(select) (operate) (direct op) (dir. op, noack)	17, 28	(index)	129	response		echo of request
20	0	Binary Counter - Any Variation	1 22	(read) (assign class)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)				
			7 8 9 10	(freeze) (freeze noack) (freeze clear) (frz. cl. Noack)	00, 01 06 07, 08	(start-stop) (no range, or all) (limited qty)				
20	1	32-Bit Binary Counter with Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
20	2	16-Bit Binary Counter with Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
20	5 (default - see note 1)	32-Bit Binary Counter without Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
20	6	16-Bit Binary Counter without Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
21	0	Frozen Counter - Any Variation	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)				
21	1	32-Bit Frozen Counter with Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
21	2	16-Bit Frozen Counter with Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
21	5	32-Bit Frozen Counter with Time of Freeze	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 1)
21	6	16-Bit Frozen Counter with Time of Freeze	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) 17, 28 (index - see note 1)
21	9 (default - see note 1)	32-Bit Frozen Counter without Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)

	Object			ſ	Request				Respo	onse
	Ob	ject	(Library will parse)			(Library will respond with)				
Object Number	Variation Number	Description	Fun	ction Codes (dec)	(ualifier Codes (hex)	Fui	nction Codes (dec)	Q	ualifier Codes (hex)
21	10	16-Bit Frozen Counter without Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
`22	0	Counter Change Event - Any Variation	1	(read)	06 07, 08	(no range, or all) (limited qty)				
22	1 (default - see note 1)	32-Bit Counter Change Event without Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
22	2	16-Bit Counter Change Event without Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
22	5	32-Bit Counter Change Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
22	6	16-Bit Counter Change Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
23	0	Frozen Counter Event (Variation 0 is used to request default variation)	1	(read)	06 07, 08	(no range, or all) (limited qty)				
23	1 (default - see note 1)	32-Bit Frozen Counter Event	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
23	2	16-Bit Frozen Counter Event	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
23	5	32-Bit Frozen Counter Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
23	6	16-Bit Frozen Counter Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
30	0	Analog Input - Any Variation	1 22	(read) (assign class)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)				
30	1	32-Bit Analog Input	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
30	2	16-Bit Analog Input	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
30	3 (default - see note 1)	32-Bit Analog Input without Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
30	4	16-Bit Analog Input without Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
30	5	Short floating point	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
32	0	Analog Change Event - Any Variation	1	(read)	06 07, 08	(no range, or all) (limited qty)				
32	1 (default - see note 1)	32-Bit Analog Change Event without Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
32	2	16-Bit Analog Change Event without Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
32	3	32-Bit Analog Change Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
32	4	16-Bit Analog Change Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
32	5	Short floating point Analog Change Event without Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
32	7	Short floating point Analog Change Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)

					Request				Respo	onse	
	Ob	ject			ry will p	arse)		(Library	y will respond with)		
Object Number	Variation Number	Description	Fund	ction Codes (dec)	()ualifier Codes (hex)	Fui	nction Codes (dec)	Q	ualifier Codes (hex)	
34	0	Analog Input Deadband (Variation 0 is used to request default variation)	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)					
34	1	16 Bit Analog Input Deadband	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)	
			2	(write)	00, 01 07, 08 17, 27, 28	(start-stop) (limited qty) (index)					
34	2 (default - see note 1)	32 Bit Analog Input Deadband	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(stort-stop) (index - see note 2)	
			2	(write)	00, 01 07, 08 17, 27, 28	(start-stop) (limited qty) (index)					
34	3	Short Floating Point Analog Input Deadband	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)	
			2	(write)	00, 01 07, 08 17, 27, 28	(start-stop) (limited qty) (index)					
40	0	Analog Output Status (Variation 0 is used to request default variation)	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)					
40	1 (default - see note 1)	32-Bit Analog Output Status	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(stort-stop) (index - see note 2)	
40	2	16-Bit Analog Output Status	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(stort-stop) (index - see note 2)	
40	3	Short Floating Point Analog Output Status	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(stort-stop) (index - see note 2)	
41	1	32-Bit Analog Output Block	3 4 5 6	(select) (operate) (direct op) (dir. op, noack)	17, 28 27	(index) (index)	129	response		echo of request	
41	2	16-Bit Analog Output Block	3 4 5 6	(select) (operate) (direct op) (dir. op, noack)	17, 28 27	(index) (index)	129	response		echo of request	
41	3	Short Floating Point Analog Output Block	3 4 5 6	(select) (operate) (direct op) (dir. op, noack)	17, 27, 28	(index)	129	response		echo of request	
50	1 (default - see note 1)	Time and Date	1	(read)	07	(limited qty = 1)	129	response	07	(limited qty = 1)	
			2	(write)	07	(limited qty = 1)					
60	0	Not defined					\perp			1	
60	2	Class 0 Data Class 1 Data	1	(read)	06	(no range, or all)					
			122	(and a d.)	07, 08	(limited qty)				-	
60	3	Class 2 Data	1	(assign class)	06 06 07, 08	(no range, or all) (no range, or all) (limited qty)					
			22	(assign class)	06	(no range, or all)					
60	4	Class 3 Data	1	(read)	06 07, 08	(no range, or all) (limited qty)					

	Object			(Libra			Response (Library will respond with)			
Object Number	Variation Number	Description	Fun	ction Codes (dec)		Qualifier Codes (hex)	Fu	nction Codes (dec)	Qualifier Codes (hex)	
			22	(assign class)	06	(no range, or all)				
70	0	File Event - Any Variation	1	(read)	06 07, 08	(no range, or all) (limited qty)				
			22	(assign class)	06	(no range, or all)				
70	2	File Authentication	29	(authenticate)	5b	(free-format)	129	response		5B (free-format)
70	3	File Command	25 27	(open) (delete)	5b	(free-format)				
70	4	File Command Status	26 30	(close) (abort)	5b	(free-format)	129	response		5B (free-format)
70	5	File Transfer	1	(read)	5b	(free-format)	129	response		5B (free-format)
70	6	File Transfer Status					129	response		5B (free-format)
70	7	File Descriptor	28	(get file info)	5b	(free-format)	129	response		5B (free-format)
80	1	Internal Indications	1	(read)	00, 01	(start-stop)	129	response	00,01	(start-stop)
		No Object (function code only)	13	(cold restart)						
		No Object (function code only)	14	(warm restart)						
		No Object (function code only)	23	(delay meas.)						

Note:

A Default variation refers to the variation responded to when variation 0 is requested and/or in class 0, 1, 2, or 3 scans.

Note

For static (non-change-event) objects, qualifiers 17 or 28 are only responded to when a request is sent with qualifiers 17 or 28, respectively. Otherwise, static object requests sent with qualifiers 00, 01, 06, 07, or 08, will be responded to with qualifiers 00 or 01. For change-event objects, qualifiers 17 or 28 are always responded to.

7.3.8.3 DNP3 INTERNAL INDICATIONS

The following table lists the DNP3.0 Internal Indications (IIN) and identifies those that are supported by the device.

The IIN form an information element used to convey the internal states and diagnostic results of a device. This information can be used by a receiving station to perform error recovery or other suitable functions. The IIN is a two-octet field that follows the function code in all responses from the device. When a request cannot be processed due to formatting errors or the requested data is not available, the IIN is always returned with the appropriate bits set.

Bit	Indication	Description	Supported
		Octet 1	
0	All stations message received	Set when a request is received with the destination address of the all stations address (6553510). It is cleared after the next response (even if a response to a global request is required). This IIN is used to let the master station know that a "broadcast" message was received by the relay.	Yes

Bit	Indication	Description	Supported
1	Class 1 data available	Set when data that has been configured as Class 1 data is ready to be sent to the master. The master station should request this class data from the relay when this bit is set in a response.	Yes
2	Class 2 data available	Set when data that has been configured as Class 2 data is ready to be sent to the master. The master station should request this class data from the relay when this bit is set in a response.	Yes
3	Class 3 data available	Set when data that has been configured as Class 3 data is ready to be sent to the master. The master station should request this class data from the relay when this bit is set in a response.	Yes
4	Time-synchronization required	The relay requires time synchronization from the master station (using the Time and Date object). This IIN is cleared once the time has been synchronized. It can also be cleared by explicitly writing a 0 into this bit of the Internal Indication object.	Yes
5	Local	Set when some or all of the relays digital output points (Object 10/12) are in the Local state. That is, the relays control outputs are NOT accessible through the DNP protocol. This IIN is clear when the relay is in the Remote state. That is, the relays control outputs are fully accessible through the DNP protocol.	No
6	Device in trouble	Set when an abnormal condition exists in the relay. This IIN is only used when the state cannot be described by a combination of one or more of the other IIN bits.	No
7	Device restart	Set when the device software application restarts. This IIN is cleared when the master station explicitly writes a 0 into this bit of the Internal Indications object.	Yes
		Octet 2	
0	Function code not implemented	The received function code is not implemented within the relay.	Yes
1	Requested object(s) unknown	The relay does not have the specified objects or there are no objects assigned to the requested class. This IIN should be used for debugging purposes and usually indicates a mismatch in device profiles or configuration problems.	Yes
2	Out of range	Parameters in the qualifier, range or data fields are not valid or out of range. This is a 'catch-all' for application request formatting errors. It should only be used for debugging purposes. This IIN usually indicates configuration problems.	Yes
3	Buffer overflow	Event buffer(s), or other application buffers, have overflowed. The master station should attempt to recover as much data as possible and indicate to the user that there may be lost data. The appropriate error recovery procedures should be initiated by the user.	Yes
4	Already executing	The received request was understood but the requested operation is already executing.	
5	Bad configuration	Set to indicate that the current configuration in the relay is corrupt. The master station may download another configuration to the relay.	Yes
6	Reserved	Always returned as zero.	
7	Reserved	Always returned as zero.	

7.3.8.4 DNP3 RESPONSE STATUS CODES

When the device processes Control Relay Output Block (Object 12) requests, it returns a set of status codes; one for each point contained within the original request. The complete list of codes appears in the following table:

Code Number	Identifier Name	Description
0	Success	The received request has been accepted, initiated, or queued.
1	Timeout	The request has not been accepted because the 'operate' message was received after the arm timer (Select Before Operate) timed out. The arm timer was started when the select operation for the same point was received.
2	No select	The request has not been accepted because no previous matching 'select' request exists. (An 'operate' message was sent to activate an output that was not previously armed with a matching 'select' message).
3	Format error	The request has not been accepted because there were formatting errors in the control request ('select', 'operate', or 'direct operate').
4	Not supported	The request has not been accepted because a control operation is not supported for this point.
5	Already active	The request has not been accepted because the control queue is full or the point is already active.
6	Hardware error	The request has not been accepted because of control hardware problems.
7	Local	The request has not been accepted because local access is in progress.
8	Too many operations	The request has not been accepted because too many operations have been requested.
9	Not authorized	The request has not been accepted because of insufficient authorization.
127	Undefined	The request not been accepted because of some other undefined reason.

Note:

Code numbers 10 through to 126 are reserved for future use.

7.3.9 DNP3 CONFIGURATION

To configure the device:

- 1. Select the CONFIGURATION column and check that the Comms settings cell is set to Visible.
- 2. Select the COMMUNICATIONS column.
- 3. Move to the first cell down (*RP1 protocol*). This is a non-settable cell, which shows the chosen communication protocol in this case *DNP3.0*.

COMMUNICATIONS RP1 Protocol DNP3.0

4. Move down to the next cell (*RP1 Address*). This cell controls the DNP3.0 address of the IED. Up to 32 IEDs can be connected to one spur, therefore it is necessary for each IED to have a unique address so that messages from the master control station are accepted by only one IED. DNP3.0 uses a decimal number between 1 and 65519 for the Relay Address. It is important that no two IEDs have the same address.

COMMUNICATIONS RP1 Address 1

5. Move down to the next cell (*RP1 Baud Rate*). This cell controls the baud rate to be used. Six baud rates are supported by the IED 1200 bps, 2400 bps, 4800 bps, 9600 bps, 19200 bps and 38400 bps. Make sure that the baud rate selected on the IED is the same as that set on the master station.

COMMUNICATIONS RP1 Baud rate 9600 bits/s

6. Move down to the next cell (*RP1 Parity*). This cell controls the parity format used in the data frames. The parity can be set to be one of *None*, *Odd* or *Even*. Make sure that the parity format selected on the IED is the same as that set on the master station.

COMMUNICATIONS
RP1 Parity
None

7. If the optional fibre optic connectors are fitted, the *RP1 PhysicalLink* cell is visible. This cell controls the physical media used for the communication (Copper or Fibre optic).

COMMUNICATIONS RP1 PhysicalLink Copper

8. Move down to the next cell (*RP1 Time Sync*). This cell affects the time synchronisation request from the master by the IED. It can be set to *enabled* or *disabled*. If enabled it allows the DNP3.0 master to synchronise the time on the IED.

COMMUNICATIONS RP1 Time Sync Enabled

7.3.9.1 DNP3 CONFIGURATOR

A PC support package for DNP3.0 is available as part of the supplied settings application software (MiCOM S1 Agile) to allow configuration of the device's DNP3.0 response. The configuration data is uploaded from the device to the PC in a block of compressed format data and downloaded in a similar manner after modification. The new DNP3.0 configuration takes effect after the download is complete. To restore the default configuration at any time, from the CONFIGURATION column, select the Restore Defaults cell then select All Settings.

In MiCOM S1 Agile, the DNP3.0 data is shown in three main folders, one folder each for the point configuration, integer scaling and default variation (data format). The point configuration also includes screens for binary inputs, binary outputs, counters and analogue input configuration.

If the device supports DNP Over Ethernet, the configuration related settings are done in the folder **DNP Over Ethernet**.

7.4 MODBUS

This section describes how the MODBUS standard is applied to the Px40 platform. It is not a description of the standard itself. The level at which this section is written assumes that the reader is already familiar with the MODBUS standard.

The MODBUS protocol is a master/slave protocol, defined and administered by the MODBUS Organization For further information on MODBUS and the protocol specifications, please seethe Modbus web site (www.modbus.org).

7.4.1 PHYSICAL CONNECTION AND LINK LAYER

Two connection options are available for MODBUS

- Rear Port 1 (RP1) for permanent SCADA connection via RS485
- Optional fibre port (RP1 in slot A) for permanent SCADA connection via optical fibre

The MODBUS interface uses 'RTU' mode communication rather than 'ASCII' mode as this provides more efficient use of the communication bandwidth. This mode of communication is defined by the MODBUS standard.

The IED address and baud rate can be selected using the front panel menu or by the settings application software.

When using a serial interface, the data format is: 1 start bit, 8 data bits, 1 parity bit with 1 stop bit, or 2 stop bits (a total of 11 bits per character).

7.4.2 MODBUS FUNCTIONS

The following MODBUS function codes are supported:

- 01: Read Coil Status
- 02: Read Input Status
- 03: Read Holding Registers
- 04: Read Input Registers
- 06: Preset Single Register
- 08: Diagnostics
- 11: Fetch Communication Event Counter
- 12: Fetch Communication Event Log
- 16: Preset Multiple Registers 127 max

These are interpreted by the MiCOM IED in the following way:

- 01: Read status of output contacts (0xxxx addresses)
- 02: Read status of opto inputs (1xxxx addresses)
- 03: Read setting values (4xxxx addresses)
- 04: Read measured values (3xxxx addresses
- 06: Write single setting value (4xxxx addresses)
- 16: Write multiple setting values (4xxxx addresses)

7.4.3 RESPONSE CODES

MCode	MODBUS Description	MiCOM Interpretation
01	Illegal Function Code	The function code transmitted is not supported by the slave.
02	Illegal Data Address	The start data address in the request is not an allowable value. If any of the addresses in the range cannot be accessed due to password protection then all changes within the request are discarded and this error response will be returned. Note: If the start address is correct but the range includes non-implemented addresses this response is not produced.
03	Illegal Value	A value referenced in the data field transmitted by the master is not within range. Other values transmitted within the same packet will be executed if inside range.
06	Slave Device Busy	The write command cannot be implemented due to the database being locked by another interface. This response is also produced if the software is busy executing a previous request.

7.4.4 REGISTER MAPPING

The device supports the following memory page references:

- Memory Page: Interpretation
- Oxxxx: Read and write access of the output relays
- 1xxxx: Read only access of the opto inputs
- 3xxxx: Read only access of data
- 4xxxx: Read and write access of settings

where xxxx represents the addresses available in the page (0 to 9999).

A complete map of the MODBUS addresses supported by the device is contained in the relevant menu database, which is available on request.

Note:

The "extended memory file" (6xxxx) is not supported.

Note:

MODBUS convention is to document register addresses as ordinal values whereas the actual protocol addresses are literal values. The MiCOM relays begin their register addresses at zero. Therefore, the first register in a memory page is register address zero. The second register is register address 1 and so on.

Note:

The page number notation is not part of the address.

7.4.5 EVENT EXTRACTION

The device supports two methods of event extraction providing either automatic or manual extraction of the stored event, fault, and maintenance records.

7.4.5.1 AUTOMATIC EVENT RECORD EXTRACTION

The automatic extraction facilities allow all types of record to be extracted as they occur. Event records are extracted in sequential order including any fault or maintenance data that may be associated with the event.

The MODBUS master can determine whether the device has any events stored that have not yet been extracted. This is performed by reading the status register 30001 (G26 data type). If the event bit of this register is set then the device has non-extracted events available. To select the next event for sequential extraction, the master station writes a value of 1 to the record selection register 40400 (G18 data type). The event data together with any fault/maintenance data can be read from the registers specified below. Once the data has been read, the event record can be marked as having been read by writing a value of '2' to register 40400.

7.4.5.2 MANUAL EVENT RECORD EXTRACTION

There are three registers available to manually select stored records and three read-only registers allowing the number of stored records to be determined.

- 40100: Select Event
- 40101: Select Fault
- 40102: Select Maintenance Record

For each of the above registers a value of 0 represents the most recent stored record. The following registers can be read to indicate the numbers of the various types of record stored.

- 30100: Number of stored records.
- 30101: Number of stored fault records
- 30102: Number of stored maintenance records

Each fault or maintenance record logged causes an event record to be created. If this event record is selected, the additional registers allowing the fault or maintenance record details will also become populated.

7.4.5.3 RECORD DATA

The location and format of the registers used to access the record data is the same whether they have been selected using either automatic or manual extraction.

Event Description	MODBUS Address	Length	Comments
Time and Date	30103	4	See G12 data type description
Event Type	30107	1	See G13 data type description
Event Value	30108	2	Nature of value depends on event type. This will contain the status as a binary flag for contact, opto-input, alarm, and protection events.
MODBUS Address	30110	1	This indicates the MODBUS register address where the change occurred. Alarm 30011 Relays 30723 Optos 30725 Protection events – like the relay and opto addresses this will map onto the MODBUS address of the appropriate DDB status register depending on which bit of the DDB the change occurred. These will range from 30727 to 30785. For platform events, fault events and maintenance events the default is 0.
Event Index	30111	1	This register will contain the DDB ordinal for protection events or the bit number for alarm events. The direction of the change will be indicated by the most significant bit; 1 for 0 – 1 change and 0 for 1 – 0 change.
Additional Data Present	30112	1	0 means that there is no additional data. 1 means fault record data can be read from 30113 to 30199 (number of registers depends on the product). 2 means maintenance record data can be read from 30036 to 30039.

If a fault record or maintenance record is directly selected using the manual mechanism then the data can be read from the register ranges specified above. The event record data in registers 30103 to 30111 will not be available.

It is possible using register 40401(G6 data type) to independently clear the stored relay event/fault and maintenance records. This register also provides an option to reset the device indications, which has the same effect on the relay as pressing the clear key within the alarm viewer using the HMI panel menu.

7.4.6 DISTURBANCE RECORD EXTRACTION

The IED provides facilities for both manual and automatic extraction of disturbance records.

Records extracted over MODBUS from Px40 devices are presented in COMTRADE format. This involves extracting an ASCII text configuration file and then extracting a binary data file.

Each file is extracted by reading a series of data pages from the IED The data page is made up of 127 registers, giving a maximum transfer of 254 bytes per page.

The following set of registers is presented to the master station to support the extraction of uncompressed disturbance records:

MODBUS registers

MODBUS Register	Name	Description
3x00001	Status register	Provides the status of the relay as bit flags: b0: Out of service b1: Minor self test failure b2: Event b3: Time synchronization b4: Disturbance b5: Fault b6: Trip b7: Alarm b8 to b15: Unused A '1' on b4 indicates the presence of a disturbance
3×00800	No of stored disturbances	Indicates the total number of disturbance records currently stored in the relay, both extracted and non-extracted.

MODBUS Register	Name	Description
3x00801	Unique identifier of the oldest disturbance record	Indicates the unique identifier value for the oldest disturbance record stored in the relay. This is an integer value used in conjunction with the 'Number of stored disturbances' value to calculate a value for manually selecting records.
4x00250	Manual disturbance record selection register	This register is used to manually select disturbance records. The values written to this cell are an offset of the unique identifier value for the oldest record. The offset value, which ranges from 0 to the Number of stored disturbances - 1, is added to the identifier of the oldest record to generate the identifier of the required record.
4x00400	Record selection command register	This register is used during the extraction process and has a number of commands. These are: b0: Select next event b1: Accept event b2: Select next disturbance record b3: Accept disturbance record b4: Select next page of disturbance data b5: Select data file
3x00930 - 3x00933	Record time stamp	These registers return the timestamp of the disturbance record.
3x00802	No of registers in data page	This register informs the master station of the number of registers in the data page that are populated.
3x00803 - 3x00929	Data page registers	These 127 registers are used to transfer data from the relay to the master station. They are 16-bit unsigned integers.
3x00934	Disturbance record status register	The disturbance record status register is used during the extraction process to indicate to the master station when data is ready for extraction. See next table.
4x00251	Data file format selection	This is used to select the required data file format. This is reserved for future use.

Note:

Register addresses are provided in reference code + address format. E.g. 4×00001 is reference code $4\times$, address 1 (which is specified as function code 03, address 0×0000 in the MODBUS specification).

The disturbance record status register will report one of the following values:

Disturbance record states

State	Description
Idle	This will be the state reported when no record is selected; such as after power on or after a record has been marked as extracted.
Busy	The relay is currently processing data.
Page ready	The data page has been populated and the master station can now safely read the data.
Configuration complete	All of the configuration data has been read without error.
Record complete	All of the disturbance data has been extracted.
Disturbance overwritten	An error occurred during the extraction process where the disturbance being extracted was overwritten by a new record.
No non-extracted disturbances	An attempt was made by the master station to automatically select the next oldest non-extracted disturbance when all records have been extracted.
Not a valid disturbance	An attempt was made by the master station to manually select a record that did not exist in the relay.
Command out of sequence	The master station issued a command to the relay that was not expected during the extraction process.

7.4.6.1 MANUAL EXTRACTION PROCEDURE

The procedure used to extract a disturbance manually is shown below. The manual method of extraction does not allow for the acceptance of disturbance records.

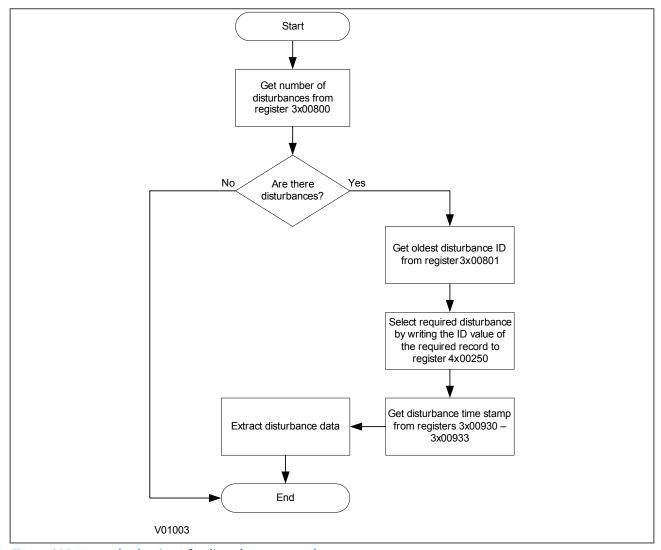


Figure 215: Manual selection of a disturbance record

7.4.6.2 AUTOMATIC EXTRACTION PROCEDURE

There are two methods that can be used for automatically extracting disturbances:

Method 1

Method 1 is simpler and is better at extracting single disturbance records (when the disturbance recorder is polled regularly).

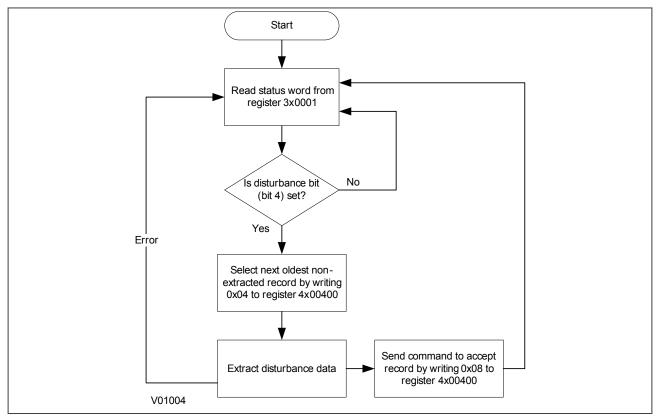


Figure 216: Automatic selection of disturbance record - method 1

Method 2

Method 2 is more complex to implement but is more efficient at extracting large quantities of disturbance records. This may be useful when the disturbance recorder is polled only occasionally and therefore may have many stored records.

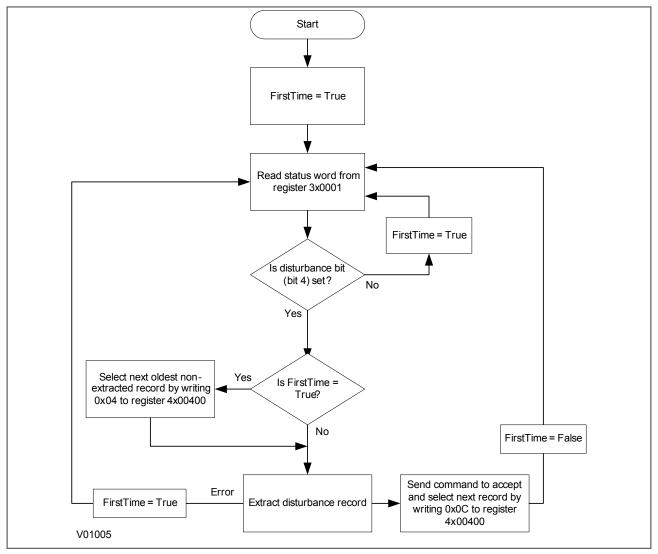


Figure 217: Automatic selection of disturbance record - method 2

7.4.6.3 EXTRACTING THE DISTURBANCE DATA

The extraction of the disturbance record is a two-stage process that involves extracting the configuration file first and then the data file. first the configuration file must be extracted, followed by the data file:

Extracting the Comtrade configuration file

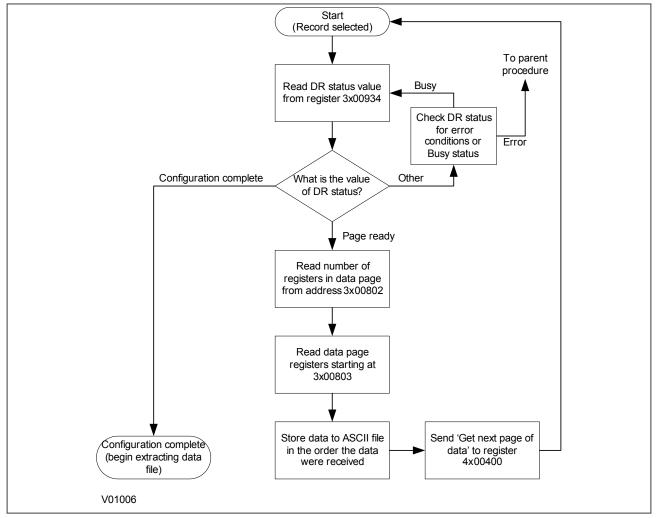


Figure 218: Configuration file extraction

Extracting the comtrade data file

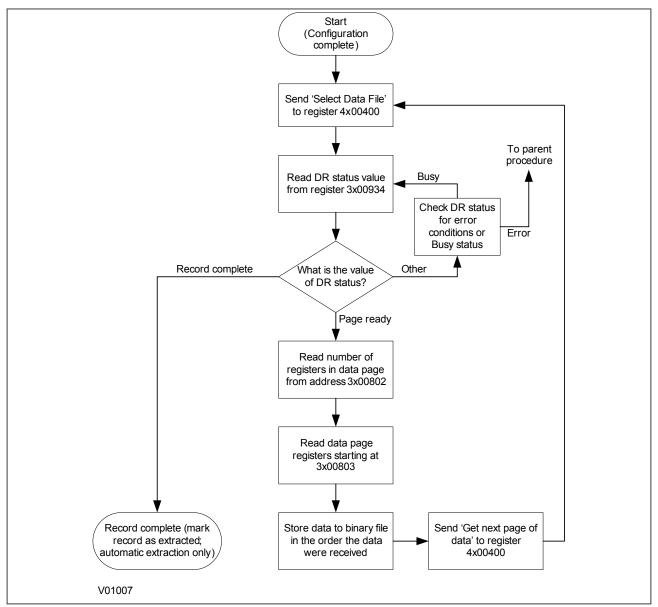


Figure 219: Data file extraction

During the extraction of the COMTRADE files, an error may occur, which will be reported on the DR Status register 3x00934. In this case, you must take action to re-start the record extraction or to abort according to the table below.

Value	State	Description
0	Idle	This will be the state reported when no record is selected; such as after power on or after a record has been marked as extracted.
1	Busy	The relay is currently processing data.
2	Page ready	The data page has been populated and the master station can now safely read the data.
3	Configuration complete	All of the configuration data has been read without error.
4	Record complete	All of the disturbance data has been extracted.
5	Disturbance overwritten	An error occurred during the extraction process where the disturbance being extracted was overwritten by a new record.

Value	State	Description
6		An attempt was made by the master station to automatically select the next oldest unextracted disturbance when all records have been extracted.
7	Not a valid disturbance	An attempt was made by the master station to manually select a record that did not exist in the relay.
8	Command out of sequence	The master station issued a command to the relay that was not expected during the extraction process.

7.4.7 SETTING CHANGES

All the IED settings are 4xxxx page addresses. The following points should be noted when changing settings:

- Settings implemented using multiple registers must be written to using a multi-register write operation.
- The first address for a multi-register write must be a valid address. If there are unmapped addresses within the range being written to, the data associated with these addresses will be discarded.
- If a write operation is performed with values that are out of range, the illegal data response will be produced. Valid setting values within the same write operation will be executed.
- If a write operation is performed, which attempts to change registers requiring a higher level of password access than is currently enabled then all setting changes in the write operation will be discarded.

7.4.8 PASSWORD PROTECTION

The following registers are available to control password protection:

Function	MODBUS Registers
Password entry	4x00001 to 4x00002 and 4x20000 to 4x20003
Setting to change password level 1 (4 character)	4x00023 to 4x00024
Setting to change password level 1 (8 character)	4x20008 to 4x20011
Setting to change password level 2	4x20016 to 4x20019
Setting to change password level 3	4x20024 to 4x20027
Can be read to indicate current access level	3×00010

7.4.9 PROTECTION AND DISTURBANCE RECORDER SETTINGS

Setting changes to either of these areas are stored in a scratchpad area and will not be used by the IED unless confirmed. Register 40405 can be used either to confirm or abort the setting changes within the scratchpad area.

The IED supports four groups of protection settings. The MODBUS addresses for each of the four groups are repeated within the following address ranges.

- Group 1: 4x1000 4x2999
- Group 2: 4x3000 4x4999
- Group 3: 4x5000 4x6999
- Group 4: 4x7000 4x8999

In addition to the basic editing of the protection setting groups, the following functions are provided:

- Default values can be restored to a setting group or to all of the relay settings by writing to register 4x0402.
- It is possible to copy the contents of one setting group to another by writing the source group to register 40406 and the target group to 4×0407 .

The setting changes performed by either of the two operations defined above are made to the scratchpad area. These changes must be confirmed by writing to register 4x0405.

The active protection setting groups can be selected by writing to register 40404. An illegal data response will be returned if an attempt is made to set the active group to one that has been disabled.

7.4.10 TIME SYNCHRONISATION

The date-time data type G12 allows *real* date and time information to be conveyed to a resolution of 1 ms. The structure of the data type is compliant with the IEC 60870-5-4 **Binary Time 2a** format.

The seven bytes of the date/time frame are packed into four 16-bit registers and are transmitted in sequence starting from byte 1. This is followed by a null byte, making eight bytes in total.

Register data is usually transmitted starting with the highest-order byte. Therefore byte 1 will be in the high-order byte position followed by byte 2 in the low-order position for the first register. The last register will contain just byte 7 in the high order position and the low order byte will have a value of zero.

G12 date & time data type structure

		Bit Position						
Byte	7	6	5	4	3	2	1	0
1	m7	m6	m5	m4	m3	m2	m1	m0
2	m15	m14	m13	m12	m11	m10	m9	m8
3	IV	R	15	14	13	12	11	10
4	SU	R	R	H4	Н3	H2	H1	Н0
5	W2	W1	W0	D4	D3	D2	D1	D0
6	R	R	R	R	M3	M2	M1	MO
7	R	Y6	Y5	Y4	Y3	Y2	Y1	Y0

Key to table:

m = milliseconds: 0 to 59.999

I = minutes: 0 to 59H = hours: 0 to 23

• W = day of the week: 1 to 7 starting from Monday

• D = day of the month: 1 to 31

• M = month of the year: 1 to 12 starting from January

• Y = year of the century: 0 to 99

R = reserved: 0

SU = summertime: 0 = GMT, 1 = summertime
 IV = invalid: 0 = invalid value, 1 = valid value

Since the range of the data type is only 100 years, the century must be deduced. The century is calculated as the one that will produce the nearest time value to the current date. For example: 30-12-99 is 30-12-1999 when received in 1999 & 2000, but is 30-12-2099 when received in 2050. This technique allows 2 digit years to be accurately converted to 4 digits in a ± 50 year window around the current date.

The invalid bit has two applications:

- It can indicate that the date-time information is considered inaccurate, but is the best information available.
- It can indicate that the date-time information is not available.

The summertime bit is used to indicate that summertime (day light saving) is being used and, more importantly, to resolve the alias and time discontinuity which occurs when summertime starts and ends. This is important for the correct time correlation of time stamped records.

The day of the week field is optional and if not calculated will be set to zero.

The concept of time zone is not catered for by this data type and hence by the relay. It is up to the end user to determine the time zone. Normal practice is to use UTC (universal co-ordinated time).

7.4.11 POWER AND ENERGY MEASUREMENT DATA FORMATS

The power and energy measurements are available in two data formats:

Data Type G29: an integer format using 3 registers

Data Type G125: a 32 bit floating point format using 2 registers

The G29 registers are listed in the first part of the MEASUREMENTS 2 column of the Courier database. The G125 equivalents appear at the end of the MEASUREMENTS 2 column.

Data type G29

Data type G29 consists of three registers:

The first register is the per unit (or normalised) power or energy measurement. It is a signed 16 bit quantity. This register is of Data Type G28.

The second and third registers contain a multiplier to convert the per unit value to a real value. These are unsigned 32-bit quantities. These two registers together are of Data Type G27.

Thee overall power or energy value conveyed by the G29 data type is therefore $G29 = G28 \times G27$.

The IED calculates the G28 per unit power or energy value as:

G28 = (measured secondary quantity/CT secondary)(110V/(VT secondary).

Since data type G28 is a signed 16-bit integer, its dynamic range is constrained to \pm 32768. You should take this limitation into consideration for the energy measurements, as the G29 value will saturate a long time before the equivalent G125 does.

The associated G27 multiplier is calculated as:

G27 = (CT primary)(VT primary/110V) when primary value measurements are selected

and

G27 = (CT secondary)(VT secondary/110V) when secondary value measurements are selected.

Due to the required truncations from floating point values to integer values in the calculations of the G29 component parts and its limited dynamic range, we only recommend using G29 values when the MODBUS master cannot deal with the G125 IEEE754 floating point equivalents.

Note:

The G29 values must be read in whole multiples of three registers. It is not possible to read the G28 and G27 parts with separate read commands.

Example of Data Type G29

Assuming the CT/VT configurations are as follows:

- Main VT Primary 6.6 kV
- Main VT Secondary 110 V
- Phase CT Primary 3150 A
- Phase CT Secondary 1 A

The Three-phase Active Power displayed on the measurement panel on the front display of the IED would be 21.94 MW

The registers related to the Three-phase Active Power are: 3x00327, 3x00328, 3x00329

Register Address	Data read from these registers	Format of the data
3x00327	116	G28
3x00328	2	G27

Register Address	Data read from these registers	Format of the data
3x00329	57928	G27

The Equivalent G27 value = $[2^{16} * Value in the address 3x00328 + Value in the address 3x00329] = 216*2 + 57928 = 189000$

The Equivalent value of power G29 = G28 * Equivalent G27 =116 * 189000 =21.92 MW

Note

The above calculated value (21.92 MW) is same as the power value measured on the front panel display.

Data type G125

Data type G125 is a short float IEEE754 floating point format, which occupies 32 bits in two consecutive registers. The high order byte of the format is in the first (low order) register and the low order byte in the second register.

The value of the G125 measurement is as accurate as the IED's ability to resolve the measurement after it has applied the secondary or primary scaling factors. It does not suffer from the truncation errors or dynamic range limitations associated with the G29 data format.

7.4.12 MODBUS CONFIGURATION

To configure the device:

- 1. Select the CONFIGURATION column and check that the Comms settings cell is set to Visible.
- 2. Select the COMMUNICATIONS column.
- 3. Move to the first cell down (*RP1 protocol*). This is a non settable cell, which shows the chosen communication protocol in this case *Modbus*.

COMMUNICATIONS RP1 Protocol Modbus

4. Move down to the next cell (*RP1 Address*). This cell controls the Modbus address of the IED. Up to 32 IEDs can be connected to one spur, therefore it is necessary for each IED to have a unique address so that messages from the master control station are accepted by only one IED. Modbus uses a decimal number between 1 and 247 for the Relay Address. It is important that no two IEDs have the same address.

COMMUNICATIONS
RP1 Address
1

5. Move down to the next cell (*RP1 InactivTimer*). This cell controls the inactivity timer. The inactivity timer controls how long the IED waits without receiving any messages on the rear port before it reverts to its default state, including revoking any password access that was enabled. For the rear port this can be set between 1 and 30 minutes.

COMMUNICATIONS RP1 Inactivtimer 10.00 mins

6. Move down to the next cell (*RP1 Baud Rate*). This cell controls the baud rate to be used. Six baud rates are supported by the IED 1200 bits/s, 2400 bits/s, 4800 bits/s, 9600 bits/s, 19200 bits/s and 38400 bits/s. Make sure that the baud rate selected on the IED is the same as that set on the master station.

COMMUNICATIONS
RP1 Baud rate
9600 bits/s

7. Move down to the next cell (*RP1 Parity*). This cell controls the parity format used in the data frames. The parity can be set to be one of *None*, *Odd* or *Even*. Make sure that the parity format selected on the IED is the same as that set on the master station.

COMMUNICATIONS RP1 Parity None

8. Move down to the next cell (*Modbus IEC Time*). This cell controls the order in which the bytes of information are transmitted. There is a choice of Standard or Reverse. When *Standard* is selected the time format complies with IEC 60870-5-4 requirements such that byte 1 of the information is transmitted first, followed by bytes 2 through to 7. If *Reverse* is selected the transmission of information is reversed.

COMMUNICATIONS Modbus IEC Time Standard

7.5 IEC 61850

This section describes how the IEC 61850 standard is applied to General Electric products. It is not a description of the standard itself. The level at which this section is written assumes that the reader is already familiar with the IEC 61850 standard.

IEC 61850 is the international standard for Ethernet-based communication in substations. It enables integration of all protection, control, measurement and monitoring functions within a substation, and additionally provides the means for interlocking and inter-tripping. It combines the convenience of Ethernet with the security that is so essential in substations today.

There are two editions of IEC 61850; IEC 61850 edition 1 and IEC 61850 edition 2. The edition which this product supports depends on your exact model.

7.5.1 BENEFITS OF IEC 61850

The standard provides:

- Standardised models for IEDs and other equipment within the substation
- Standardised communication services (the methods used to access and exchange data)
- Standardised formats for configuration files
- Peer-to-peer communication

The standard adheres to the requirements laid out by the ISO OSI model and therefore provides complete vendor interoperability and flexibility on the transmission types and protocols used. This includes mapping of data onto

Ethernet, which is becoming more and more widely used in substations, in favour of RS485. Using Ethernet in the substation offers many advantages, most significantly including:

- Ethernet allows high-speed data rates (currently 100 Mbps, rather than tens of kbps or less used by most serial protocols)
- Ethernet provides the possibility to have multiple clients
- Ethernet is an open standard in every-day use
- There is a wide range of Ethernet-compatible products that may be used to supplement the LAN installation (hubs, bridges, switches)

7.5.2 IEC 61850 INTEROPERABILITY

A major benefit of IEC 61850 is interoperability. IEC 61850 standardizes the data model of substation IEDs, which allows interoperability between products from multiple vendors.

An IEC 61850-compliant device may be interoperable, but this does not mean it is interchangeable. You cannot simply replace a product from one vendor with that of another without reconfiguration. However the terminology is pre-defined and anyone with prior knowledge of IEC 61850 should be able to integrate a new device very quickly without having to map all of the new data. IEC 61850 brings improved substation communications and interoperability to the end user, at a lower cost.

7.5.3 THE IEC 61850 DATA MODEL

The data model of any IEC 61850 IED can be viewed as a hierarchy of information, whose nomenclature and categorization is defined and standardized in the IEC 61850 specification.

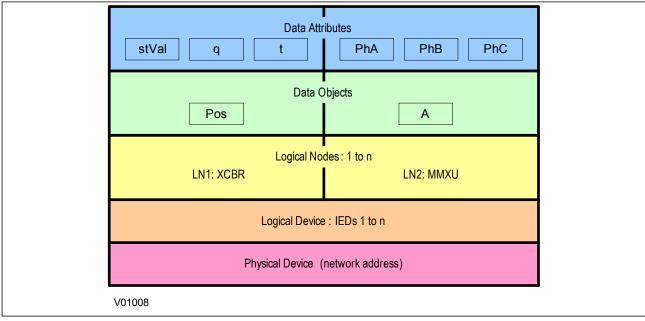


Figure 220: Data model layers in IEC 61850

The levels of this hierarchy can be described as follows:

Data Frame format

Layer	Description
	Identifies the actual IED within a system. Typically the device's name or IP address can be used (for example Feeder_1 or 10.0.0.2.
	Identifies groups of related Logical Nodes within the Physical Device. For the MiCOM IEDs, 5 Logical Devices exist: Control, Measurements, Protection, Records, System.

Layer	Description
Wrapper/Logical Node Instance	Identifies the major functional areas within the IEC 61850 data model. Either 3 or 6 characters are used as a prefix to define the functional group (wrapper) while the actual functionality is identified by a 4 character Logical Node name suffixed by an instance number. For example, XCBR1 (circuit breaker), MMXU1 (measurements), FrqPTOF2 (overfrequency protection, stage 2).
Data Object	This next layer is used to identify the type of data you will be presented with. For example, Pos (position) of Logical Node type XCBR.
Data Attribute	This is the actual data (measurement value, status, description, etc.). For example, stVal (status value) indicating actual position of circuit breaker for Data Object type Pos of Logical Node type XCBR.

7.5.4 IEC 61850 IN MICOM IEDS

IEC 61850 is implemented by use of a separate Ethernet card. This Ethernet card manages the majority of the IEC 61850 implementation and data transfer to avoid any impact on the performance of the protection functions.

To communicate with an IEC 61850 IED on Ethernet, it is necessary only to know its IP address. This can then be configured into either:

- An IEC 61850 client (or master), for example a bay computer (MiCOM C264)
- An HMI
- An MMS browser, with which the full data model can be retrieved from the IED, without any prior knowledge
 of the IED

The IEC 61850 compatible interface standard provides capability for the following:

- Read access to measurements
- Refresh of all measurements at the rate of once per second.
- Generation of non-buffered reports on change of status or measurement
- SNTP time synchronization over an Ethernet link. (This is used to synchronize the IED's internal real time clock.
- GOOSE peer-to-peer communication
- Disturbance record extraction by file transfer. The record is extracted as an ASCII format COMTRADE file
- Controls (Direct and Select Before Operate)

Note:

Setting changes are not supported in the current IEC 61850 implementation. Currently these setting changes are carried out using the settings application software.

7.5.5 IEC 61850 DATA MODEL IMPLEMENTATION

The data model naming adopted in the IEDs has been standardised for consistency. Therefore the Logical Nodes are allocated to one of the five Logical Devices, as appropriate.

The data model is described in the Model Implementation Conformance Statement (MICS) document, which is available as a separate document.

7.5.6 IEC 61850 COMMUNICATION SERVICES IMPLEMENTATION

The IEC 61850 communication services which are implemented in the IEDs are described in the Protocol Implementation Conformance Statement (PICS) document, which is available as a separate document.

7.5.7 IEC 61850 PEER-TO-PEER (GOOSE) COMMUNICATIONS

The implementation of IEC 61850 Generic Object Oriented Substation Event (GOOSE) enables faster communication between IEDs offering the possibility for a fast and reliable system-wide distribution of input and output data values. The GOOSE model uses multicast services to deliver event information. Multicast messaging means that messages are sent to selected devices on the network. The receiving devices can specifically accept frames from certain devices and discard frames from the other devices. It is also known as a publisher-subscriber system. When a device detects a change in one of its monitored status points it publishes a new message. Any device that is interested in the information subscribes to the data it contains.

7.5.8 MAPPING GOOSE MESSAGES TO VIRTUAL INPUTS

Each GOOSE signal contained in a subscribed GOOSE message can be mapped to any of the virtual inputs within the PSL. The virtual inputs allow the mapping to internal logic functions for protection control, directly to output contacts or LEDs for monitoring.

An IED can subscribe to all GOOSE messages but only the following data types can be decoded and mapped to a virtual input:

- BOOLEAN
- BSTR2
- INT16
- INT32
- INT8
- UINT16
- UINT32
- UINT8

7.5.8.1 IEC 61850 GOOSE CONFIGURATION

All GOOSE configuration is performed using the IEC 61850 Configurator tool available in the MiCOM S1 Agile software application.

All GOOSE publishing configuration can be found under the **GOOSE Publishing** tab in the configuration editor window. All GOOSE subscription configuration parameters are under the **External Binding** tab in the configuration editor window.

Settings to enable GOOSE signalling and to apply Test Mode are available using the HMI.

7.5.9 ETHERNET FUNCTIONALITY

IEC 61850 **Associations** are unique and made between the client and server. If Ethernet connectivity is lost for any reason, the associations are lost, and will need to be re-established by the client. The IED has a **TCP_KEEPALIVE** function to monitor each association, and terminate any which are no longer active.

The IED allows the re-establishment of associations without disruption of its operation, even after its power has been removed. As the IED acts as a server in this process, the client must request the association. Uncommitted settings are cancelled when power is lost, and reports requested by connected clients are reset. The client must re-enable these when it next creates the new association to the IED.

7.5.10 IEC 61850 CONFIGURATION

You cannot configure the device for IEC 61850 edition 1 using the HMI panel on the product. For this you must use the IEC 61850 Configurator, which is part of the settings application software. If the device is compatible with edition 2, however, you can configure it with the HMI. To configure IEC61850 edition 2 using the HMI, you must first enable the IP From HMI setting, after which you can set the media (copper or fibre), IP address, subnet mask and gateway address.

IEC 61850 allows IEDs to be directly configured from a configuration file. The IED's system configuration capabilities are determined from an IED Capability Description file (ICD), supplied with the product. By using ICD files from the products to be installed, you can design, configure and test (using simulation tools), a substation's entire protection scheme before the products are installed into the substation.

To help with this process, the settings application software provides an IEC 61850 Configurator tool, which allows the pre-configured IEC 61850 configuration file to be imported and transferred to the IED. As well as this, you can manually create configuration files for all products, based on their original IED capability description (ICD file).

Other features include:

- The extraction of configuration data for viewing and editing.
- A sophisticated error checking sequence to validate the configuration data before sending to the IED.

Note:

Some configuration data is available in the IEC61850 CONFIG. column, allowing read-only access to basic configuration data.

7.5.10.1 IEC 61850 CONFIGURATION BANKS

There are two configuration banks:

- Active Configuration Bank
- Inactive Configuration Bank

Any new configuration sent to the IED is automatically stored in the inactive configuration bank, therefore not immediately affecting the current configuration.

Following an upgrade, the IEC 61850 Configurator tool can be used to transmit a command, which authorises activation of the new configuration contained in the inactive configuration bank. This is done by switching the active and inactive configuration banks. The capability of switching the configuration banks is also available using the *IEC61850 CONFIG*, column of the HMI.

The SCL Name and Revision attributes of both configuration banks are available in the *IEC61850 CONFIG.* column of the HMI.

7.5.10.2 IEC 61850 NETWORK CONNECTIVITY

Configuration of the IP parameters and SNTP (Simple Network Time Protocol) time synchronisation parameters is performed by the IEC 61850 Configurator tool. If these parameters are not available using an SCL (Substation Configuration Language) file, they must be configured manually.

Every IP address on the Local Area Network must be unique. Duplicate IP addresses result in conflict and must be avoided. Most IEDs check for a conflict on every IP configuration change and at power up and they raise an alarm if an IP conflict is detected.

The IED can be configured to accept data from other networks using the *Gateway* setting. If multiple networks are used, the IP addresses must be unique across networks.

8 READ ONLY MODE

With IEC 61850 and Ethernet/Internet communication capabilities, security has become an important issue. For this reason, all relevant General Electric IEDs have been adapted to comply with the latest cyber-security standards.

In addition to this, a facility is provided which allows you to enable or disable the communication interfaces. This feature is available for products using Courier, IEC 60870-5-103, or IEC 61850.

8.1 IEC 60870-5-103 PROTOCOL BLOCKING

If Read-Only Mode is enabled for RP1 or RP2 with IEC 60870-5-103, the following commands are blocked at the interface:

- Write parameters (=change setting) (private ASDUs)
- General Commands (ASDU20), namely:
 - o INF16 auto-recloser on/off
 - INF19 LED reset
 - Private INFs (for example: CB open/close, Control Inputs)

The following commands are still allowed:

- Poll Class 1 (Read spontaneous events)
- Poll Class 2 (Read measurands)
- GI sequence (ASDU7 'Start GI', Poll Class 1)
- Transmission of Disturbance Records sequence (ASDU24, ASDU25, Poll Class 1)
- Time Synchronisation (ASDU6)
- General Commands (ASDU20), namely:
 - INF23 activate characteristic 1
 - INF24 activate characteristic 2
 - INF25 activate characteristic 3
 - INF26 activate characteristic 4

Note.

For IEC 60870-5-103, Read Only Mode function is different from the existing Command block feature.

8.2 COURIER PROTOCOL BLOCKING

If Read-Only Mode is enabled for RP1 or RP2 with Courier, the following commands are blocked at the interface:

- Write settings
- All controls, including:Reset Indication (Trip LED)
 - Operate Control Inputs
 - CB operations
 - Auto-reclose operations
 - Reset demands
 - Clear event/fault/maintenance/disturbance records
 - Test LEDs & contacts

The following commands are still allowed:

- Read settings, statuses, measurands
- Read records (event, fault, disturbance)
- Time Synchronisation
- Change active setting group

8.3 IEC 61850 PROTOCOL BLOCKING

If Read-Only Mode is enabled for the Ethernet interfacing with IEC 61850, the following commands are blocked at the interface:

- All controls, including:
 - Enable/disable protection
 - Operate Control Inputs
 - CB operations (Close/Trip, Lock)
 - Reset LEDs

The following commands are still allowed:

- Read statuses, measurands
- Generate reports
- Extract disturbance records
- Time synchronisation
- Change active setting group

8.4 READ-ONLY SETTINGS

The following settings are available for enabling or disabling Read Only Mode.

- RP1 Read Only
- RP2 Read Only (only for products that have RP2)
- NIC Read Only (where Ethernet is available)

8.5 READ-ONLY DDB SIGNALS

The remote read only mode is also available in the PSL using three dedicated DDB signals:

- RP1 Read Only
- RP2 Read Only (only for products that have RP2)
- NIC Read Only (where Ethernet is available)

Using the PSL, these signals can be activated by opto-inputs, Control Inputs and function keys if required.

9 TIME SYNCHRONISATION

In modern protection schemes it is necessary to synchronise the IED's real time clock so that events from different devices can be time stamped and placed in chronological order. This is achieved in various ways depending on the chosen options and communication protocols.

- Using the IRIG-B input (if fitted)
- Using the SNTP time protocol (for Ethernet IEC 61850 versions + DNP3 OE)
- By using the time synchronisation functionality inherent in the data protocols

9.1 DEMODULATED IRIG-B

IRIG stands for Inter Range Instrumentation Group, which is a standards body responsible for standardising different time code formats. There are several different formats starting with IRIG-A, followed by IRIG-B and so on. The letter after the "IRIG" specifies the resolution of the time signal in pulses per second (PPS). IRIG-B, the one which we use has a resolution of 100 PPS. IRIG-B is used when accurate time-stamping is required.

The following diagram shows a typical GPS time-synchronised substation application. The satellite RF signal is picked up by a satellite dish and passed on to receiver. The receiver receives the signal and converts it into time signal suitable for the substation network. IEDs in the substation use this signal to govern their internal clocks and event recorders.

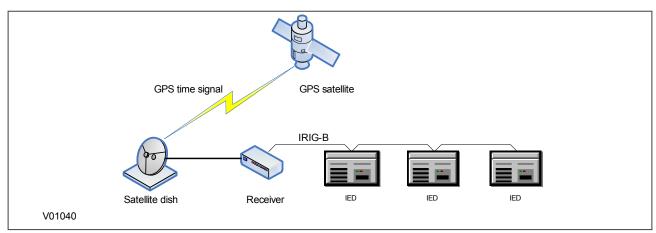


Figure 221: GPS Satellite timing signal

The IRIG-B time code signal is a sequence of one second time frames. Each frame is split up into ten 100 mS slots as follows:

- Time-slot 1: Seconds
- Time-slot 2: Minutes
- Time-slot 3: Hours
- Time-slot 4: Davs
- Time-slot 5 and 6: Control functions
- Time-slots 7 to 10: Straight binary time of day

The first four time-slots define the time in BCD (Binary Coded Decimal). Time-slots 5 and 6 are used for control functions, which control deletion commands and allow different data groupings within the synchronisation strings. Time-slots 7-10 define the time in SBS (Straight Binary Second of day).

9.1.1 IRIG-B IMPLEMENTATION

Depending on the chosen hardware options, the product can be equipped with an IRIG-B input for time synchronisation purposes. The IRIG-B interface is implemented either on a dedicated card, or together with other

communication functionality such as Ethernet. The IRIG-B connection is presented by a connector is a BNC connector. IRIG-B signals are usually presented as an RF-modulated signal. There are two types of input to our IRIG-B boards: demodulated or modulated. A board that accepts a demodulated input is used where the IRIG-B signal has already been demodulated by another device before being fed to the IED. A board that accepts a modulated input has an on-board demodulator.

To set the device to use IRIG-B, use the setting IRIG-B Sync cell in the DATE AND TIME column.

The IRIG-B status can be viewed in the IRIG-B Status cell in the DATE AND TIME column.

9.2 SNTP

SNTP is used to synchronise the clocks of computer systems over packet-switched, variable-latency data networks, such as IP. SNTP can be used as the time synchronisation method for models using IEC 61850 over Ethernet.

The device is synchronised by the main SNTP server. This is achieved by entering the IP address of the SNTP server into the IED using the IEC 61850 Configurator software described in the settings application software manual. A second server is also configured with a different IP address for backup purposes.

This function issues an alarm when there is a loss of time synchronisation on the SNTP server. This could be because there is no response or no valid clock signal.

The HMI menu does not contain any configurable settings relating to SNTP, as the only way to configure it is using the IEC 61850 Configurator. However it is possible to view some parameters in the *COMMUNICATIONS* column under the sub-heading SNTP parameters. Here you can view the SNTP server addresses and the SNTP poll rate in the cells *SNTP Server 1*, *SNTP Server 2* and *SNTP Poll rate* respectively.

The SNTP time synchronisation status is displayed in the SNTP Status cell in the DATE AND TIME column.

9.2.1 LOSS OF SNTP SERVER SIGNAL ALARM

This function issues an alarm when there is a loss of time synchronization on the SNTP server. It is issued when the SNTP sever has not detected a valid time synchronisation response within its 5 second window. This is because there is no response or no valid clock. The alarm is mapped to IEC 61850.

9.3 IEEE 1588 PRECISION TIME PROTOCOL

The MiCOM P40 modular products support the IEEE C37.238 (Power Profile) of IEEE 1588 Precision Time Protocol (PTP) as a slave-only clock. This can be used to replace or supplement IRIG-B and SNTP time synchronisation so that the IED can be synchronised using Ethernet messages from the substation LAN without any additional physical connections being required.

A dedicated DDB signal (PTP Failure) his provided to indicate failure of failure of PTP.

9.3.1 ACCURACY AND DELAY CALCULATION

A time synchronisation accuracy of within 5 ms is possible. Both peer-to-peer or end-to-end mode delay measurement can be used.

In peer-to-peer mode, delays are measured between each link in the network and are compensated for. This provides greater accuracy, but requires that every device between the Grand Master and Slaves supports the peer-to-peer delay measurement.

In end-to-end mode, delays are only measured between each Grand Master and Slave. The advantage of this mode is that the requirements for the switches on the network are lower; they do not need to independently calculate delays. The main disadvantage is that more inaccuracy is introduced, because the method assumes that forward and reverse delays are always the same, which may not always be correct.

When using end-to-end mode, the IED can be connected in a ring or line topology using RSTP or Self Healing Protocol without any additional Transparent Clocks. But because the IED is a slave-only device, additional inaccuracy is introduced. The additional error will be less than 1ms for a network of eight devices.

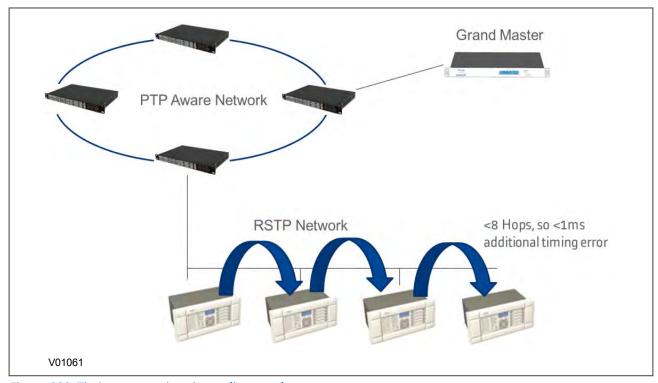


Figure 222: Timing error using ring or line topology

9.3.2 PTP DOMAINS

PTP traffic can be segregated into different domains using Boundary Clocks. These allow different PTP clocks to share the same network while maintaining independent synchronisation within each grouped set.

9.4 TIME SYNCHRONSIATION USING THE COMMUNICATION PROTOCOLS

All communication protocols have in-built time synchronisation mechanisms. If an external time synchronisation mechanism such as IRIG-B, SNTP, or IEEE 1588 PTP is not used to synchronise the devices, the time synchronisation mechanism within the relevant serial protocol is used. The real time is usually defined in the master station and communicated to the relevant IEDs via one of the rear serial ports using the chosen protocol. It is also possible to define the time locally using settings in the *DATE AND TIME* column.

The time synchronisation for each protocol is described in the relevant protocol description section.

CHAPTER 19

CYBER-SECURITY

1 OVERVIEW

In the past, substation networks were traditionally isolated and the protocols and data formats used to transfer information between devices were often proprietary.

For these reasons, the substation environment was very secure against cyber-attacks. The terms used for this inherent type of security are:

- Security by isolation (if the substation network is not connected to the outside world, it cannot be accessed from the outside world).
- Security by obscurity (if the formats and protocols are proprietary, it is very difficult to interpret them).

The increasing sophistication of protection schemes, coupled with the advancement of technology and the desire for vendor interoperability, has resulted in standardisation of networks and data interchange within substations. Today, devices within substations use standardised protocols for communication. Furthermore, substations can be interconnected with open networks, such as the internet or corporate-wide networks, which use standardised protocols for communication. This introduces a major security risk making the grid vulnerable to cyber-attacks, which could in turn lead to major electrical outages.

Clearly, there is now a need to secure communication and equipment within substation environments. This chapter describes the security measures that have been put in place for our range of Intelligent Electronic Devices (IEDs).

Note:

Cyber-security compatible devices do not enforce NERC compliance, they merely facilitate it. It is the responsibility of the user to ensure that compliance is adhered to as and when necessary.

This chapter contains the following sections:

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2 THE NEED FOR CYBER-SECURITY

Cyber-security provides protection against unauthorised disclosure, transfer, modification, or destruction of information or information systems, whether accidental or intentional. To achieve this, there are several security requirements:

- Confidentiality (preventing unauthorised access to information)
- Integrity (preventing unauthorised modification)
- Availability / Authentication (preventing the denial of service and assuring authorised access to information)
- Non-repudiation (preventing the denial of an action that took place)
- Traceability / Detection (monitoring and logging of activity to detect intrusion and analyse incidents)

The threats to cyber-security may be unintentional (e.g. natural disasters, human error), or intentional (e.g. cyber-attacks by hackers).

Good cyber-security can be achieved with a range of measures, such as closing down vulnerability loopholes, implementing adequate security processes and procedures and providing technology to help achieve this.

Examples of vulnerabilities are:

- Indiscretions by personnel (users keep passwords on their computer)
- Bad practice (users do not change default passwords, or everyone uses the same password to access all substation equipment)
- Bypassing of controls (users turn off security measures)
- Inadequate technology (substation is not firewalled)

Examples of availability issues are:

- Equipment overload, resulting in reduced or no performance
- Expiry of a certificate preventing access to equipment

To help tackle these issues, standards organisations have produced various standards. Compliance with these standards significantly reduces the threats associated with lack of cyber-security.

3 STANDARDS

There are several standards, which apply to substation cyber-security. The standards currently applicable to General Electric IEDs are NERC and IEEE1686.

Standard	Country	Description
NERC CIP (North American Electric Reliability Corporation)	USA	Framework for the protection of the grid critical Cyber Assets
BDEW (German Association of Energy and Water Industries)	Germany	Requirements for Secure Control and Telecommunication Systems
ANSI ISA 99	USA	ICS oriented then Relevant for EPU completing existing standard and identifying new topics such as patch management
IEEE 1686	International	International Standard for substation IED cyber-security capabilities
IEC 62351	International	Power system data and Comm. protocol
ISO/IEC 27002	International	Framework for the protection of the grid critical Cyber Assets
NIST SP800-53 (National Institute of Standards and Technology)	USA	Complete framework for SCADA SP800-82and ICS cyber-security
CPNI Guidelines (Centre for the Protection of National Infrastructure)	UK	Clear and valuable good practices for Process Control and SCADA security

3.1 NERC COMPLIANCE

The North American Electric Reliability Corporation (NERC) created a set of standards for the protection of critical infrastructure. These are known as the CIP standards (Critical Infrastructure Protection). These were introduced to ensure the protection of 'Critical Cyber Assets', which control or have an influence on the reliability of North America's electricity generation and distribution systems.

These standards have been compulsory in the USA for several years now. Compliance auditing started in June 2007, and utilities face extremely heavy fines for non-compliance.

NERC CIP standards

CIP standard	Description
CIP-002-1 Critical Cyber Assets	Define and document the Critical Assets and the Critical Cyber Assets
CIP-003-1 Security Management Controls	Define and document the Security Management Controls required to protect the Critical Cyber Assets
CIP-004-1 Personnel and Training	Define and Document Personnel handling and training required protecting Critical Cyber Assets
CIP-005-1 Electronic Security	Define and document logical security perimeters where Critical Cyber Assets reside. Define and document measures to control access points and monitor electronic access
CIP-006-1 Physical Security	Define and document Physical Security Perimeters within which Critical Cyber Assets reside
CIP-007-1 Systems Security Management	Define and document system test procedures, account and password management, security patch management, system vulnerability, system logging, change control and configuration required for all Critical Cyber Assets
CIP-008-1 Incident Reporting and Response Planning	Define and document procedures necessary when Cyber-security Incidents relating to Critical Cyber Assets are identified
CIP-009-1 Recovery Plans	Define and document Recovery plans for Critical Cyber Assets

3.1.1 CIP 002

CIP 002 concerns itself with the identification of:

- Critical assets, such as overhead lines and transformers
- Critical cyber assets, such as IEDs that use routable protocols to communicate outside or inside the Electronic Security Perimeter; or are accessible by dial-up

Power utility responsibilities:	General Electric's contribution:
I CROTE THE LIST OF THE ASSETS	We can help the power utilities to create this asset register automatically. We can provide audits to list the Cyber assets

3.1.2 CIP 003

CIP 003 requires the implementation of a cyber-security policy, with associated documentation, which demonstrates the management's commitment and ability to secure its Critical Cyber Assets.

The standard also requires change control practices whereby all entity or vendor-related changes to hardware and software components are documented and maintained.

Power utility responsibilities:	General Electric's contribution:
To create a Cyber-security Policy	We can help the power utilities to have access control to its critical assets by providing centralized Access control. We can help the customer with its change control by providing a section in the documentation where it describes changes affecting the hardware and software.

3.1.3 CIP 004

CIP 004 requires that personnel with authorized cyber access or authorized physical access to Critical Cyber Assets, (including contractors and service vendors), have an appropriate level of training.

Power utility responsibilities:	General Electric's contribution:
To provide appropriate training of its personnel	We can provide cyber-security training

3.1.4 CIP 005

CIP 005 requires the establishment of an Electronic Security Perimeter (ESP), which provides:

- The disabling of ports and services that are not required
- Permanent monitoring and access to logs (24x7x365)
- Vulnerability Assessments (yearly at a minimum)
- Documentation of Network Changes

Power utility responsibilities:	General Electric's contribution:
To monitor access to the ESP To perform the vulnerability assessments To document network changes	To disable all ports not used in the IED To monitor and record all access to the IED

3.1.5 CIP 006

CIP 006 states that Physical Security controls, providing perimeter monitoring and logging along with robust access controls, must be implemented and documented. All cyber assets used for Physical Security are considered critical and should be treated as such:

Power utility responsibilities:	General Electric's contribution:
Provide physical security controls and perimeter monitoring. Ensure that people who have access to critical cyber assets don't have criminal records.	General Electric cannot provide additional help with this aspect.

3.1.6 CIP 007

CIP 007 covers the following points:

- Test procedures
- Ports and services
- Security patch management
- Antivirus
- Account management
- Monitoring
- An annual vulnerability assessment should be performed

Power utility responsibilities:	General Electric's contribution:
To provide an incident response team and have appropriate processes in place	Test procedures, we can provide advice and help on testing. Ports and services, our devices can disable unused ports and services Security patch management, we can provide assistance Antivirus, we can provide advise and assistance Account management, we can provide advice and assistance Monitoring, our equipment monitors and logs access

3.1.7 CIP 008

CIP 008 requires that an incident response plan be developed, including the definition of an incident response team, their responsibilities and associated procedures.

Power utility responsibilities:	General Electric's contribution:
To provide an incident response team and have appropriate processes in place.	General Electric cannot provide additional help with this aspect.

3.1.8 CIP 009

CIP 009 states that a disaster recovery plan should be created and tested with annual drills.

Power utility responsibilities:	General Electric's contribution:	
TO implement a recovery plan	To provide guidelines on recovery plans and backup/restore documentation	

3.2 IEEE 1686-2007

IEEE 1686-2007 is an IEEE Standard for substation IEDs' cyber-security capabilities. It proposes practical and achievable mechanisms to achieve secure operations.

The following features described in this standard apply:

- Passwords are 8 characters long and can contain upper-case, lower-case, numeric and special characters.
- Passwords are never displayed or transmitted to a user.

- IED functions and features are assigned to different password levels. The assignment is fixed.
- The audit trail is recorded, listing events in the order in which they occur, held in a circular buffer.
- Records contain all defined fields from the standard and record all defined function event types where the function is supported.
- No password defeat mechanism exists. Instead a secure recovery password scheme is implemented.
- Unused ports (physical and logical) may be disabled.

4 CYBER-SECURITY IMPLEMENTATION

The General Electric IEDs have always been and will continue to be equipped with state-of-the-art security measures. Due to the ever-evolving communication technology and new threats to security, this requirement is not static. Hardware and software security measures are continuously being developed and implemented to mitigate the associated threats and risks.

This section describes the current implementation of cyber-security. This is valid for the release of platform software to which this manual pertains. This current cyber-security implementation is known as Cyber-security Phase 1.

At the IED level, these cyber-security measures have been implemented:

- NERC-compliant default display
- Four-level access
- Enhanced password security
- Password recovery procedure
- Disabling of unused physical and logical ports
- Inactivity timer
- Security events management

External to the IEDs, the following cyber-security measures have been implemented:

- Antivirus
- Security patch management

4.1 NERC-COMPLIANT DISPLAY

For the device to be NERC-compliant, it must provide the option for a NERC-compliant default display. The default display that is implemented in our cyber-security concept contains a warning that the IED can be accessed by authorised users. You can change this if required with the *User Banner* setting in the *SECURITY CONFIG* column.

ACCESS ONLY FOR AUTHORISED USERS HOWKEY

If you try to change the default display from the NERC-compliant one, a further warning is displayed:

DISPLAY NOT NERC COMPLIANT OK?

The default display navigation map shows how NERC-compliance is achieved with the product's default display concept.

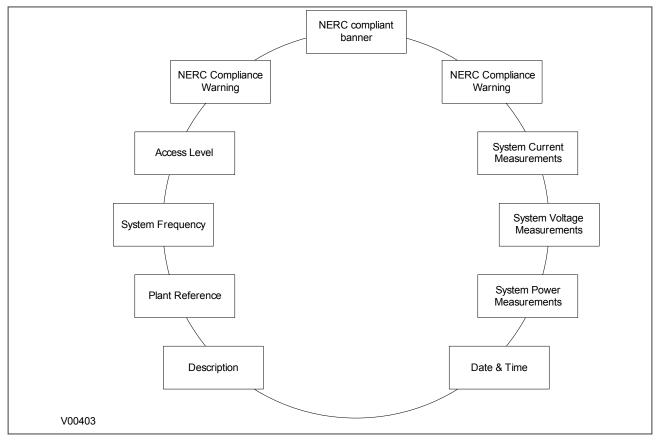


Figure 223: Default display navigation

4.2 FOUR-LEVEL ACCESS

The menu structure contains four levels of access, three of which are password protected.

Password levels

Level	Meaning	Read Operation	Write Operation
0	Read Some Write Minimal	SYSTEM DATA column: Description Plant Reference Model Number Serial Number S/W Ref. Access Level Security Feature SECURITY CONFIG column: User Banner Attempts Remain Blk Time Remain Fallback PW level Security Code (UI only)	Password Entry LCD Contrast (UI only)
1	Read All Write Few	All data and settings are readable. Poll Measurements	All items writeable at level 0. Level 1 Password setting Extract Disturbance Record Select Event, Main and Fault (upload) Extract Events (e.g. via MiCOM S1 Studio)

Level	Meaning	Read Operation	Write Operation	
2	Read All Write Some	All data and settings are readable. Poll Measurements	All items writeable at level 1. Setting Cells that change visibility (Visible/Invisible). Setting Values (Primary/Secondary) selector Commands: Reset Indication Reset Demand Reset Statistics Reset CB Data / counters Level 2 Password setting	
3	Read All Write All	All data and settings are readable. Poll Measurements	All items writeable at level 2. Change all Setting cells Operations: Extract and download Setting file. Extract and download PSL Extract and download MCL61850 (IEC61850 CONFIG) Auto-extraction of Disturbance Recorder Courier/Modbus Accept Event (auto event extraction, e.g. via A2R) Commands: Change Active Group setting Close / Open CB Change Comms device address. Set Date & Time Switch MCL banks / Switch Conf. Bank in UI (IEC61850 CONFIG) Enable / Disable Device ports (in SECURITY CONFIG column) Level 3 password setting	

4.2.1 BLANK PASSWORDS

A blank password is effectively a zero-length password. Through the front panel it is entered by confirming the password entry without actually entering any password characters. Through a communications port the Courier and Modbus protocols each have a means of writing a blank password to the IED. A blank password disables the need for a password at the level that this password is applied.

Blank passwords have a slightly different validation procedure. If a blank password is entered through the front panel, the following text is displayed, after which the procedure is the same as already described:

BLANK PASSWORD ENTERED CONFIRM

Blank passwords cannot be configured if the lower level password is not blank.

Blank passwords affect the fall back level after inactivity timeout or logout.

The 'fallback level' is the password level adopted by the IED after an inactivity timeout, or after the user logs out. This will be either the level of the highest-level password that is blank, or level 0 if no passwords are blank.

4.2.2 PASSWORD RULES

- Default passwords are blank for Level 1 and are AAAA for Levels 2 and 3
- Passwords may be any length between 0 and 8 characters long
- Passwords may or may not be NERC compliant
- Passwords may contain any ASCII character in the range ASCII code 33 (21 Hex) to ASCII code 122 (7A Hex) inclusive
- Only one password is required for all the IED interfaces

4.2.3 ACCESS LEVEL DDBS

The 'Access level' cell is in the 'System data' column (address 00D0). Also the current level of access for each interface is available for use in the Programming Scheme Logic (PSL) by mapping to these Digital Data Bus (DDB) signals:

- HMI Access Lvl 1
- HMI Access Lvl 2
- FPort AccessLvl1
- FPort AccessLvl2
- RPrt1 AccessLvl1
- RPrt1 AccessLvl2
- RPrt2 AccessLvl1
- RPrt2 AccessLvl2

Each pair of DDB signals indicates the access level as follows:

- Level 1 off, Level 2 off = 0
- Level 1 on, Level 2 off = 1
- Level 1 off, Level 2 on = 2
- Level 1 on, Level 2 on = 3

Key:

HMI = Human Machine Interface

FPort = Front Port

RPrt = Rear Port

Lvl = Level

4.3 ENHANCED PASSWORD SECURITY

Cyber-security requires strong passwords and validation for NERC compliance.

4.3.1 PASSWORD STRENGTHENING

NERC compliant passwords have the following requirements:

- At least one upper-case alpha character
- At least one lower-case alpha character
- At least one numeric character
- At least one special character (%,\$...)
- At least six characters long

4.3.2 PASSWORD VALIDATION

The IED checks for NERC compliance. If the password is entered through the front panel, this is briefly displayed on the LCD.

If the entered password is NERC compliant, the following text is displayed.

NERC COMPLIANT
P/WORD WAS SAVED

If the password entered is not NERC-compliant, the user is required to actively confirm this, in which case the non-compliance is logged.

If the entered password is not NERC compliant, the following text is displayed:

NERC COMPLIANCE NOT MET CONFIRM?

On confirmation, the non-compliant password is stored and the following acknowledgement message is displayed for 2 seconds.

NON-NERC P/WORD SAVED OK

If the action is cancelled, the password is rejected and the following message is displayed for 2 seconds.

NON-NERC P/WORD NOT SAVE

If the password is entered through a communications port using Courier or Modbus protocols, the device will store the password, irrespective of whether it is NERC-compliant or not. It then uses appropriate response codes to inform the client of the NERC-compliancy status. You can then choose to enter a new NERC-compliant password or accept the non-NERC compliant password just entered.

4.3.3 PASSWORD BLOCKING

You are locked out temporarily, after a defined number of failed password entry attempts. Each invalid password entry attempt decrements the 'Attempts Remain' data cell by 1. When the maximum number of attempts has been reached, access is blocked. If the attempts timer expires, or the correct password is entered *before* the 'attempt count' reaches the maximum number, then the 'attempts count' is reset to 0.

An attempt is only counted if the attempted password uses only characters in the valid range, but the attempted password is not correct (does not match the corresponding password in the IED). Any attempt where one or more characters of the attempted password are not in the valid range will not be counted.

Once the password entry is blocked, a 'blocking timer' is started. Attempts to access the interface while the 'blocking timer' is running results in an error message, irrespective of whether the correct password is entered or not. Once the 'blocking timer' has expired, access to the interface is unblocked and the attempts counter is reset to zero.

If you try to enter the password while the interface is blocked, the following message is displayed for 2 seconds.

NOT ACCEPTED ENTRY IS BLOCKED

A similar response occurs if you try to enter the password through a communications port.

The parameters can then be configured using the **Attempts Limit**, **Attempts Timer** and **Blocking Timer** settings in the SECURITY CONFIG column.

Password blocking configuration

Setting	Cell col row	Units	Default Setting	Available Setting
Attempts Limit	25 02		3	0 to 3 step 1
Attempts Timer	25 03	Minutes	2	1 to 3 step 1
Blocking Timer	25 04	Minutes	5	1 to 30 step 1

4.4 PASSWORD RECOVERY

If you mislay a device's password, they can be recovered. To obtain the recovery password you must contact the Contact Centre and supply the Serial Number and its Security Code. The Contact Centre will use these items to generate a Recovery Password.

The security code is a 16-character string of upper case characters. It is a read-only parameter. The device generates its own security code randomly. A new code is generated under the following conditions:

- On power up
- Whenever settings are set back to default
- On expiry of validity timer (see below)
- When the recovery password is entered

As soon as the security code is displayed on the LCD, a validity timer is started. This validity timer is set to 72 hours and is not configurable. This provides enough time for the contact centre to manually generate and send a recovery password. The Service Level Agreement (SLA) for recovery password generation is one working day, so 72 hours is sufficient time, even allowing for closure of the contact centre over weekends and bank holidays.

To prevent accidental reading of the IED security code, the cell will initially display a warning message:

PRESS ENTER TO READ SEC. CODE

The security code is displayed on confirmation. The validity timer is then started. The security code can only be read from the front panel.

4.4.1 ENTRY OF THE RECOVERY PASSWORD

The recovery password is intended for recovery only. It is not a replacement password that can be used continually. It can only be used once – for password recovery.

Entry of the recovery password causes the IED to reset all passwords back to default. This is all it is designed to do. After the passwords have been set back to default, it is up to the user to enter new passwords. Each password should be appropriate for its intended function, ensuring NERC compliance, if required.

On this action, the following message is displayed:

PASSWORDS HAVE BEEN SET TO DEFAULT

The recovery password can be applied through any interface, local or remote. It will achieve the same result irrespective of which interface it is applied through.

4.4.2 PASSWORD ENCRYPTION

The IED supports encryption for passwords entered remotely. The encryption key can be read from the IED through a specific cell available only through communication interfaces, not the front panel. Each time the key is read the IED generates a new key that is valid only for the next password encryption write. Once used, the key is invalidated and a new key must be read for the next encrypted password write. The encryption mechanism is otherwise transparent to the user.

4.5 DISABLING PHYSICAL PORTS

It is possible to disable unused physical ports. A level 3 password is needed to perform this action.

To prevent accidental disabling of a port, a warning message is displayed according to whichever port is required to be disabled. For example if rear port 1 is to be disabled, the following message appears:

REAR PORT 1 TO BE DISABLED.CONFIRM

The following ports can be disabled, depending on the model.

- Front port (Front Port setting)
- Rear port 1 (Rear Port 1 setting)
- Rear port 2 (Rear Port 2 setting)
- Ethernet port (*Ethernet* setting)

Note:

It is not possible to disable a port from which the disabling port command originates.

Note:

We do not generally advise disabling the physical Ethernet port.

4.6 DISABLING LOGICAL PORTS

It is possible to disable unused logical ports. A level 3 password is needed to perform this action.

Note:

The port disabling setting cells are not provided in the settings file. It is only possible to do this using the HMI front panel.

The following protocols can be disabled:

- IEC 61850 (*IEC61850* setting)
- DNP3 Over Ethernet (**DNP3 OE** setting)
- Courier Tunnelling (Courier Tunnel setting)

Note:

If any of these protocols are enabled or disabled, the Ethernet card will reboot.

4.7 SECURITY EVENTS MANAGEMENT

To implement NERC-compliant cyber-security, a range of Event records need to be generated. These log security issues such as the entry of a non-NERC-compliant password, or the selection of a non-NERC-compliant default display.

Security event values

Event Value	Display
PASSWORD LEVEL UNLOCKED	USER LOGGED IN ON {int} LEVEL {n}
PASSWORD LEVEL RESET	USER LOGGED OUT ON {int} LEVEL {n}
PASSWORD SET BLANK	P/WORD SET BLANK BY {int} LEVEL {p}
PASSWORD SET NON-COMPLIANT	P/WORD NOT-NERC BY {int} LEVEL {p}
PASSWORD MODIFIED	PASSWORD CHANGED BY {int} LEVEL {p}
PASSWORD ENTRY BLOCKED	PASSWORD BLOCKED ON {int}
PASSWORD ENTRY UNBLOCKED	P/WORD UNBLOCKED ON {int}
INVALID PASSWORD ENTERED	INV P/W ENTERED ON <int}< td=""></int}<>
PASSWORD EXPIRED	P/WORD EXPIRED ON {int}
PASSWORD ENTERED WHILE BLOCKED	P/W ENT WHEN BLK ON {int}
RECOVERY PASSWORD ENTERED	RCVY P/W ENTERED ON {int}
IED SECURITY CODE READ	IED SEC CODE RD ON {int}
IED SECURITY CODE TIMER EXPIRED	IED SEC CODE EXP
PORT DISABLED	PORT DISABLED BY {int} PORT {prt}
PORT ENABLED	PORT ENABLED BY {int} PORT {prt}
DEF. DISPLAY NOT NERC COMPLIANT	DEF DSP NOT-NERC
PSL SETTINGS DOWNLOADED	PSL STNG D/LOAD BY {int} GROUP {grp}

Event Value	Display
DNP SETTINGS DOWNLOADED	DNP STNG D/LOAD BY {int}
TRACE DATA DOWNLOADED	TRACE DAT D/LOAD BY {int}
IEC61850 CONFIG DOWNLOADED	IED CONFG D/LOAD BY {int}
USER CURVES DOWNLOADED	USER CRV D/LOAD BY {int} GROUP {crv}
PSL CONFIG DOWNLOADED	PSL CONFG D/LOAD BY {int} GROUP {grp}
SETTINGS DOWNLOADED	SETTINGS D/LOAD BY {int} GROUP {grp}
PSL SETTINGS UPLOADED	PSL STNG UPLOAD BY {int} GROUP {grp}
DNP SETTINGS UPLOADED	DNP STNG UPLOAD BY {int}
TRACE DATA UPLOADED	TRACE DAT UPLOAD BY {int}
IEC61850 CONFIG UPLOADED	IED CONFG UPLOAD BY {int}
USER CURVES UPLOADED	USER CRV UPLOAD BY {int} GROUP {crv}
PSL CONFIG UPLOADED	PSL CONFG UPLOAD BY {int} GROUP {grp}
SETTINGS UPLOADED	SETTINGS UPLOAD BY {int} GROUP {grp}
EVENTS HAVE BEEN EXTRACTED	EVENTS EXTRACTED BY {int} {nov} EVNTS
ACTIVE GROUP CHANGED	ACTIVE GRP CHNGE BY {int} GROUP {grp}
CS SETTINGS CHANGED	C & S CHANGED BY {int}
DR SETTINGS CHANGED	DR CHANGED BY {int}
SETTING GROUP CHANGED	SETTINGS CHANGED BY {int} GROUP {grp}
POWER ON	POWER ON -
SOFTWARE_DOWNLOADED	S/W DOWNLOADED -

where:

- int is the interface definition (UI, FP, RP1, RP2, TNL, TCP)
- prt is the port ID (FP, RP1, RP2, TNL, DNP3, IEC, ETHR)
- grp is the group number (1, 2, 3, 4)

- crv is the Curve group number (1, 2, 3, 4)
- n is the new access level (0, 1, 2, 3)
- p is the password level (1, 2, 3)
- nov is the number of events (1 nnn)

Each new event has an incremented unique number, therefore missing events appear as 'gap' in the sequence. The unique identifier forms part of the event record that is read or uploaded from the IED.

Note

It is no longer possible to clear Event, Fault, Maintenance, and Disturbance Records.

4.8 LOGGING OUT

If you have been configuring the IED, you should 'log out'. Do this by going up to the top of the menu tree. When you are at the Column Heading level and you press the Up button, you may be prompted to log out with the following display:

DO YOU WANT TO LOG OUT?

You will only be asked this question if your password level is higher than the fallback level.

If you confirm, the following message is displayed for 2 seconds:

LOGGED OUT Access Level #

Where # is the current fallback level.

If you decide not to log out, the following message is displayed for 2 seconds.

LOGOUT CANCELLED Access Level #

where # is the current access level

CHAPTER 20

INSTALLATION

Chapter 20 - Installation P14x

1 CHAPTER OVERVIEW

This chapter provides information about installing the product.

This chapter contains the following sections:

Chapter Overview	479
Handling the Goods	480
Mounting the Device	481
Cables and Connectors	484
Case Dimensions	488

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2 HANDLING THE GOODS

Our products are of robust construction but require careful treatment before installation on site. This section discusses the requirements for receiving and unpacking the goods, as well as associated considerations regarding product care and personal safety.



Caution:

Before lifting or moving the equipment you should be familiar with the Safety Information chapter of this manual.

2.1 RECEIPT OF THE GOODS

On receipt, ensure the correct product has been delivered. Unpack the product immediately to ensure there has been no external damage in transit. If the product has been damaged, make a claim to the transport contractor and notify us promptly.

For products not intended for immediate installation, repack them in their original delivery packaging.

2.2 UNPACKING THE GOODS

When unpacking and installing the product, take care not to damage any of the parts and make sure that additional components are not accidentally left in the packing or lost. Do not discard any CDROMs or technical documentation. These should accompany the unit to its destination substation and put in a dedicated place.

The site should be well lit to aid inspection, clean, dry and reasonably free from dust and excessive vibration. This particularly applies where installation is being carried out at the same time as construction work.

2.3 STORING THE GOODS

If the unit is not installed immediately, store it in a place free from dust and moisture in its original packaging. Keep any de-humidifier bags included in the packing. The de-humidifier crystals lose their efficiency if the bag is exposed to ambient conditions. Restore the crystals before replacing it in the carton. Ideally regeneration should be carried out in a ventilating, circulating oven at about 115°C. Bags should be placed on flat racks and spaced to allow circulation around them. The time taken for regeneration will depend on the size of the bag. If a ventilating, circulating oven is not available, when using an ordinary oven, open the door on a regular basis to let out the steam given off by the regenerating silica gel.

On subsequent unpacking, make sure that any dust on the carton does not fall inside. Avoid storing in locations of high humidity. In locations of high humidity the packaging may become impregnated with moisture and the dehumidifier crystals will lose their efficiency.

The device can be stored between -25° to $+70^{\circ}$ C for unlimited periods or between -40° C to $+85^{\circ}$ C for up to 96 hours (see technical specifications).

2.4 DISMANTLING THE GOODS

If you need to dismantle the device, always observe standard ESD (Electrostatic Discharge) precautions. The minimum precautions to be followed are as follows:

- Use an antistatic wrist band earthed to a suitable earthing point.
- Avoid touching the electronic components and PCBs.

3 MOUNTING THE DEVICE

The products are dispatched either individually or as part of a panel or rack assembly.

Individual products are normally supplied with an outline diagram showing the dimensions for panel cut-outs and hole centres.

The products are designed so the fixing holes in the mounting flanges are only accessible when the access covers are open.

If you use a P991 or MMLG test block with the product, when viewed from the front, position the test block on the right-hand side of the associated product. This minimises the wiring between the product and test block, and allows the correct test block to be easily identified during commissioning and maintenance tests.

If you need to test the product for correct operation during installation, open the lower access cover, hold the battery in place and pull the red tab to remove the battery isolation strip.

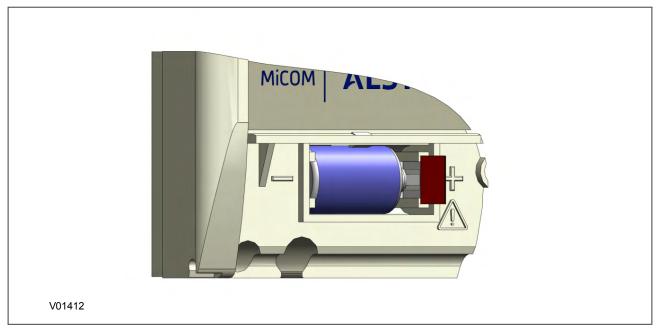


Figure 224: Location of battery isolation strip

3.1 FLUSH PANEL MOUNTING

Panel-mounted devices are flush mounted into panels using M4 SEMS Taptite self-tapping screws with captive 3 mm thick washers (also known as a SEMS unit).



Caution:

Do not use conventional self-tapping screws, because they have larger heads and could damage the faceplate.

Alternatively, you can use tapped holes if the panel has a minimum thickness of 2.5 mm.

For applications where the product needs to be semi-projection or projection mounted, a range of collars are available.

If several products are mounted in a single cut-out in the panel, mechanically group them horizontally or vertically into rigid assemblies before mounting in the panel.

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Caution:

Do not fasten products with pop rivets because this makes them difficult to remove if repair becomes necessary.

3.2 RACK MOUNTING

Panel-mounted variants can also be rack mounted using single-tier rack frames (our part number FX0021 101), as shown in the figure below. These frames are designed with dimensions in accordance with IEC 60297 and are supplied pre-assembled ready to use. On a standard 483 mm (19 inch) rack this enables combinations of case widths up to a total equivalent of size 80TE to be mounted side by side.

The two horizontal rails of the rack frame have holes drilled at approximately 26 mm intervals. Attach the products by their mounting flanges using M4 Taptite self-tapping screws with captive 3 mm thick washers (also known as a SEMS unit).



Caution:

Risk of damage to the front cover molding. Do not use conventional self-tapping screws, including those supplied for mounting MiDOS products because they have slightly larger heads.

Once the tier is complete, the frames are fastened into the racks using mounting angles at each end of the tier.

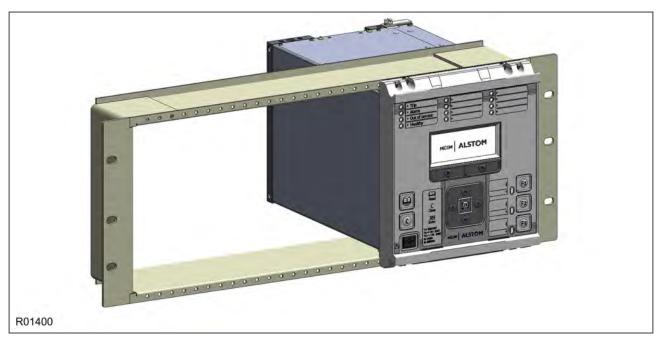


Figure 225: Rack mounting of products

Products can be mechanically grouped into single tier (4U) or multi-tier arrangements using the rack frame. This enables schemes using products from different product ranges to be pre-wired together before mounting.

Use blanking plates to fill any empty spaces. The spaces may be used for installing future products or because the total size is less than 80TE on any tier. Blanking plates can also be used to mount ancillary components. The part numbers are as follows:

Case size summation	Blanking plate part number
STE	GJ2028 101
10TE	GJ2028 102

Case size summation	Blanking plate part number
15TE	GJ2028 103
20TE	GJ2028 104
25TE	GJ2028 105
30TE	GJ2028 106
35TE	GJ2028 107
40TE	GJ2028 108

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4 CABLES AND CONNECTORS

This section describes the type of wiring and connections that should be used when installing the device. For pinout details please refer to the Hardware Design chapter or the wiring diagrams.



Caution:

Before carrying out any work on the equipment you should be familiar with the Safety Section and the ratings on the equipment's rating label.

4.1 TERMINAL BLOCKS

The device may use one or more of the terminal block types shown in the following diagram. The terminal blocks are fastened to the rear panel with screws.

- Heavy duty (HD) terminal blocks for CT and VT circuits
- Medium duty (MD) terminal blocks for the power supply, relay outputs and rear communications port
- MiDOS terminal blocks for CT and VT circuits
- RTD/CLIO terminal block for connection to analogue transducers

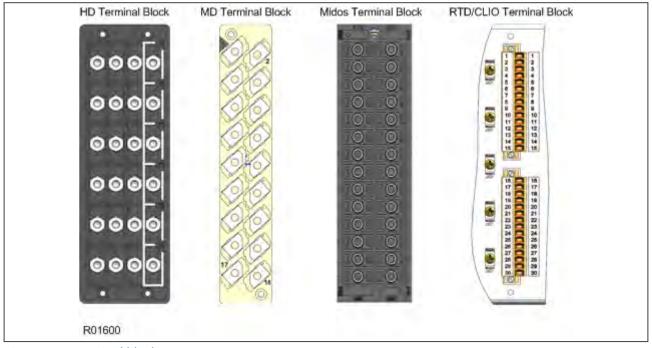


Figure 226: Terminal block types

MiCOM products are supplied with sufficient M4 screws for making connections to the rear mounted terminal blocks using ring terminals, with a recommended maximum of two ring terminals per terminal.

If required, M4 90° crimp ring terminals can be supplied in three different sizes depending on wire size. Each type is available in bags of 100.

Part number	Wire size	Insulation color
ZB9124 901	0.25 - 1.65 mm ² (22 – 16 AWG)	Red
ZB9124 900	1.04 - 2.63 mm ² (16 – 14 AWG)	Blue

4.2 POWER SUPPLY CONNECTIONS

These should be wired with 1.5 mm PVC insulated multi-stranded copper wire terminated with M4 ring terminals. The wire should have a minimum voltage rating of 300 V RMS.



Caution:

Protect the auxiliary power supply wiring with a maximum 16 A high rupture capacity (HRC) type NIT or TIA fuse.

4.3 EARTH CONNNECTION

Every device must be connected to the cubicle earthing bar using the M4 earth terminal.

Use a wire size of at least 2.5 mm^2 terminated with a ring terminal.

Due to the physical limitations of the ring terminal, the maximum wire size you can use is 6.0 mm² using ring terminals that are not pre-insulated. If using pre insulated ring terminals, the maximum wire size is reduced to 2.63 mm² per ring terminal. If you need a greater cross-sectional area, use two wires in parallel, each terminated in a separate ring terminal.

The wire should have a minimum voltage rating of 300 V RMS.

Note:

To prevent any possibility of electrolytic action between brass or copper ground conductors and the rear panel of the product, precautions should be taken to isolate them from one another. This could be achieved in several ways, including placing a nickel-plated or insulating washer between the conductor and the product case, or using tinned ring terminals.

4.4 CURRENT TRANSFORMERS

Current transformers would generally be wired with 2.5 mm² PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

Due to the physical limitations of the ring terminal, the maximum wire size you can use is 6.0 mm² using ring terminals that are not pre-insulated. If using pre insulated ring terminals, the maximum wire size is reduced to 2.63 mm² per ring terminal. If you need a greater cross-sectional area, use two wires in parallel, each terminated in a separate ring terminal.

The wire should have a minimum voltage rating of 300 V RMS.



Caution:

Current transformer circuits must never be fused.

Note:

If there are CTs present, spring-loaded shorting contacts ensure that the terminals into which the CTs connect are shorted before the CT contacts are broken.

Note:

For 5A CT secondaries, we recommend using $2 \times 2.5 \text{ mm}^2$ PVC insulated multi-stranded copper wire.

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4.5 VOLTAGE TRANSFORMER CONNECTIONS

Voltage transformers should be wired with 2.5 mm² PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

The wire should have a minimum voltage rating of 300 V RMS.

4.6 WATCHDOG CONNECTIONS

These should be wired with 1 mm PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

The wire should have a minimum voltage rating of 300 V RMS.

4.7 EIA(RS)485 AND K-BUS CONNECTIONS

For connecting the EIA(RS485) / K-Bus ports, use 2-core screened cable with a maximum total length of 1000 m or 200 nF total cable capacitance.

To guarantee the performance specifications, you must ensure continuity of the screen, when daisy chaining the connections.

Two-core screened twisted pair cable should be used. It is important to avoid circulating currents, which can cause noise and interference, especially when the cable runs between buildings. For this reason, the screen should be continuous and connected to ground at one end only, normally at the master connection point.

The K-Bus signal is a differential signal and there is no signal ground connection. If a signal ground connection is present in the bus cable then it must be ignored. At no stage should this be connected to the cable's screen or to the product's chassis. This is for both safety and noise reasons.

A typical cable specification would be:

- Each core: 16/0.2 mm² copper conductors, PVC insulated
- Nominal conductor area: 0.5 mm² per core
- Screen: Overall braid, PVC sheathed

4.8 IRIG-B CONNECTION

The IRIG-B input and BNC connector have a characteristic impedance of 50 ohms. We recommend that connections between the IRIG-B equipment and the product are made using coaxial cable of type RG59LSF with a halogen free, fire retardant sheath.

4.9 OPTO-INPUT CONNECTIONS

These should be wired with 1 mm² PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

Each opto-input has a selectable preset $\frac{1}{2}$ cycle filter. This makes the input immune to noise induced on the wiring. This can, however slow down the response. If you need to switch off the $\frac{1}{2}$ cycle filter, either use double pole switching on the input, or screened twisted cable on the input circuit.



Caution:

Protect the opto-inputs and their wiring with a maximum 16 A high rupture capacity (HRC) type NIT or TIA fuse.

4.10 OUTPUT RELAY CONNECTIONS

These should be wired with 1 mm PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

4.11 ETHERNET METALLIC CONNECTIONS

If the device has a metallic Ethernet connection, it can be connected to either a 10Base-T or a 100Base-TX Ethernet hub. Due to noise sensitivity, we recommend this type of connection only for short distance connections, ideally where the products and hubs are in the same cubicle. For increased noise immunity, CAT 6 (category 6) STP (shielded twisted pair) cable and connectors can be used.

The connector for the Ethernet port is a shielded RJ-45. The pin-out is as follows:

Pin	Signal name	Signal definition
1	TXP	Transmit (positive)
2	TXN	Transmit (negative)
3	RXP	Receive (positive)
4	-	Not used
5	-	Not used
6	RXN	Receive (negative)
7	-	Not used
8	-	Not used

4.12 ETHERNET FIBRE CONNECTIONS

We recommend the use of fibre-optic connections for permanent connections in a substation environment. The 100 Mbps fibre optic port uses type ST connectors (one for Tx and one for Rx), compatible with $50/125 \, \mu m$ or $62.5/125 \, \mu m$ multimode fibres at $1300 \, nm$ wavelength.

Note:

For models equipped with redundant Ethernet connections the product must be partially dismantled to set the fourth octet of the second IP address. This ideally, should be done before installation.

4.13 RS232 CONNECTION

Short term connections to the EIA(RS)232 port, located behind the bottom access cover, can be made using a screened multi-core communication cable up to 15 m long, or a total capacitance of 2500 pF. The cable should be terminated at the product end with a standard 9-pin D-type male connector.

4.14 DOWNLOAD/MONITOR PORT

Short term connections to the download/monitor port, located behind the bottom access cover, can be made using a screened 25-core communication cable up to 4 m long. The cable should be terminated at the product end with a 25-pin D-type male connector.

4.15 GPS FIBRE CONNECTION

Some products use a GPS 1 PPS timing signal. If applicable, this is connected to a fibre-optic port on the coprocessor board in slot B. The fibre-optic port uses an ST type connector, compatible with fibre multimode $50/125 \, \mu m$ or $62.5/125 \, \mu m - 850 \, nm$.

4.16 FIBRE COMMUNICATION CONNECTIONS

The fibre optic port consists of one or two channels using ST type connectors (one for Tx and one for Rx). The type of fibre used depends on the option selected.

850 nm and 1300 nm multimode systems use $50/125 \, \mu m$ or $62.5/125 \, \mu m$ multimode fibres. 1300 nm and 1550 nm single mode systems use $9/125 \, \mu m$ single mode fibres.

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5 CASE DIMENSIONS

Not all products are available in all case sizes.

5.1 CASE DIMENSIONS 40TE

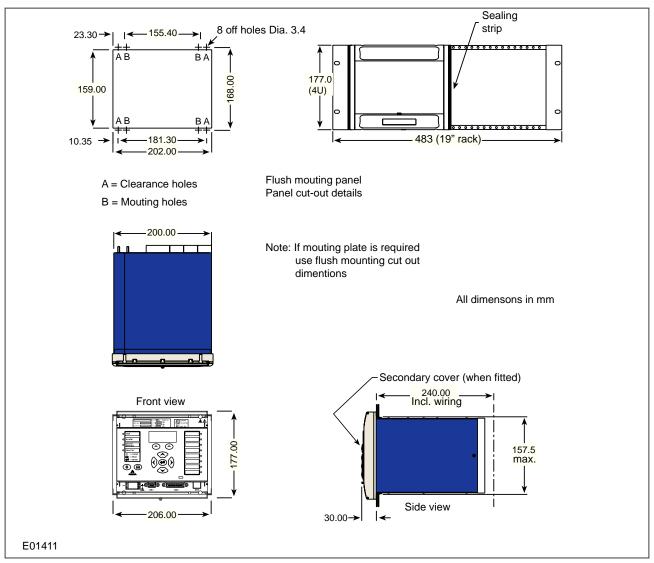


Figure 227: 40TE case dimensions

5.2 CASE DIMENSIONS 60TE

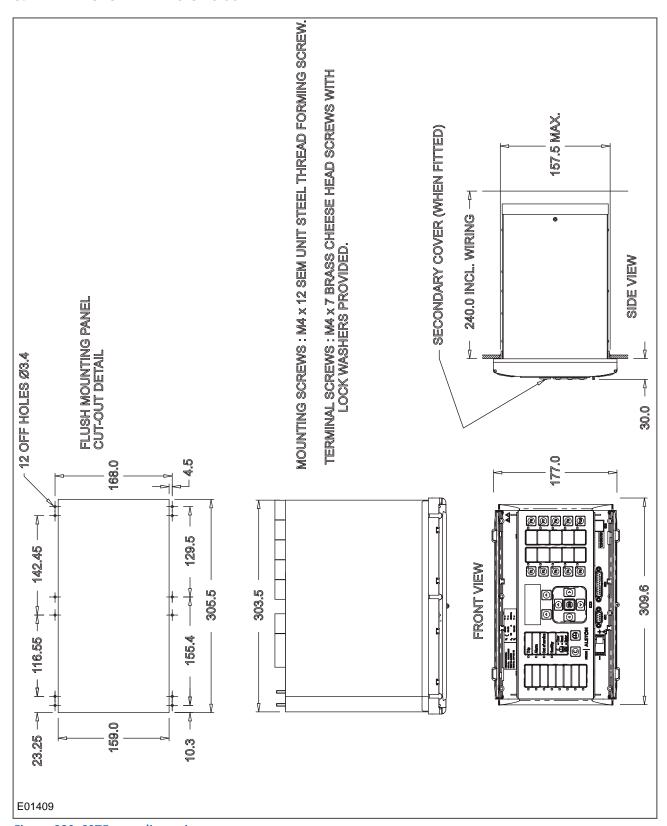


Figure 228: 60TE case dimensions

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5.3 CASE DIMENSIONS 80TE

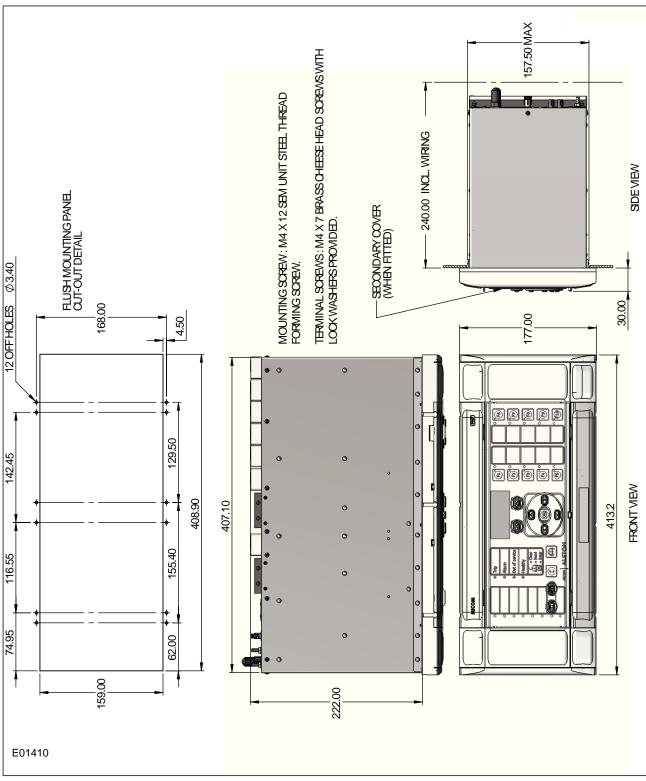


Figure 229: 80TE case dimensions

CHAPTER 21

COMMISSIONING INSTRUCTIONS

1	CHAPTER	OVERVIEW

This chapter contains the following sections:	
Chapter Overview	493
General Guidelines	494
Commissioning Test Menu	495
Commissioning Equipment	498
Product Checks	500
Setting Checks	509
Protection Timing Checks	511
Onload Checks	513
Final Checks	515

2 GENERAL GUIDELINES

General Electric IEDs are self-checking devices and will raise an alarm in the unlikely event of a failure. This is why the commissioning tests are less extensive than those for non-numeric electronic devices or electro-mechanical relays.

To commission the devices, you (the commissioning engineer) do not need to test every function. You need only verify that the hardware is functioning correctly and that the application-specific software settings have been applied. You can check the settings by extracting them using the settings application software, or by means of the front panel interface (HMI panel).

The menu language is user-selectable, so you can change it for commissioning purposes if required.

Note:

Remember to restore the language setting to the customer's preferred language on completion.



Caution:

Before carrying out any work on the equipment you should be familiar with the contents of the Safety Section or Safety Guide SFTY/4LM as well as the ratings on the equipment's rating label.



Warning:

With the exception of the CT shorting contacts check, do not disassemble the device during commissioning.

3 COMMISSIONING TEST MENU

The IED provides several test facilities under the *COMMISSION TESTS* menu heading. There are menu cells that allow you to monitor the status of the opto-inputs, output relay contacts, internal Digital Data Bus (DDB) signals and user-programmable LEDs. This section describes these commissioning test facilities.

3.1 OPTO I/P STATUS CELL (OPTO-INPUT STATUS)

This cell can be used to monitor the status of the opto-inputs while they are sequentially energised with a suitable DC voltage. The cell is a binary string that displays the status of the opto-inputs where '1' means energised and '0' means de-energised. If you move the cursor along the binary numbers, the corresponding label text is displayed for each logic input.

3.2 RELAY O/P STATUS CELL (RELAY OUTPUT STATUS)

This cell can be used to monitor the status of the relay outputs. The cell is a binary string that displays the status of the relay outputs where '1' means energised and '0' means de-energised. If you move the cursor along the binary numbers, the corresponding label text is displayed for each relay output.

The cell indicates the status of the output relays when the IED is in service. You can check for relay damage by comparing the status of the output contacts with their associated bits.

Note:

When the **Test Mode** cell is set to Contacts Blocked, the relay output status indicates which contacts would operate if the IED was in-service. It does not show the actual status of the output relays, as they are blocked.

3.3 TEST PORT STATUS CELL

This cell displays the status of the DDB signals that have been allocated in the **Monitor Bit** cells. If you move the cursor along the binary numbers, the corresponding DDB signal text string is displayed for each monitor bit.

By using this cell with suitable monitor bit settings, the state of the DDB signals can be displayed as various operating conditions or sequences are applied to the IED. This allows you to test the Programmable Scheme Logic (PSL).

3.4 MONITOR BIT 1 TO 8 CELLS

The eight Monitor Bit cells allows you to select eight DDB signals that can be observed in the Test Port Status cell or downloaded via the front port.

Each Monitor Bit cell can be assigned to a particular DDB signal. You set it by entering the required DDB signal number from the list of available DDB signals.

The pins of the monitor/download port used for monitor bits are as follows:

Monitor Bit	1	2	3	4	5	6	7	8
Monitor/Download Port Pin	11	12	15	13	20	21	23	24

The signal ground is available on pins 18, 19, 22 and 25.



Caution:

The monitor/download port is not electrically isolated against induced voltages on the communications channel. It should therefore only be used for local communications.

3.5 TEST MODE CELL

This cell allows you to perform secondary injection testing. It also lets you test the output contacts directly by applying menu-controlled test signals.

To go into test mode, select the *Test Mode* option in the *Test Mode* cell. This takes the IED out of service causing an alarm condition to be recorded and the *Out of Service* LED to illuminate. This also freezes any information stored in the *CB CONDITION* column. In IEC 60870-5-103 versions, it changes the Cause of Transmission (COT) to Test Mode.

In Test Mode, the output contacts are still active. To disable the output contacts you must select the Contacts Blocked option.

Once testing is complete, return the device back into service by setting the *Test Mode* Cell back to *Disabled*.



Caution:

When the cell is in Test Mode, the Scheme Logic still drives the output relays, which could result in tripping of circuit breakers. To avoid this, set the *Test Mode* cell to *Contacts Blocked*.

Note

Test mode and Contacts Blocked mode can also be selected by energising an opto-input mapped to the Test Mode signal, and the Contact Block signal respectively.

3.6 TEST PATTERN CELL

The **Test Pattern** cell is used to select the output relay contacts to be tested when the **Contact Test** cell is set to $Apply\ Test$. The cell has a binary string with one bit for each user-configurable output contact, which can be set to '1' to operate the output and '0' to not operate it.

3.7 CONTACT TEST CELL

When the Apply Test command in this cell is issued, the contacts set for operation change state. Once the test has been applied, the command text on the LCD will change to **No Operation** and the contacts will remain in the Test state until reset by issuing the Remove Test command. The command text on the LCD will show **No Operation** after the Remove Test command has been issued.

Note:

When the **Test Mode** cell is set to Contacts Blocked the **Relay O/P Status** cell does not show the current status of the output relays and therefore cannot be used to confirm operation of the output relays. Therefore it will be necessary to monitor the state of each contact in turn.

3.8 TEST LEDS CELL

When the $Apply\ Test$ command in this cell is issued, the user-programmable LEDs illuminate for approximately 2 seconds before switching off, and the command text on the LCD reverts to **No Operation**.

3.9 TEST AUTORECLOSE CELL

Where the IED provides an auto-reclose function, this cell will be available for testing the sequence of circuit breaker trip and auto-reclose cycles.

The 3 Pole Test command causes the device to perform the first three phase trip/reclose cycle so that associated output contacts can be checked for operation at the correct times during the cycle. Once the trip

output has operated the command text will revert to *No Operation* whilst the rest of the auto-reclose cycle is performed. To test subsequent three-phase autoreclose cycles, you repeat the *3 Pole Test* command.

Note:

The default settings for the programmable scheme logic has the AR Trip Test signals mapped to the Trip Input signals. If the programmable scheme logic has been changed, it is essential that these signals retain this mapping for the Test Autoreclose facility to work.

3.10 RED AND GREEN LED STATUS CELLS

These cells contain binary strings that indicate which of the user-programmable red and green LEDs are illuminated when accessing from a remote location. A '1' indicates that a particular LED is illuminated.

Note:

When the status in both Red LED Status and Green LED Status cells is '1', this indicates the LEDs illumination is yellow.

3.11 USING A MONITOR PORT TEST BOX

A test box containing eight LEDs and a switchable audible indicator is available. It is housed in a small plastic box with a 25-pin male D-connector that plugs directly into the monitor/download port. There is also a 25-pin female D-connector which allows other connections to be made to the monitor/download port while the monitor/download port test box is in place.

Each LED corresponds to one of the monitor bit pins on the monitor/download port. *Monitor Bit 1* is on the left-hand side when viewed from the front of the IED. The audible indicator can be selected to sound if a voltage appears on any of the eight monitor pins. Alternatively it can be set to remain silent, using only the LEDs.

4 COMMISSIONING EQUIPMENT

Specialist test equipment is required to commission this product. We recognise three classes of equipment for commissioning :

- Recommended
- Essential
- Advisory

Recommended equipment constitutes equipment that is both necessary, and sufficient, to verify correct performance of the principal protection functions.

Essential equipment represents the minimum necessary to check that the product includes the basic expected protection functions and that they operate within limits.

Advisory equipment represents equipment that is needed to verify satisfactory operation of features that may be unused, or supplementary, or which may, for example, be integral to a distributed control/automation scheme. Operation of such features may, perhaps, be more appropriately verified as part of a customer defined commissioning requirement, or as part of a system-level commissioning regime.

4.1 RECOMMENDED COMMISSIONING EQUIPMENT

The minimum recommended equipment is a multifunctional three-phase AC current and voltage injection test set featuring:

- Controlled three-phase AC current and voltage sources,
- Transient (dynamic) switching between pre-fault and post-fault conditions (to generate delta conditions),
- Dynamic impedance state sequencer (capable of sequencing through 4 impedance states),
- Integrated or separate variable DC supply (0 250 V)
- Integrated or separate AC and DC measurement capabilities (0-440V AC, 0-250V DC)
- Integrated and/or separate timer,
- Integrated and/or separate test switches.

In addition, you will need:

- A portable computer, installed with appropriate software to liaise with the equipment under test (EUT). Typically this software will be proprietary to the product's manufacturer (for example MiCOM S1 Agile).
- Suitable electrical test leads.
- Electronic or brushless insulation tester with a DC output not exceeding 500 V
- Continuity tester
- Verified application-specific settings files

4.2 ESSENTIAL COMMISSIONING EQUIPMENT

As an absolute minimum, the following equipment is required:

- AC current source coupled with AC voltage source
- Variable DC supply (0 250V)
- Multimeter capable of measuring AC and DC current and voltage (0-440V AC, 0-250V DC)
- Timer
- Test switches
- Suitable electrical test leads
- Continuity tester

4.3 ADVISORY TEST EQUIPMENT

Advisory test equipment may be required for extended commissioning procedures:

- Current clamp meter
- Multi-finger test plug:
 - P992 for test block type P991
 - MMLB for test block type MMLG blocks
- Electronic or brushless insulation tester with a DC output not exceeding 500 V
- KITZ K-Bus EIA(RS)232 protocol converter for testing EIA(RS)485 K-Bus port
- EIA(RS)485 to EIA(RS)232 converter for testing EIA(RS)485 Courier/MODBUS/IEC60870-5-103/DNP3 port
- A portable printer (for printing a setting record from the portable PC) and or writeable, detachable memory device.
- Phase angle meter
- Phase rotation meter
- Fibre-optic power meter.
- Fibre optic test leads (minimum 2). 10m minimum length, multimode 50/125 μ m or 62.5 μ m terminated with BFOC (ST) 2.5 connectors for testing the fibre-optic RP1 port.

5 PRODUCT CHECKS

These product checks are designed to ensure that the device has not been physically damaged prior to commissioning, is functioning correctly and that all input quantity measurements are within the stated tolerances.

If the application-specific settings have been applied to the IED prior to commissioning, you should make a copy of the settings. This will allow you to restore them at a later date if necessary. This can be done by:

- Obtaining a setting file from the customer.
- Extracting the settings from the IED itself, using a portable PC with appropriate setting software.

If the customer has changed the password that prevents unauthorised changes to some of the settings, either the revised password should be provided, or the original password restored before testing.

Note:

If the password has been lost, a recovery password can be obtained from General Electric.

5.1 PRODUCT CHECKS WITH THE IED DE-ENERGISED



Warning:

The following group of tests should be carried out without the auxiliary supply being applied to the IED and, if applicable, with the trip circuit isolated.

The current and voltage transformer connections must be isolated from the IED for these checks. If a P991 test block is provided, the required isolation can be achieved by inserting test plug type P992. This open circuits all wiring routed through the test block.

Before inserting the test plug, you should check the scheme diagram to ensure that this will not cause damage or a safety hazard (the test block may, for example, be associated with protection current transformer circuits). The sockets in the test plug, which correspond to the current transformer secondary windings, must be linked before the test plug is inserted into the test block.



Warning:

Never open-circuit the secondary circuit of a current transformer since the high voltage produced may be lethal and could damage insulation.

If a test block is not provided, the voltage transformer supply to the IED should be isolated by means of the panel links or connecting blocks. The line current transformers should be short-circuited and disconnected from the IED terminals. Where means of isolating the auxiliary supply and trip circuit (for example isolation links, fuses and MCB) are provided, these should be used. If this is not possible, the wiring to these circuits must be disconnected and the exposed ends suitably terminated to prevent them from being a safety hazard.

5.1.1 VISUAL INSPECTION

Warning:

Check the rating information under the top access cover on the front of the IED.



Warning:

Check that the IED being tested is correct for the line or circuit.

Warning:

Record the circuit reference and system details.

Warning:

Check the CT secondary current rating and record the CT tap which is in use.

Carefully examine the IED to see that no physical damage has occurred since installation.

Ensure that the case earthing connections (bottom left-hand corner at the rear of the IED case) are used to connect the IED to a local earth bar using an adequate conductor.

5.1.2 CURRENT TRANSFORMER SHORTING CONTACTS

Check the current transformer shorting contacts to ensure that they close when the heavy-duty terminal block is disconnected from the current input board.

The heavy-duty terminal blocks are fastened to the rear panel using four crosshead screws. These are located two at the top and two at the bottom.

Note:

Use a magnetic bladed screwdriver to minimise the risk of the screws being left in the terminal block or lost.

Pull the terminal block away from the rear of the case and check with a continuity tester that all the shorting switches being used are closed.

5.1.3 INSULATION

Insulation resistance tests are only necessary during commissioning if explicitly requested.

Isolate all wiring from the earth and test the insulation with an electronic or brushless insulation tester at a DC voltage not exceeding 500 V. Terminals of the same circuits should be temporarily connected together.

The insulation resistance should be greater than 100 M Ω at 500 V.

On completion of the insulation resistance tests, ensure all external wiring is correctly reconnected to the IED.

5.1.4 EXTERNAL WIRING



Caution:

Check that the external wiring is correct according to the relevant IED and scheme diagrams. Ensure that phasing/phase rotation appears to be as expected.

5.1.5 WATCHDOG CONTACTS

Using a continuity tester, check that the Watchdog contacts are in the following states:

Terminals	Contact state with product de-energised
11 - 12 on power supply board	Closed
13 - 14 on power supply board	Open

5.1.6 POWER SUPPLY

Depending on its nominal supply rating, the IED can be operated from either a DC only or an AC/DC auxiliary supply. The incoming voltage must be within the operating range specified below.

Without energising the IED measure the auxiliary supply to ensure it is within the operating range.

Nominal supply rating DC	Nominal supply rating AC RMS	DC operating range	AC operating range
24 - 54 V	N/A	19 to 65 V	N/A
48 - 125 V	30 - 100 V	37 to 150 V	24 - 110 V
110 - 250 V	100 - 240 V	87 to 300 V	80 to 265 V

Note:

The IED can withstand an AC ripple of up to 12% of the upper rated voltage on the DC auxiliary supply.



Warning:

Do not energise the IED or interface unit using the battery charger with the battery disconnected as this can irreparably damage the power supply circuitry.



Caution:

Energise the IED only if the auxiliary supply is within the specified operating ranges. If a test block is provided, it may be necessary to link across the front of the test plug to connect the auxiliary supply to the IED.

5.2 PRODUCT CHECKS WITH THE IED ENERGISED



Warning:

The current and voltage transformer connections must remain isolated from the IED for these checks. The trip circuit should also remain isolated to prevent accidental operation of the associated circuit breaker.

The following group of tests verifies that the IED hardware and software is functioning correctly and should be carried out with the supply applied to the IED.

5.2.1 WATCHDOG CONTACTS

Using a continuity tester, check that the Watchdog contacts are in the following states when energised and healthy.

Terminals	Contact state with product energised
11 - 12 on power supply board	Open

Terminals	Contact state with product energised
13 - 14 on power supply board	Closed

5.2.2 TEST LCD

The Liquid Crystal Display (LCD) is designed to operate in a wide range of substation ambient temperatures. For this purpose, the IEDs have an *LCD Contrast* setting. The contrast is factory pre-set, but it may be necessary to adjust the contrast to give the best in-service display.

To change the contrast, you can increment or decrement the *LCD Contrast* cell in the *CONFIGURATION* column.



Caution:

Before applying a contrast setting, make sure that it will not make the display so light or dark such that menu text becomes unreadable. It is possible to restore the visibility of a display by downloading a setting file, with the LCD Contrast set within the typical range of 7 - 11.

5.2.3 DATE AND TIME

The date and time is stored in memory, which is backed up by an auxiliary battery situated at the front of the device behind the lower access cover. When delivered, this battery is isolated to prevent battery drain during transportation and storage.

Before setting the date and time, ensure that the isolation strip has been removed. With the lower access cover open, the battery isolation strip can be identified by a red tab protruding from the positive side of the battery compartment. Pull the red tab to remove the isolation strip.

The method for setting the date and time depends on whether an IRIG-B signal is being used or not. The IRIG-B signal will override the time, day and month settings, but not the initial year setting. For this reason, you must ensure you set the correct year, even if the device is using IRIG-B to maintain the internal clock.

You set the Date and Time by one of the following methods:

- Using the front panel to set the **Date and Time** cells respectively
- By sending a courier command to the **Date/Time** cell (Courier reference 0801)

Note:

If the auxiliary supply fails, the time and date will be maintained by the auxiliary battery. Therefore, when the auxiliary supply is restored, you should not have to set the time and date again. To test this, remove the IRIG-B signal, and then remove the auxiliary supply. Leave the device de-energised for approximately 30 seconds. On re energisation, the time should be correct.

When using IRIG-B to maintain the clock, the IED must first be connected to the satellite clock equipment (usually a P594), which should be energised and functioning.

- 1. Set the IRIG-B Sync cell in the DATE AND TIME column to Enabled.
- 2. Ensure the IED is receiving the IRIG-B signal by checking that cell IRIG-B Status reads Active.
- 3. Once the IRIG-B signal is active, adjust the time offset of the universal co coordinated time (satellite clock time) on the satellite clock equipment so that local time is displayed.
- 4. Check that the time, date and month are correct in the Date/Time cell. The IRIG-B signal does not contain the current year so it will need to be set manually in this cell.
- 5. Reconnect the IRIG-B signal.

If the time and date is not being maintained by an IRIG-B signal, ensure that the IRIG-B Sync cell in the DATE AND TIME column is set to <code>Disabled</code>.

1. Set the date and time to the correct local time and date using Date/Time cell or using the serial protocol.

5.2.4 TEST LEDS

On power-up, all LEDs should first flash yellow. Following this, the green "Healthy" LED should illuminate indicating that the device is healthy.

The IED's non-volatile memory stores the states of the alarm, the trip, and the user-programmable LED indicators (if configured to latch). These indicators may also illuminate when the auxiliary supply is applied.

If any of these LEDs are ON then they should be reset before proceeding with further testing. If the LEDs successfully reset (the LED goes off), no testing is needed for that LED because it is obviously operational.

5.2.5 TEST ALARM AND OUT-OF-SERVICE LEDS

The alarm and out of service LEDs can be tested using the COMMISSION TESTS menu column.

- 1. Set the **Test Mode** cell to Contacts Blocked.
- 2. Check that the out of service LED illuminates continuously and the alarm LED flashes.

It is not necessary to return the **Test Mode** cell to <code>Disabled</code> at this stage because the test mode will be required for later tests.

5.2.6 TEST TRIP LED

The trip LED can be tested by initiating a manual circuit breaker trip. However, the trip LED will operate during the setting checks performed later. Therefore no further testing of the trip LED is required at this stage.

5.2.7 TEST USER-PROGRAMMABLE LEDS

To test these LEDs, set the Test LEDs cell to Apply Test. Check that all user-programmable LEDs illuminate.

5.2.8 TEST OPTO-INPUTS

This test checks that all the opto-inputs on the IED are functioning correctly.

The opto-inputs should be energised one at a time. For terminal numbers, please see the external connection diagrams in the "Wiring Diagrams" chapter. Ensuring correct polarity, connect the supply voltage to the appropriate terminals for the input being tested.

The status of each opto-input can be viewed using either the *Opto I/P Status* cell in the *SYSTEM DATA* column, or the *Opto I/P Status* cell in the *COMMISSION TESTS* column.

A '1' indicates an energised input and a '0' indicates a de-energised input. When each opto-input is energised, one of the characters on the bottom line of the display changes to indicate the new state of the input.

5.2.9 TEST OUTPUT RELAYS

This test checks that all the output relays are functioning correctly.

- 1. Ensure that the IED is still in test mode by viewing the **Test Mode** cell in the **COMMISSION TESTS** column. Ensure that it is set to **Contacts Blocked**.
- 2. The output relays should be energised one at a time. To select output relay 1 for testing, set the Test Pattern cell as appropriate.
- 3. Connect a continuity tester across the terminals corresponding to output relay 1 as shown in the external connection diagram.
- 4. To operate the output relay set the Contact Test cell to Apply Test.
- 5. Check the operation with the continuity tester.
- 6. Measure the resistance of the contacts in the closed state.

- 7. Reset the output relay by setting the Contact Test cell to Remove Test.
- 8. Repeat the test for the remaining output relays.
- 9. Return the IED to service by setting the Test Mode cell in the COMMISSION TESTS menu to Disabled.

5.2.10 TEST SERIAL COMMUNICATION PORT RP1

You need only perform this test if the IED is to be accessed from a remote location with a permanent serial connection to the communications port. The scope of this test does not extend to verifying operation with connected equipment beyond any supplied protocol converter. It verifies operation of the rear communication port (and if applicable the protocol converter) and varies according to the protocol fitted.

5.2.10.1 CHECK PHYSICAL CONNECTIVITY

The rear communication port RP1 is presented on terminals 16, 17 and 18 of the power supply terminal block. Screened twisted pair cable is used to make a connection to the port. The cable screen should be connected to pin 16 and pins 17 and 18 are for the communication signal:

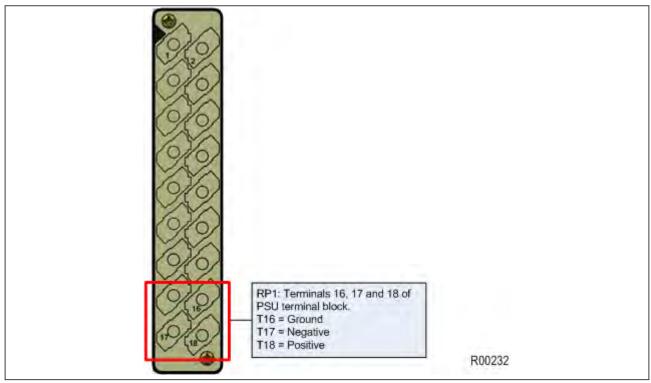


Figure 230: RP1 physical connection

For K-Bus applications, pins 17 and 18 are not polarity sensitive and it does not matter which way round the wires are connected. EIA(RS)485 is polarity sensitive, so you must ensure the wires are connected the correct way round (pin 18 is positive, pin 17 is negative).

If K-Bus is being used, a Kitz protocol converter (KITZ101, KITZ102 OR KITZ201) will have been installed to convert the K-Bus signals into RS232. Likewise, if RS485 is being used, an RS485-RS232 converter will have been installed. In the case where a protocol converter is being used, a laptop PC running appropriate software (such as MiCOM S1 Agile) can be connected to the incoming side of the protocol converter. An example for K-bus to RS232 conversion is shown below. RS485 to RS232 would follow the same principle, only using a RS485-RS232 converter. Most modern laptops have USB ports, so it is likely you will also require a RS232 to USB converter too.

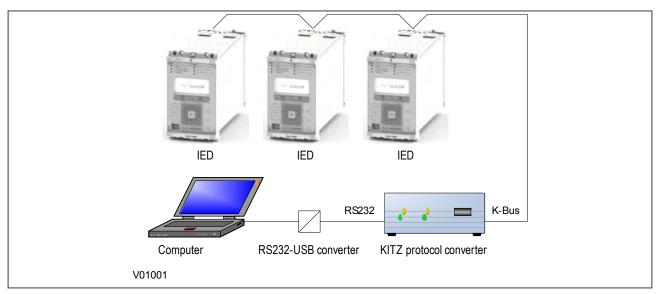


Figure 231: Remote communication using K-bus

Fibre Connection

Some models have an optional fibre optic communications port fitted (on a separate communications board). The communications port to be used is selected by setting the Physical Link cell in the COMMUNICATIONS column, the values being Copper or K-Bus for the RS485/K-bus port and $Fibre\ Optic$ for the fibre optic port.

5.2.10.2 CHECK LOGICAL CONNECTIVITY

The logical connectivity depends on the chosen data protocol, but the principles of testing remain the same for all protocol variants:

- 1. Ensure that the communications baud rate and parity settings in the application software are set the same as those on the protocol converter.
- 2. For Courier models, ensure that you have set the correct RP1 address
- 3. Check that communications can be established with this IED using the portable PC/Master Station.

5.2.11 TEST SERIAL COMMUNICATION PORT RP2

RP2 is an optional second serial port board providing additional serial connectivity. It provides two 9-pin D-type serial port connectors SK4 and SK5. Both ports are configured as DTE (Date Terminal Equipment) ports. That means they can be connected to communications equipment such as a modem with a straight-through cable.

SK4 can be configured as an EIA(RS232), EIA(RS485), or K-Bus connection for Courier protocol only, whilst SK5 is fixed to EIA(RS)232 for InterMiCOM signalling only.

It is not the intention of this test to verify the operation of the complete communication link between the IED and the remote location, just the IED's rear communication port and, if applicable, the protocol converter.

The only checks that need to be made are as follows:

- 1. Set the *RP2 Port Config* cell in the *COMMUNICATIONS* column to the required physical protocol; (K-Bus, EIA(RS)485, or EIA(RS)232.
- 2. Set the IED's Courier address to the correct value (it must be between 1 and 254).

5.2.12 TEST ETHERNET COMMUNICATION

For products that employ Ethernet communications, we recommend that testing be limited to a visual check that the correct ports are fitted and that there is no sign of physical damage.

If there is no board fitted or the board is faulty, a NIC link alarm will be raised (providing this option has been set in the *NIC Link Report* cell in the *COMMUNICATIONS* column).

5.3 SECONDARY INJECTION TESTS

Secondary injection testing is carried out to verify the integrity of the VT and CT readings. All devices leave the factory set for operation at a system frequency of 50 Hz. If operation at 60 Hz is required, you must set this in the Frequency cell in the SYSTEM DATA column.

The PMU must be installed and connected to a 1pps fibre optic synchronising signal and a demodulated IRIG-B signal, provided by a device such as a P594 or a REASON RT430.

Connect the current and voltage outputs of the test set to the appropriate terminals of the first voltage and current channel and apply nominal voltage and current with the current lagging the voltage by 90 degrees.

5.3.1 TEST CURRENT INPUTS

This test verifies that the current measurement inputs are configured correctly.

- 1. Using secondary injection test equipment such as an Omicron, apply and measure nominal rated current to each CT in turn.
- 2. Check its magnitude using a multi-meter or test set readout. Check this value against the value displayed on the HMI panel (usually in MEASUREMENTS 1 column).
- 3. Record the displayed value. The measured current values will either be in primary or secondary Amperes. If the Local Values cell in the MEASURE'T SETUP column is set to Primary, the values displayed should be equal to the applied current multiplied by the corresponding current transformer ratio (set in the CT AND VT RATIOS column). If the Local Values cell is set to Secondary, the value displayed should be equal to the applied current.

Note:

If a PC connected to the IED using the rear communications port is being used to display the measured current, the process will be similar. However, the setting of the Remote Values cell in the MEASURE'T SETUP column will determine whether the displayed values are in primary or secondary Amperes.

The measurement accuracy of the IED is \pm 1%. However, an additional allowance must be made for the accuracy of the test equipment being used.

5.3.2 TEST VOLTAGE INPUTS

This test verifies that the voltage measurement inputs are configured correctly.

- 1. Using secondary injection test equipment, apply and measure the rated voltage to each voltage transformer input in turn.
- 2. Check its magnitude using a multimeter or test set readout. Check this value against the value displayed on the HMI panel (usually in MEASUREMENTS 1 column).
- 3. Record the value displayed. The measured voltage values will either be in primary or secondary Volts. If the Local Values cell in the MEASURE'T SETUP column is set to Primary, the values displayed should be equal to the applied voltage multiplied by the corresponding voltage transformer ratio (set in the CT AND VT RATIOS column). If the Local Values cell is set to Secondary, the value displayed should be equal to the applied voltage.

Note:

If a PC connected to the IED using the rear communications port is being used to display the measured current, the process will be similar. However, the setting of the Remote Values cell in the MEASURE'T SETUP column will determine whether the displayed values are in primary or secondary Amperes.

The measurement accuracy of the IED is +/-1%. However, an additional allowance must be made for the accuracy of the test equipment being used.

6 SETTING CHECKS

The setting checks ensure that all of the application-specific settings (both the IED's function and programmable scheme logic settings) have been correctly applied.

Note:

If applicable, the trip circuit should remain isolated during these checks to prevent accidental operation of the associated circuit breaker.

6.1 APPLY APPLICATION-SPECIFIC SETTINGS

There are two different methods of applying the settings to the IED

- Transferring settings to the IED from a pre-prepared setting file using MiCOM S1 Agile
- Enter the settings manually using the IED's front panel HMI

6.1.1 TRANSFERRING SETTINGS FROM A SETTINGS FILE

This is the preferred method for transferring function settings. It is much faster and there is a lower margin for error.

- 1. Connect a PC running the Settings Application Software to the IED's front port, or a rear Ethernet port.

 Alternatively connect to the rear Courier communications port, using a KITZ protocol converter if necessary.
- 2. Power on the IED
- 3. Enter the IP address of the device if it is Ethernet enabled
- 4. Right-click the appropriate device name in the System Explorer pane and select **Send**
- 5. In the **Send to** dialog select the setting files and click **Send**

Note:

The device name may not already exist in the system shown in **System Explorer**. In this case, perform a **Quick Connect** to the IED, then manually add the settings file to the device name in the system. Refer to the Settings Application Software help for details of how to do this.

6.1.2 ENTERING SETTINGS USING THE HMI

- 1. Starting at the default display, press the Down cursor key to show the first column heading.
- 2. Use the horizontal cursor keys to select the required column heading.
- 3. Use the vertical cursor keys to view the setting data in the column.
- 4. To return to the column header, either press the Up cursor key for a second or so, or press the **Cancel** key once. It is only possible to move across columns at the column heading level.
- 5. To return to the default display, press the Up cursor key or the Cancel key from any of the column headings. If you use the auto-repeat function of the Up cursor key, you cannot go straight to the default display from one of the column cells because the auto-repeat stops at the column heading.
- 6. To change the value of a setting, go to the relevant cell in the menu, then press the **Enter** key to change the cell value. A flashing cursor on the LCD shows that the value can be changed. You may be prompted for a password first.
- 7. To change the setting value, press the vertical cursor keys. If the setting to be changed is a binary value or a text string, select the required bit or character to be changed using the left and right cursor keys.

- 8. Press the **Enter** key to confirm the new setting value or the **Clear** key to discard it. The new setting is automatically discarded if it is not confirmed within 15 seconds.
- 9. For protection group settings and disturbance recorder settings, the changes must be confirmed before they are used. When all required changes have been entered, return to the column heading level and press the down cursor key. Before returning to the default display, the following prompt appears.

Update settings? ENTER or CLEAR

10. Press the **Enter** key to accept the new settings or press the **Clear** key to discard the new settings.

Note:

If the menu time-out occurs before the setting changes have been confirmed, the setting values are also discarded. Control and support settings are updated immediately after they are entered, without the Update settings prompt. It is not possible to change the PSL using the IED's front panel HMI.



Caution:

Where the installation needs application-specific PSL, the relevant .psl files, must be transferred to the IED, for each and every setting group that will be used. If you do not do this, the factory default PSL will still be resident. This may have severe operational and safety consequences.

7 PROTECTION TIMING CHECKS

There is no need to check every protection function. Only one protection function needs to be checked as the purpose is to verify the timing on the processor is functioning correctly.

7.1 OVERCURRENT CHECK

If the overcurrent protection function is being used, test the overcurrent protection for stage 1.

- 1. Check for any possible dependency conditions and simulate as appropriate.
- 2. In the CONFIGURATION column, disable all protection elements other than the one being tested.
- 3. Make a note of which elements need to be re-enabled after testing.
- 4. Connect the test circuit.
- 5. Perform the test.
- 6. Check the operating time.

7.2 CONNECTING THE TEST CIRCUIT

- 1. Use the PSL to determine which output relay will operate when an overcurrent trip occurs.
- 2. Use the output relay assigned to *Trip Output A*.
- 3. Use the PSL to map the protection stage under test directly to an output relay.

Note:

If using the default PSL, use output relay 3 as this is already mapped to the DDB signal Trip Command Out.

- 4. Connect the output relay so that its operation will trip the test set and stop the timer.
- 5. Connect the current output of the test set to the A-phase current transformer input.

 If the *I>1 Directional* cell in the *OVERCURRENT* column is set to *Directional Fwd*, the current should flow out of terminal 2. If set to *Directional Rev*, it should flow into terminal 2.
 - If the *I>1 Directional* cell in the *OVERCURRENT* column has been set to *Directional Fwd* or *Directional Rev*, the rated voltage should be applied to terminals 20 and 21.
- 6. Ensure that the timer starts when the current is applied.

Note:

If the timer does not stop when the current is applied and stage 1 has been set for directional operation, the connections may be incorrect for the direction of operation set. Try again with the current connections reversed.

7.3 PERFORMING THE TEST

- 1. Ensure that the timer is reset.
- 2. Apply a current of twice the setting shown in the *I>1 Current Set* cell in the *OVERCURRENT* column.
- 3. Note the time displayed when the timer stops.
- 4. Check that the red trip LED has illuminated.

7.4 CHECK THE OPERATING TIME

Check that the operating time recorded by the timer is within the range shown below.

For all characteristics, allowance must be made for the accuracy of the test equipment being used.

Characteristic	Operating time at twice current setting and time multiplier/ time dial setting of 1.0	
	Nominal (seconds)	Range (seconds)
DT	I>1 Time Delay setting	Setting ±2%
IEC S Inverse	10.03	9.53 - 10.53
IEC V Inverse	13.50	12.83 - 14.18
IEC E Inverse	26.67	24.67 - 28.67
UK LT Inverse	120.00	114.00 - 126.00
IEEE M Inverse	3.8	3.61 - 4.0
IEEE V Inverse	7.03	6.68 - 7.38
IEEE E Inverse	9.50	9.02 - 9.97
US Inverse	2.16	2.05 - 2.27
US ST Inverse	12.12	11.51 - 12.73

Note

With the exception of the definite time characteristic, the operating times given are for a Time Multiplier Setting (TMS) or Time Dial Setting (TDS) of 1. For other values of TMS or TDS, the values need to be modified accordingly.

Note

For definite time and inverse characteristics there is an additional delay of up to 0.02 second and 0.08 second respectively. You may need to add this the IED's acceptable range of operating times.



Caution:

On completion of the tests, you must restore all settings to customer specifications.

8 ONLOAD CHECKS



Warning:

Onload checks are potentially very dangerous and may only be carried out by qualified and authorised personnel.

Onload checks can only be carried out if there are no restrictions preventing the energisation of the plant, and the other devices in the group have already been commissioned.

Remove all test leads and temporary shorting links, then replace any external wiring that has been removed to allow testing.



Warnina:

If any external wiring has been disconnected for the commissioning process, replace it in accordance with the relevant external connection or scheme diagram.

8.1 CONFIRM CURRENT CONNECTIONS

- 1. Measure the current transformer secondary values for each input either by:
 - a. reading from the device's HMI panel (providing it has first been verified by a secondary injection test)
 - b. using a current clamp meter
- 2. Check that the current transformer polarities are correct by measuring the phase angle between the current and voltage, either against a phase meter already installed on site and known to be correct or by determining the direction of power flow by contacting the system control centre.
- 3. Ensure the current flowing in the neutral circuit of the current transformers is negligible.

If the *Local Values* cell is set to *Secondary*, the values displayed should be equal to the applied secondary voltage. The values should be within 1% of the applied secondary voltages. However, an additional allowance must be made for the accuracy of the test equipment being used.

If the *Local Values* cell is set to *Primary*, the values displayed should be equal to the applied secondary voltage multiplied the corresponding voltage transformer ratio set in the *CT & VT RATIOS* column. The values should be within 1% of the expected values, plus an additional allowance for the accuracy of the test equipment being used.

8.2 CONFIRM VOLTAGE CONNECTIONS

- 1. Using a multimeter, measure the voltage transformer secondary voltages to ensure they are correctly rated.
- 2. Check that the system phase rotation is correct using a phase rotation meter.
- 3. Compare the values of the secondary phase voltages with the measured voltage magnitude values, which can be found in the MEASUREMENTS 1 menu column.

Cell in MEASUREMENTS 1 Column	Corresponding VT ratio in CT/VT RATIOS column
VAB MAGNITUDE	
VBC MAGNITUDE	
VCA MAGNITUDE	Main VT Primary / Main VT Sec'y
VAN MAGNITUDE	Main VI Primary / Main VI Sec y
VBN MAGNITUDE	
VCN MAGNITUDE	
C/S Voltage Mag	CS VT Primary / CS VT Secondary

If the *Local Values* cell is set to *Secondary*, the values displayed should be equal to the applied secondary voltage. The values should be within 1% of the applied secondary voltages. However, an additional allowance must be made for the accuracy of the test equipment being used.

If the *Local Values* cell is set to *Primary*, the values displayed should be equal to the applied secondary voltage multiplied the corresponding voltage transformer ratio set in the *CT & VT RATIOS* column. The values should be within 1% of the expected values, plus an additional allowance for the accuracy of the test equipment being used.

8.3 ON-LOAD DIRECTIONAL TEST

This test ensures that directional overcurrent and fault locator functions have the correct forward/reverse response to fault and load conditions. For this test you must first know the actual direction of power flow on the system. If you do not already know this you must determine it using adjacent instrumentation or protection already in-service.

- For load current flowing in the Forward direction (power export to the remote line end), the **A Phase Watts** cell in the MEASUREMENTS 2 column should show positive power signing.
- For load current flowing in the Reverse direction (power import from the remote line end), the *A Phase Watts* cell in the *MEASUREMENTS 2* column should show negative power signing.

Note:

This check applies only for Measurement Modes 0 (default), and 2. This should be checked in the MEASURE'T SETUP column (**Measurement Mode** = 0 or 2). If measurement modes 1 or 3 are used, the expected power flow signing would be opposite to that shown above.

In the event of any uncertainty, check the phase angle of the phase currents with respect to their phase voltage.

9 FINAL CHECKS

- 1. Remove all test leads and temporary shorting leads.
- 2. If you have had to disconnect any of the external wiring in order to perform the wiring verification tests, replace all wiring, fuses and links in accordance with the relevant external connection or scheme diagram.
- 3. The settings applied should be carefully checked against the required application-specific settings to ensure that they are correct, and have not been mistakenly altered during testing.
- 4. Ensure that all protection elements required have been set to Enabled in the CONFIGURATION column.
- 5. Ensure that the IED has been restored to service by checking that the **Test Mode** cell in the **COMMISSION TESTS** column is set to **Disabled**.
- 6. If the IED is in a new installation or the circuit breaker has just been maintained, the circuit breaker maintenance and current counters should be zero. These counters can be reset using the **Reset All Values** cell. If the required access level is not active, the device will prompt for a password to be entered so that the setting change can be made.
- 7. If the menu language has been changed to allow accurate testing it should be restored to the customer's preferred language.
- 8. If a P991/MMLG test block is installed, remove the P992/MMLB test plug and replace the cover so that the protection is put into service.
- 9. Ensure that all event records, fault records, disturbance records, alarms and LEDs and communications statistics have been reset.

Note:

Remember to restore the language setting to the customer's preferred language on completion.

CHAPTER 22

MAINTENANCE AND TROUBLESHOOTING

1 CHAPTER OVERVIEW

The Maintenance and Troubleshooting chapter provides details of how to maintain and troubleshoot products based on the Px4x and P40Agile platforms. Always follow the warning signs in this chapter. Failure to do so may result injury or defective equipment.



Caution:

Before carrying out any work on the equipment you should be familiar with the contents of the Safety Section or the Safety Guide SFTY/4LM and the ratings on the equipment's rating label.

The troubleshooting part of the chapter allows an error condition on the IED to be identified so that appropriate corrective action can be taken.

If the device develops a fault, it is usually possible to identify which module needs replacing. It is not possible to perform an on-site repair to a faulty module.

If you return a faulty unit or module to the manufacturer or one of their approved service centres, you should include a completed copy of the Repair or Modification Return Authorization (RMA) form.

This chapter contains the following sections:

Chapter Overview	519
Maintenance	520
Troubleshooting	528
Repair and Modification Procedure	532

2 MAINTENANCE

2.1 MAINTENANCE CHECKS

In view of the critical nature of the application, General Electric products should be checked at regular intervals to confirm they are operating correctly. General Electric products are designed for a life in excess of 20 years.

The devices are self-supervising and so require less maintenance than earlier designs of protection devices. Most problems will result in an alarm, indicating that remedial action should be taken. However, some periodic tests should be carried out to ensure that they are functioning correctly and that the external wiring is intact. It is the responsibility of the customer to define the interval between maintenance periods. If your organisation has a Preventative Maintenance Policy, the recommended product checks should be included in the regular program. Maintenance periods depend on many factors, such as:

- The operating environment
- The accessibility of the site
- The amount of available manpower
- The importance of the installation in the power system
- The consequences of failure

Although some functionality checks can be performed from a remote location, these are predominantly restricted to checking that the unit is measuring the applied currents and voltages accurately, and checking the circuit breaker maintenance counters. For this reason, maintenance checks should also be performed locally at the substation.



Caution:

Before carrying out any work on the equipment you should be familiar with the contents of the Safety Section or the Safety Guide SFTY/4LM and the ratings on the equipment's rating label.

2.1.1 ALARMS

First check the alarm status LED to see if any alarm conditions exist. If so, press the Read key repeatedly to step through the alarms.

After dealing with any problems, clear the alarms. This will clear the relevant LEDs.

2.1.2 OPTO-ISOLATORS

Check the opto-inputs by repeating the commissioning test detailed in the Commissioning chapter.

2.1.3 OUTPUT RELAYS

Check the output relays by repeating the commissioning test detailed in the Commissioning chapter.

2.1.4 MEASUREMENT ACCURACY

If the power system is energised, the measured values can be compared with known system values to check that they are in the expected range. If they are within a set range, this indicates that the A/D conversion and the calculations are being performed correctly. Suitable test methods can be found in Commissioning chapter.

Alternatively, the measured values can be checked against known values injected into the device using the test block, (if fitted) or injected directly into the device's terminals. Suitable test methods can be found in the Commissioning chapter. These tests will prove the calibration accuracy is being maintained.

2.2 REPLACING THE DEVICE

If your product should develop a fault while in service, depending on the nature of the fault, the watchdog contacts will change state and an alarm condition will be flagged. In the case of a fault, you can replace either the complete device or just the faulty PCB, identified by the in-built diagnostic software.

If possible you should replace the complete device, as this reduces the chance of damage due to electrostatic discharge and also eliminates the risk of fitting an incompatible replacement PCB. However, we understand it may be difficult to remove an installed product and you may be forced to replace the faulty PCB on-site. The case and rear terminal blocks are designed to allow removal of the complete device, without disconnecting the scheme wiring.



Caution:

Replacing PCBs requires the correct on-site environment (clean and dry) as well as suitably trained personnel.



Caution:

If the repair is not performed by an approved service centre, the warranty will be invalidated.



Caution:

Before carrying out any work on the equipment, you should be familiar with the contents of the Safety Information section of this guide or the Safety Guide SFTY/4LM, as well as the ratings on the equipment's rating label. This should ensure that no damage is caused by incorrect handling of the electronic components.



Warning:

Before working at the rear of the device, isolate all voltage and current supplying it.

Note:

The current transformer inputs are equipped with integral shorting switches which will close for safety reasons, when the terminal block is removed.

To replace the complete device:

- 1. Carefully disconnect the cables not connected to the terminal blocks (e.g. IRIG-B, fibre optic cables, earth), as appropriate, from the rear of the device.
- 2. Remove the terminal block screws using a magnetic screwdriver to minimise the risk of losing the screws or leaving them in the terminal block.
- 3. Without exerting excessive force or damaging the scheme wiring, pull the terminal blocks away from their internal connectors.
- 4. Remove the terminal block screws that fasten the device to the panel and rack. These are the screws with the larger diameter heads that are accessible when the access covers are fitted and open.
- 5. Withdraw the device from the panel and rack. Take care, as the device will be heavy due to the internal transformers.
- 6. To reinstall the device, follow the above instructions in reverse, ensuring that each terminal block is relocated in the correct position and the chassis ground, IRIG-B and fibre optic connections are replaced. The terminal blocks are labelled alphabetically with 'A' on the left hand side when viewed from the rear.

Once the device has been reinstalled, it should be re-commissioned as set out in the Commissioning chapter.



Caution:

If the top and bottom access covers have been removed, some more screws with smaller diameter heads are made accessible. Do NOT remove these screws, as they secure the front panel to the device.

Note

There are four possible types of terminal block: RTD/CLIO input, heavy duty, medium duty, and MiDOS. The terminal blocks are fastened to the rear panel with slotted or cross-head screws depending on the type of terminal block. Not all terminal block types are present on all products.

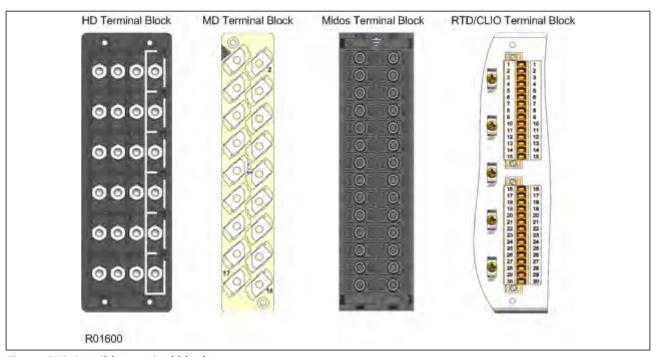


Figure 232: Possible terminal block types

2.3 REPAIRING THE DEVICE

If your product should develop a fault while in service, depending on the nature of the fault, the watchdog contacts will change state and an alarm condition will be flagged. In the case of a fault, either the complete unit or just the faulty PCB, identified by the in-built diagnostic software, should be replaced.

Replacement of printed circuit boards and other internal components must be undertaken by approved Service Centres. Failure to obtain the authorization of after-sales engineers prior to commencing work may invalidate the product warranty.

We recommend that you entrust any repairs to Automation Support teams, which are available world-wide.

2.4 REMOVING THE FRONT PANEL



Warning

Before removing the front panel to replace a PCB, you must first remove the auxiliary power supply and wait 5 seconds for the internal capacitors to discharge. You should also isolate voltage and current transformer connections and trip circuit.



Caution:

Before removing the front panel, you should be familiar with the contents of the Safety Information section of this guide or the Safety Guide SFTY/4LM, as well as the ratings on the equipment's rating label.

To remove the front panel:

- 1. Open the top and bottom access covers. You must open the hinged access covers by more than 90° before they can be removed.
- 2. If fitted, remove the transparent secondary front cover.
- 3. Apply outward pressure to the middle of the access covers to bow them and disengage the hinge lug, so the access cover can be removed. The screws that fasten the front panel to the case are now accessible.
- 4. Undo and remove the screws. The 40TE case has four cross-head screws fastening the front panel to the case, one in each corner, in recessed holes. The 60TE/80TE cases have an additional two screws, one midway along each of the top and bottom edges of the front plate.
- 5. When the screws have been removed, pull the complete front panel forward to separate it from the metal case. The front panel is connected to the rest of the circuitry by a 64-way ribbon cable.
- 6. The ribbon cable is fastened to the front panel using an IDC connector; a socket on the cable and a plug with locking latches on the front panel. Gently push the two locking latches outwards which eject the connector socket slightly. Remove the socket from the plug to disconnect the front panel.



Caution:

Do not remove the screws with the larger diameter heads which are accessible when the access covers are fitted and open. These screws hold the relay in its mounting (panel or cubicle).



Caution:

The internal circuitry is now exposed and is not protected against electrostatic discharge and dust ingress. Therefore ESD precautions and clean working conditions must be maintained at all times.

2.5 REPLACING PCBS

- 1. To replace any of the PCBs, first remove the front panel.
- 2. Once the front panel has been removed, the PCBs are accessible. The numbers above the case outline identify the guide slot reference for each printed circuit board. Each printed circuit board has a label stating the corresponding guide slot number to ensure correct relocation after removal. To serve as a reminder of the slot numbering there is a label on the rear of the front panel metallic screen.
- 3. Remove the 64-way ribbon cable from the PCB that needs replacing
- 4. Remove the PCB in accordance with the board-specific instructions detailed later in this section.

Note:

To ensure compatibility, always replace a faulty PCB with one of an identical part number.

2.5.1 REPLACING THE MAIN PROCESSOR BOARD

The main processor board is situated in the front panel. This board contains application-specific settings in its non-volatile memory. You may wish to take a backup copy of these settings. This could save time in the recommissioning process.

To replace the main processor board:

- 1. Remove front panel.
- 2. Place the front panel with the user interface face down and remove the six screws from the metallic screen, as shown in the figure below. Remove the metal plate.
- 3. Remove the two screws either side of the rear of the battery compartment recess. These are the screws that hold the main processor board in position.
- 4. Carefully disconnect the ribbon cable. Take care as this could easily be damaged by excessive twisting.
- 5. Replace the main processor board
- 6. Reassemble the front panel using the reverse procedure. Make sure the ribbon cable is reconnected to the main processor board and that all eight screws are refitted.
- 7. Refit the front panel.
- 8. Refit and close the access covers then press the hinge assistance T-pieces so they click back into the front panel moulding.
- 9. Once the unit has been reassembled, carry out the standard commissioning procedure as defined in the Commissioning chapter.

Note:

After replacing the main processor board, all the settings required for the application need to be re-entered. This may be done either manually or by downloading a settings file.

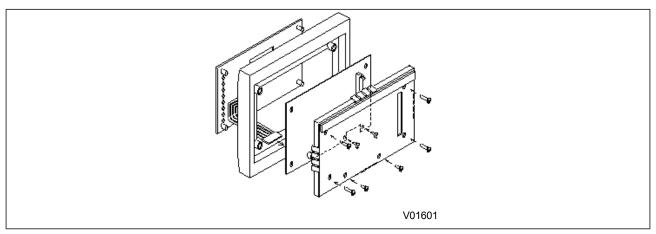


Figure 233: Front panel assembly

2.5.2 REPLACEMENT OF COMMUNICATIONS BOARDS

Most products will have at least one communications board of some sort fitted. There are several different boards available offering various functionality, depending on the application. Some products may even be fitted two boards of different types.

To replace a faulty communications board:

- 1. Remove front panel.
- 2. Disconnect all connections at the rear.
- 3. The board is secured in the relay case by two screws, one at the top and another at the bottom. Remove these screws carefully as they are not captive in the rear panel.
- 4. Gently pull the communications board forward and out of the case.
- 5. Before fitting the replacement PCB check that the number on the round label next to the front edge of the PCB matches the slot number into which it will be fitted. If the slot number is missing or incorrect, write the correct slot number on the label.

- 6. Fit the replacement PCB carefully into the correct slot. Make sure it is pushed fully back and that the securing screws are refitted.
- 7. Reconnect all connections at the rear.
- 8. Refit the front panel.
- 9. Refit and close the access covers then press the hinge assistance T-pieces so they click back into the front panel moulding.
- 10. Once the unit has been reassembled, commission it according to the Commissioning chapter.

2.5.3 REPLACEMENT OF THE INPUT MODULE

Depending on the product, the input module consists of two or three boards fastened together and is contained within a metal housing. One board contains the transformers and one contains the analogue to digital conversion and processing electronics. Some devices have an additional auxiliary transformer contained on a third board.

To replace an input module:

- 1. Remove front panel.
- 2. The module is secured in the case by two screws on its right-hand side, accessible from the front, as shown below. Move these screws carefully as they are not captive in the front plate of the module.
- 3. On the right-hand side of the module there is a small metal tab which brings out a handle (on some modules there is also a tab on the left). Grasp the handle(s) and pull the module firmly forward, away from the rear terminal blocks. A reasonable amount of force is needed due to the friction between the contacts of the terminal blocks.
- 4. Remove the module from the case. The module may be heavy, because it contains the input voltage and current transformers.
- 5. Slot in the replacement module and push it fully back onto the rear terminal blocks. To check that the module is fully inserted, make sure the v-shaped cut-out in the bottom plate of the case is fully visible.
- 6. Refit the securing screws.
- 7. Refit the front panel.
- 8. Refit and close the access covers then press the hinge assistance T-pieces so they click back into the front panel moulding.
- 9. Once the unit has been reassembled, commission it according to the Commissioning chapter.



Caution:

With non-mounted IEDs, the case needs to be held firmly while the module is withdrawn. Withdraw the input module with care as it suddenly comes loose once the friction of the terminal blocks is overcome.

Note.

If individual boards within the input module are replaced, recalibration will be necessary. We therefore recommend replacement of the complete module to avoid on-site recalibration.

2.5.4 REPLACEMENT OF THE POWER SUPPLY BOARD



Caution

Before removing the front panel, you should be familiar with the contents of the Safety Information section of this guide or the Safety Guide SFTY/4LM, as well as the ratings on the equipment's rating label.

The power supply board is fastened to an output relay board with push fit nylon pillars. This doubled-up board is secured on the extreme left hand side, looking from the front of the unit.

- 1. Remove front panel.
- 2. Pull the power supply module forward, away from the rear terminal blocks and out of the case. A reasonable amount of force is needed due to the friction between the contacts of the terminal blocks.
- 3. Separate the boards by pulling them apart carefully. The power supply board is the one with two large electrolytic capacitors.
- 4. Before reassembling the module, check that the number on the round label next to the front edge of the PCB matches the slot number into which it will be fitted. If the slot number is missing or incorrect, write the correct slot number on the label
- 5. Reassemble the module with a replacement PCB. Push the inter-board connectors firmly together. Fit the four push fit nylon pillars securely in their respective holes in each PCB.
- 6. Slot the power supply module back into the housing. Push it fully back onto the rear terminal blocks.
- 7. Refit the front panel.
- 8. Refit and close the access covers then press the hinge assistance T-pieces so they click back into the front panel moulding.
- 9. Once the unit has been reassembled, commission it according to the Commissioning chapter.

2.5.5 REPLACEMENT OF THE I/O BOARDS

There are several different types of I/O boards, which can be used, depending on the product and application. Some boards have opto-inputs, some have relay outputs and others have a mixture of both.

- 1. Remove front panel.
- 2. Gently pull the board forward and out of the case
- 3. If replacing the I/O board, make sure the setting of the link above IDC connector on the replacement board is the same as the one being replaced.
- 4. Before fitting the replacement board check the number on the round label next to the front edge of the board matches the slot number into which it will be fitted. If the slot number is missing or incorrect, write the correct slot number on the label.
- 5. Carefully slide the replacement board into the appropriate slot, ensuring that it is pushed fully back onto the rear terminal blocks.
- 6. Refit the front panel.
- 7. Refit and close the access covers then press at the hinge assistance T-pieces so they click back into the front panel moulding.
- 8. Once the unit has been reassembled, commission it according to the Commissioning chapter.

2.6 RECALIBRATION

Recalibration is not needed when a PCB is replaced, unless it is one of the boards in the input module. If any of the boards in the input module is replaced, the unit must be recalibrated.

Although recalibration is needed when a board inside the input module is replaced, it is not needed if the input module is replaced in its entirety.

Although it is possible to carry out recalibration on site, this requires special test equipment and software. We therefore recommend that the work be carried out by the manufacturer, or entrusted to an approved service centre.

2.7 CHANGING THE BATTERY

Each IED has a battery to maintain status data and the correct time when the auxiliary supply voltage fails. The data maintained includes event, fault and disturbance records and the thermal state at the time of failure.

As part of the product's continuous self-monitoring, an alarm is given if the battery condition becomes poor. Nevertheless, you should change the battery periodically to ensure reliability.

To replace the battery:

- 1. Open the bottom access cover on the front of the relay.
- 2. Gently remove the battery. If necessary, use a small insulated screwdriver.
- 3. Make sure the metal terminals in the battery socket are free from corrosion, grease and dust.
- 4. Remove the replacement battery from its packaging and insert it in the battery holder, ensuring correct polarity.
- 5. Ensure that the battery is held securely in its socket and that the battery terminals make good contact with the socket terminals.
- 6. Close the bottom access cover.



Caution:

Only use a type ½AA Lithium battery with a nominal voltage of 3.6 V and safety approvals such as UL (Underwriters Laboratory), CSA (Canadian Standards Association) or VDE (Vereinigung Deutscher Elektrizitätswerke).

Note:

Events, disturbance and maintenance records will be lost if the battery is replaced whilst the IED is de-energised.

2.7.1 POST MODIFICATION TESTS

To ensure that the replacement battery maintains the time and status data if the auxiliary supply fails, scroll across to the DATE AND TIME cell, then scroll down to Battery Status which should read Healthy.

2.7.2 BATTERY DISPOSAL

Dispose of the removed battery according to the disposal procedure for Lithium batteries in the country in which the relay is installed.

2.8 CLEANING



Warning:

Before cleaning the device, ensure that all AC and DC supplies and transformer connections are isolated, to prevent any chance of an electric shock while cleaning.

Only clean the equipment with a lint-free cloth dampened with clean water. Do not use detergents, solvents or abrasive cleaners as they may damage the product's surfaces and leave a conductive residue.

3 TROUBLESHOOTING

3.1 SELF-DIAGNOSTIC SOFTWARE

The device includes several self-monitoring functions to check the operation of its hardware and software while in service. If there is a problem with the hardware or software, it should be able to detect and report the problem, and attempt to resolve the problem by performing a reboot. In this case, the device would be out of service for a short time, during which the 'Healthy' LED on the front of the device is switched OFF and the watchdog contact at the rear is ON. If the restart fails to resolve the problem, the unit takes itself permanently out of service; the 'Healthy' LED stays OFF and watchdog contact stays ON.

If a problem is detected by the self-monitoring functions, the device attempts to store a maintenance record to allow the nature of the problem to be communicated to the user.

The self-monitoring is implemented in two stages: firstly a thorough diagnostic check which is performed on bootup, and secondly a continuous self-checking operation, which checks the operation of the critical functions whilst it is in service.

3.2 POWER-UP ERRORS

If the IED does not appear to power up, use the following to determine whether the fault is in the external wiring, auxiliary fuse, IED power supply module or IED front panel.

Test	Check	Action
1	Measure the auxiliary voltage on terminals 1 and 2. Verify the voltage level and polarity against the rating label on the front. Terminal 1 is –dc, 2 is +dc	If the auxiliary voltage is correct, go to test 2. Otherwise check the wiring and fuses in the auxiliary supply.
2	Check the LEDs and LCD backlight switch on at power-up. Also check the N/O (normally open) watchdog contact for closing.	If the LEDs and LCD backlight switch on, or the contact closes and no error code is displayed, the error is probably on the main processor board in the front panel. If the LEDs and LCD backlight do not switch on and the contact does not close, go to test 3.
3	Check the output (nominally 48 V DC)	If there is no field voltage, the fault is probably in the IED power supply module.

3.3 ERROR MESSAGE OR CODE ON POWER-UP

The IED performs a self-test during power-up. If it detects an error, a message appears on the LCD and the power-up sequence stops. If the error occurs when the IED application software is running, a maintenance record is created and the device reboots.

Test	Check	Action
1	Is an error message or code permanently displayed during power up?	If the IED locks up and displays an error code permanently, go to test 2. If the IED prompts for user input, go to test 4. If the IED reboots automatically, go to test 5.
2	Record displayed error, and then remove and re-apply IED auxiliary supply.	Record whether the same error code is displayed when the IED is rebooted. If no error code is displayed, contact the local service centre stating the error code and IED information. If the same code is displayed, go to test 3.

Test	Check	Action
3	Error Code Identification The following text messages (in English) are displayed if a fundamental problem is detected, preventing the system from booting: Bus Fail – address lines SRAM Fail – data lines FLASH Fail format error FLASH Fail checksum Code Verify Fail The following hex error codes relate to errors detected in specific IED modules:	These messages indicate that a problem has been detected on the IED's main processor board in the front panel.
3.1	0c140005/0c0d0000	Input Module (including opto-isolated inputs)
3.2	0c140006/0c0e0000	Output IED Cards
3.3	The last four digits provide details on the actual error.	Other error codes relate to hardware or software problems on the main processor board. Contact with details of the problem for a full analysis.
4	The IED displays a message for corrupt settings and prompts for the default values to be restored for the affected settings.	The power-up tests have detected corrupted IED settings. Restore the default settings to allow the power-up to complete, and then reapply the application-specific settings.
5	The IED resets when the power-up is complete. A record error code is displayed	Error 0x0E080000, programmable scheme logic error due to excessive execution time. Restore the default settings by powering up with both horizontal cursor keys pressed, then confirm restoration of defaults at the prompt using the Enter key. If the IED powers up successfully, check the programmable logic for feedback paths. Other error codes relate to software errors on the main processor board.

3.4 OUT OF SERVICE LED ON AT POWER-UP

Test	Check		Action
1	Using the IED menu, confirm the Commission Test or Test Mode setting is Enabled. If it is not Enabled, go to test 2.	If the setting Service LED	g is Enabled, disable the test mode and make sure the Out of is OFF.
2	Select the VIEW RECORDS column then view the last maintenance record from the menu.	Check for the H/W Verify Fail maintenance record. This indicates a discrepancy between the IED model number and the hardware. Examine the <i>Maint Data</i> ; cell. This indicates the causes of the failure using bit fields: Bit Meaning	
		0	The application type field in the model number does not match the software ID
		1	The application field in the model number does not match the software ID
		2	The variant 1 field in the model number does not match the software ID
		3	The variant 2 field in the model number does not match the software ID
		4	The protocol field in the model number does not match the software ID
		5	The language field in the model number does not match the software ID
		6	The VT type field in the model number is incorrect (110 V VTs fitted)
		7	The VT type field in the model number is incorrect (440 V VTs fitted)

Test	Check		Action
		8	The VT type field in the model number is incorrect (no VTs fitted)

3.5 ERROR CODE DURING OPERATION

The IED performs continuous self-checking. If the IED detects an error it displays an error message, logs a maintenance record and after a short delay resets itself. A permanent problem (for example due to a hardware fault) is usually detected in the power-up sequence. In this case the IED displays an error code and halts. If the problem was transient, the IED reboots correctly and continues operation. By examining the maintenance record logged, the nature of the detected fault can be determined.

3.5.1 BACKUP BATTERY

If the IED's self-check detects a failure of the lithium battery, the IED displays an alarm message and logs a maintenance record but the IED does not reset.

To prevent the IED from issuing an alarm when there is a battery failure, select *DATE AND TIME* then **Battery Alarm** then *Disabled*. The IED can then be used without a battery and no battery alarm message appears.

3.6 MAL-OPERATION DURING TESTING

3.6.1 FAILURE OF OUTPUT CONTACTS

An apparent failure of the relay output contacts can be caused by the configuration. Perform the following tests to identify the real cause of the failure. The self-tests verify that the coils of the output relay contacts have been energized. An error is displayed if there is a fault in the output relay board.

Test	Check	Action
1	Is the Out of Service LED ON?	If this LED is ON, the relay may be in test mode or the protection has been disabled due to a hardware verify error.
2	Examine the Contact status in the Commissioning section of the menu.	If the relevant bits of the contact status are operated, go to test 4; if not, go to test 3.
3	Examine the fault record or use the test port to check the protection element is operating correctly.	If the protection element does not operate, check the test is correctly applied. If the protection element operates, check the programmable logic to make sure the protection element is correctly mapped to the contacts.
4	Using the Commissioning or Test mode function, apply a test pattern to the relevant relay output contacts. Consult the correct external connection diagram and use a continuity tester at the rear of the relay to check the relay output contacts operate.	If the output relay operates, the problem must be in the external wiring to the relay. If the output relay does not operate the output relay contacts may have failed (the self-tests verify that the relay coil is being energized). Ensure the closed resistance is not too high for the continuity tester to detect.

3.6.2 FAILURE OF OPTO-INPUTS

The opto-isolated inputs are mapped onto the IED's internal DDB signals using the programmable scheme logic. If an input is not recognised by the scheme logic, use the *Opto I/P Status* cell in the *COMMISSION TESTS* column to check whether the problem is in the opto-input itself, or the mapping of its signal to the scheme logic functions.

If the device does not correctly read the opto-input state, test the applied signal. Verify the connections to the opto-input using the wiring diagram and the nominal voltage settings in the *OPTO CONFIG* column. To do this:

- 1. Select the nominal voltage for all opto-inputs by selecting one of the five standard ratings in the *Global Nominal V* cell.
- 2. Select Custom to set each opto-input individually to a nominal voltage.
- 3. Using a voltmeter, check that the voltage on its input terminals is greater than the minimum pick-up level (See the Technical Specifications chapter for opto pick-up levels).

If the signal is correctly applied, this indicates failure of an opto-input, which may be situated on standalone opto-input board, or on an opto-input board that is part of the input module. Separate opto-input boards can simply be replaced. If, however, the faulty opto-input board is part of the input module, the complete input module should be replaced. This is because the analogue input module cannot be individually replaced without dismantling the module and recalibration of the IED.

3.6.3 INCORRECT ANALOGUE SIGNALS

If the measured analogue quantities do not seem correct, use the measurement function to determine the type of problem. The measurements can be configured in primary or secondary terms.

- 1. Compare the displayed measured values with the actual magnitudes at the terminals.
- 2. Check the correct terminals are used.
- 3. Check the CT and VT ratios set are correct.
- 4. Check the phase displacement to confirm the inputs are correctly connected.

3.7 PSL EDITOR TROUBLESHOOTING

A failure to open a connection could be due to one or more of the following:

- The IED address is not valid (this address is always 1 for the front port)
- Password in not valid
- Communication set-up (COM port, Baud rate, or Framing) is not correct
- Transaction values are not suitable for the IED or the type of connection
- The connection cable is not wired correctly or broken
- The option switches on any protocol converter used may be incorrectly set

3.7.1 DIAGRAM RECONSTRUCTION

Although a scheme can be extracted from an IED, a facility is provided to recover a scheme if the original file is unobtainable.

A recovered scheme is logically correct but much of the original graphical information is lost. Many signals are drawn in a vertical line down the left side of the canvas. Links are drawn orthogonally using the shortest path from A to B. Any annotation added to the original diagram such as titles and notes are lost.

Sometimes a gate type does not appear as expected. For example, a single-input AND gate in the original scheme appears as an OR gate when uploaded. Programmable gates with an inputs-to-trigger value of 1 also appear as OR gates

3.7.2 PSL VERSION CHECK

The PSL is saved with a version reference, time stamp and CRC check (Cyclic Redundancy Check). This gives a visual check whether the default PSL is in place or whether a new application has been downloaded.

4 REPAIR AND MODIFICATION PROCEDURE

Please follow these steps to return an Automation product to us:

Get the Repair and Modification Return Authorization (RMA) form
 An electronic version of the RMA form is available from the following web page: www.gegridsolutions.com/contact

2. Fill in the RMA form

Fill in only the white part of the form.

Please ensure that all fields marked (M) are completed such as:

- Equipment model
- Model No. and Serial No.
- Description of failure or modification required (please be specific)
- Value for customs (in case the product requires export)
- Delivery and invoice addresses
- Contact details
- Send the RMA form to your local contact
 For a list of local service contacts worldwide, visit the following web page: www.gegridsolutions.com/contact
- 4. The local service contact provides the shipping information Your local service contact provides you with all the information needed to ship the product:
 - Pricing details
 - RMA number
 - Repair centre address

If required, an acceptance of the quote must be delivered before going to the next stage.

- 5. Send the product to the repair centre
 - Address the shipment to the repair centre specified by your local contact
 - Make sure all items are packaged in an anti-static bag and foam protection
 - Make sure a copy of the import invoice is attached with the returned unit
 - Make sure a copy of the RMA form is attached with the returned unit
 - o E-mail or fax a copy of the import invoice and airway bill document to your local contact.

CHAPTER 23

TECHNICAL SPECIFICATIONS

CHAPTER OVERVIEW 1

This chapter describes the technical specifications of the product.

This chapter contains the following sections:	
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2 INTERFACES

2.1 FRONT SERIAL PORT

Front serial port (SK1)	
Use For local connection to laptop for configuration purposes	
Standard	EIA(RS)232
Designation	SK1
Connector	9 pin D-type female connector
Isolation	Isolation to ELV level
Protocol	Courier
Constraints	Maximum cable length 15 m

2.2 DOWNLOAD/MONITOR PORT

Front download port (SK2)	
Use	For firmware downloads or monitor connection
Standard	Compatible with IEEE1284-A
Designation	SK2
Connector	25 pin D-type female connector
Isolation	Isolation to ELV level
Protocol	Proprietary
Constraints	Maximum cable length 3 m

2.3 REAR SERIAL PORT 1

Rear serial port 1 (RP1)	
Use	For SCADA communications (multi-drop)
Standard	EIA(RS)485, K-bus
Connector	General purpose block, M4 screws (2 wire)
Cable	Screened twisted pair (STP)
Supported Protocols *	Courier, IEC-60870-5-103, DNP3.0, MODBUS
Isolation	Isolation to SELV level
Constraints	Maximum cable length 1000 m
* Not all models compare all mastered and analysis anti-	

^{*} Not all models support all protocols - see ordering options

2.4 FIBRE REAR SERIAL PORT 1

Optional fibre rear serial port (RP1)		
Main Use	Serial SCADA communications over fibre	
Connector	IEC 874-10 BFOC 2.5 –(ST®) (1 each for Tx and Rx)	
Fibre type	Multimode 50/125 μm or 62.5/125 μm	
Supported Protocols	Courier, IEC870-5-103, DNP 3.0, MODBUS	
Wavelength	850 nm	

2.5 REAR SERIAL PORT 2

Optional rear serial port (RP2)		
Use	For SCADA communications (multi-drop)	
Standard	EIA(RS)485, K-bus, EIA(RS)232	
Designation	SK4	
Connector	9 pin D-type female connector	
Cable	Screened twisted pair (STP)	
Supported Protocols	Courier	
Isolation	Isolation to SELV level	
Constraints	Maximum cable length 1000 m for RS485 and K-bus, 15 m for RS232	

2.6 OPTIONAL REAR SERIAL PORT (SK5)

Optional rear serial port for teleprotection		
Use	For teleprotection in distance products	
Standard	EIA(RS)232	
Designation	SK5	
Connector	9 pin D-type female connector	
Cable	Screened twisted pair (STP)	
Supported Protocols	InterMiCOM (IM)	
Isolation	Isolation to SELV level	
Constraints	Maximum cable length 15 m	

2.7 IRIG-B (DEMODULATED)

IRIG-B Interface (Demodulated)		
Use	External clock synchronisation signal	
Standard	IRIG 200-98 format B00X	
Connector	BNC	
Cable type	50 ohm coaxial	
Isolation	Isolation to SELV level	
Constraints	Maximum cable length 10 m	
Input signal	TTL level	
Input impedance	10 k ohm at dc	
Accuracy	+/- 1 ms	

2.8 IRIG-B (MODULATED)

IRIG-B Interface (Modulated)		
Use	External clock synchronisation signal	
Standard	IRIG 200-98 format B12X	
Connector	BNC	
Cable type	50 ohm coaxial	

IRIG-B Interface (Modulated)		
Isolation	Isolation to SELV level	
Constraints	Maximum cable length 10 m	
Input signal	peak to peak, 200 mV to 20 mV	
Input impedance	6 k ohm at 1000 Hz	
Accuracy	+/- 1 ms	

2.9 REAR ETHERNET PORT COPPER

Rear Ethernet port using CAT 5/6/7 wiring		
Main Use	Substation Ethernet communications	
Standard	IEEE 802.3 10BaseT/100BaseTX	
Connector	RJ45	
Cable type	Screened twisted pair (STP)	
Isolation	1.5 kV	
Supported Protocols	IEC 61850, DNP3.0 OE	
Constraints	Maximum cable length 100 m	

2.10 REAR ETHERNET PORT FIBRE

Rear Ethernet port using fibre-optic cabling		
Main Use	Substation Ethernet communications	
Connector	IEC 874-10 BFOC 2.5 –(ST®) (1 each for Tx and Rx)	
Standard	IEEE 802.3 100 BaseFX	
Fibre type	Multimode 50/125 μm or 62.5/125 μm	
Supported Protocols	IEC 61850, DNP3.0	
Optional Redundancy Protocols Supported	Rapid spanning tree protocol (RSTP) Self-healing protocol (SHP) Dual homing protocol (DHP) Parallel Redundancy Protocol (PRP)	
Wavelength	1300 nm	

2.10.1 100 BASE FX RECEIVER CHARACTERISTICS

Parameter	Sym	Min.	Тур.	Max.	Unit
Input Optical Power Minimum at Window Edge	PIN Min. (W)		-33.5	-31	dBm avg.
Input Optical Power Minimum at Eye Center	PIN Min. (C)		-34.5	-31.8	Bm avg.
Input Optical Power Maximum	PIN Max.	-14	-11.8		dBm avg.

Conditions: TA = 0°C to 70°C

2.10.2 100 BASE FX TRANSMITTER CHARACTERISTICS

Parameter	Sym	Min.	Тур.	Max.	Unit
Output Optical Power BOL 62.5/125 µm NA = 0.275 Fibre EOL	РО	-19 -20	-16.8	-14	dBm avg.
Output Optical Power BOL 50/125 µm NA = 0.20 Fibre EOL	РО	-22.5 -23.5	-20.3	-14	dBm avg.
Optical Extinction Ratio				10 -10	% dB
Output Optical Power at Logic "0" State	PO			-45	dBm avg.

Conditions: TA = 0°C to 70°C

3 PERFORMANCE OF CURRENT PROTECTION FUNCTIONS

3.1 TRANSIENT OVERREACH AND OVERSHOOT

Additional tolerance due to increasing X/R ratios	+/-5% over the X/R ratio of 1 to 90
Overshoot of overcurrent elements	< 30 ms

3.2 PHASE OVERCURRENT PROTECTION

Accuracy		
IDMT pick-up	1.05 x Setting +/-5%	
DT pick-up	Setting +/-5%	
Drop-off (IDMT and DT)	0.98 x setting +/-5%	
IDMT operate	+/-5% of expected operating time or 40 ms, whichever is greater*	
IEEE reset	+/-5% or 40 ms, whichever is greater	
DT operate	+/-2% of setting or 40 ms, whichever is greater	
DT reset	Setting +/-5%	
Repeatability	<5%	
Characteristic UK	IEC 60255-3 1998	
Characteristic US	IEEE C37.112 1996	

Note:

*Reference conditions: TMS = 1, TD = 7, I > 1 = 1A, operating range = 2-20In

3.2.1 PHASE OVERCURRENT DIRECTIONAL PARAMETERS

Accuracy	
Directional boundary pickup (RCA +/-90%)	+/-2°
Directional boundary hysteresis	< 2°
Directional boundary repeatability	<2%

3.3 VOLTAGE DEPENDENT OVERCURRENT PROTECTION

Accuracy	
Voltage threshold pick-up	Setting +/- 5%
Voltage threshold drop-off	1.05 x setting +/- 5%
Current threshold pick-up	Formula +/- 5%
Current threshold drop-off	0.95 x formula +/- 5%

Note:

These specifications apply to both VCO and VRO

3.4 EARTH FAULT PROTECTION

Accuracy - Measured	
IDMT pick-up	1.05 x setting +/-5%
DT pick-up	Setting +/-5%
Drop-off (IDMT and DT)	0.98 x setting +/-5%
IDMT Operate	+/-5% or 40 ms, whichever is greater*
IEEE reset	+/-5% or 40 ms, whichever is greater
Pick-up and drop-off repeatability	< 2.5%
DT operate	+/-2% or 50 ms, whichever is greater
DT reset	+/-5%

Accuracy - Derived	
IDMT pick-up	1.05 x setting +/-5%
DT pick-up	Setting +/-5%
Drop-off (IDMT and DT)	0.95 x setting +/-5%
IDMT operate	+/-5% or 40 ms, whichever is greater*
IEEE reset	+/-10% or 40 ms, whichever is greater
Pick-up and drop-off repeatability	< 5%
DT operate time	+/-2% or 50 ms, whichever is greater
DT reset time	+/-2% or 50 ms, whichever is greater

Note:

Reference conditions: TMS = 1, TD = 1, IN > setting = 1 A with operating range of 2-20In = 1

3.4.1 EARTH FAULT DIRECTIONAL PARAMETERS

Zero Sequence Polarising accuracy	
Directional boundary pick-up (RCA +/- 90°)	+/-2°
Hysteresis	<3°
VN> pick-up	Setting+/-10%
VN> drop-off	0.9 × Setting +/-10%

Negative Sequence Polarising accuracy	
Directional boundary pick-up (RCA +/- 90°)	+/-2°
Hysteresis	<3°
VN2> pick-up	Setting+/-10%
VN2> drop-off	0.9 x Setting +/-10%
IN2> pick-up	Setting+/-10%
IN2> drop-off	0.9 x Setting +/-10%

3.5 SENSITIVE EARTH FAULT PROTECTION

IDMT pick-up	1.05 × Setting +/-5%
DT Pick-up	Setting +/- 5%
Drop-off (IDMT + DT)	0.95 x Setting +/-5%
IDMT operate	+/- 5% or 40 ms, whichever is greater
DT operate	+/- 2% or 60 ms, whichever is greater
DT reset	Setting +/- 5%
Repeatability	+/- 5%

Note:

Reference conditions: TMS = 1, TD = 1, IN> setting = 1 A with operating range of 2-20In.

3.5.1 SEF DIRECTIONAL PARAMETERS

Wattmetric SEF accuracy	
Pick-up for P = 0 W	ISEF > +/-5% or 5 mA
Pick-up for P > 0 W	P>+/-5%
Drop-off for P = 0 W	0.95 x ISEF> +/- 5% or 5 mA
Drop-off for P > 0 W	0.9 x P> +/- 5% or 5 mA
Boundary accuracy	+/-5% with hysteresis < 1°
Repeatability	+/- 5%

SEF CosΦ accuracy	
Pick-up	Setting +/-5% for angles RCA+/-60°
Drop-off	0.9 x setting
Repeatability	+/- 2%

SEF SinΦ accuracy	
Pick-up	Setting +/-5% for angles RCA+/-60° to RCA+/-90°
Drop-off	0.9 x setting
Repeatability	+/- 2%

3.6 RESTRICTED EARTH FAULT PROTECTION

High Impedance and Low Impedance	
Pick-up	Setting formula +/- 5%
Drop-off	0.8 x Setting formula +/-5%
Operating time	< 60 ms
High set pick-up	Setting +/- 10%
High set operating time	< 30 ms
Repeatability	< 15%

3.7 NEGATIVE SEQUENCE OVERCURRENT PROTECTION

IDMT pick-up	1.05 × Setting +/-5%
DT pick-up	Setting +/- 5%
Drop-off (IDMT + DT)	0.95 x Setting +/-5%
IDMT operate	+/- 5% or 40 ms, whichever is greater
DT operate	+/- 2% or 60 ms, whichever is greater
DT Reset	Setting +/- 5%

3.7.1 NPSOC DIRECTIONAL PARAMETERS

Directional boundary pick-up (RCA +/-90%)	+/-2°
Directional boundary hysteresis	< 2°
Directional boundary repeatability	< 2%

3.8 CIRCUIT BREAKER FAIL AND UNDERCURRENT PROTECTION

I< Pick-up	Setting +/- 5% or 20 mA, whichever is greater
I< Drop-off	100% of setting +/- 5% or 20 mA, whichever is greater
Timers	+/- 2% or 50 ms, whichever is greater
Reset time	< 35 ms

3.9 BROKEN CONDUCTOR PROTECTION

Pick-up	Setting +/- 2.5%
Drop-off	0.95 x Setting +/- 2.5%
DT operate	+/- 2% or 40 ms, whichever is greater
Reset time	<25 ms

3.10 THERMAL OVERLOAD PROTECTION

Thermal alarm pick-up	Calculated trip time +/- 10%
Thermal overload pick-up	Calculated trip time +/- 10%
Cooling time accuracy	+/- 15% of theoretical
Repeatability	<5%

Note.

Operating time measured with applied current of 20% above thermal setting.

3.11 COLD LOAD PICKUP PROTECTION

l> Pick-up	Setting +/- 1.5%
IN> Pick-up	Setting +/- 1.5%
l> Drop-off	0.95 x Setting +/- 1.5%
IN> Drop-off	0.95 x Setting +/- 1.5%
DT operate	+/- 0.5% or 40 ms, whichever is greater
Repeatability	+/- 1%

3.12 SELECTIVE OVERCURRENT PROTECTION

Fast Block operation	< 25 ms
Fast Block reset	< 30 ms
Time delay	Setting +/- 2% or 20 ms, whichever is greater

3.13 VOLTAGE DEPENDENT OVERCURRENT PROTECTION

VCO/VRO threshold pick-up	Setting +/- 5%
Overcurrent pick-up	K-factor x setting +/- 5%
VCO/VRO threshold drop-off	1.05 x setting +/- 5%
Overcurrent drop-off	0.95(K-factor x setting) +/- 5%
Operating time	+/- 5% or 60 ms, whichever is greater
Repeatability	< 5%

3.14 NEUTRAL ADMITTANCE PROTECTION

YN, BN, GN measurements	+/-5%
YN, BN, GN pick-up	Setting +/-5%
YN, BN, GN drop-off	0.85 x setting +/-5%
DT operate	+/- 2% or 50 ms, whichever is greater
DT reset	Setting +/- 5%
Disengagement	< 40 ms
Directional boundary accuracy	+/- 2°
VN	Setting +/-5%

4 PERFORMANCE OF VOLTAGE PROTECTION FUNCTIONS

4.1 UNDERVOLTAGE PROTECTION

Pick-up (IDMT and DT)	Setting +/- 5%
Drop-off (IDMT and DT)	1.02 x Setting +/-5%
IDMT operate	+/- 5% or 50 ms, whichever is greater
DT operate	+/- 2% or 50 ms, whichever is greater
DT reset	< 75 ms
Repeatability	< 1%

4.2 OVERVOLTAGE PROTECTION

Pick-up (IDMT and DT)	Setting +/- 5%
Drop-off (IDMT and DT)	0.98 x Setting +/-5%
IDMT operate	+/- 5% or 50 ms, whichever is greater
DT operate	+/- 2% or 50 ms, whichever is greater
DT reset	< 75 ms
Repeatability	< 1%

4.3 RESIDUAL OVERVOLTAGE PROTECTION

IDMT pick-up	1.05 x Setting +/- 5%
DT pick-up	Setting +/- 5%
Drop-off (IDMT and DT)	0.95 x Setting +/-5%
IDMT operate	+/- 5% or 65 ms, whichever is greater
DT operate	+/- 2% or 60 ms or whichever is greater
DT reset	< 35 ms
Repeatability	< 10%

4.4 NEGATIVE SEQUENCE VOLTAGE PROTECTION

Pick-up	Setting +/- 5%
Drop-off	0.95 x Setting +/-5%
DT operate	+/- 2% or 50 ms, whichever is greater
Repeatability	< 5%

4.5 RATE OF CHANGE OF VOLTAGE PROTECTION

Accuracy for 110 V VT	
Tolerance	1% or 0.07, whichever is greater
Pick-up	Setting +/- tolerance
Drop-off for positive direction	(Setting – 0.07)+/- tolerance
Drop-off for negative direction	(Setting + 0.07)+/- tolerance
Operating time at 50 Hz	(Average cycle x 20) +60 ms
Reset time at 50 Hz	40 ms

5 PERFORMANCE OF FREQUENCY PROTECTION FUNCTIONS

5.1 BASIC OVERFREQUENCY PROTECTION

Pick-up	Setting +/- 5 mHz
Drop-off	(Setting - 25 mHz) +/- 5mHz
DT operate*	+/- 2% or 50 ms, whichever is greater

Note

5.2 BASIC UNDERFREQUENCY PROTECTION

Pick-up	Setting +/- 5 mHz
Drop-off	(Setting + 25 mHz) +/- 5mHz
DT operate*	+/- 2% or 50 ms, whichever is greater

Note:

5.3 ADVANCED OVERFREQUENCY PROTECTION

Accuracy	
Pick-up	Setting +/- 5 mHz
Drop-off	(Setting - 25 mHz) +/- 5 mHz
Operating timer	+/- 2% or 50 ms, whichever is greater

Operating and Reset time	
Operating time (Fs/Ff ratio less than 2)	<125 ms
Operating time (Fs/Ff ratio between 2 and 30)	<150 ms
Operating time (Fs/Ff ratio greater than 30)	<200 ms
Reset time	<200 ms

Reference conditions: Tested using step changed in frequency with Freq. Av Cycles setting = 0 and no intentional time delay.

Fs = start frequency - frequency setting

Ff = frequency setting - end frequency

^{*}The operating time also includes the time to track the frequency at 20 Hz per second

^{*}The operating time also includes the time to track the frequency at 20 Hz per second

5.4 ADVANCED UNDERFREQUENCY PROTECTION

Accuracy	
Pick-up	Setting +/- 5 mHz
Drop-off	(Setting + 25 mHz) +/- 5 mHz
Operating timer	+/- 2% or 50 ms, whichever is greater

Operating and Reset time	
Operating time (Fs/Ff ratio less than 2)	<125 ms
Operating time (Fs/Ff ratio between 2 and 6)	<160 ms
Operating time (Fs/Ff ratio greater than 6)	<230 ms
Reset time	<200 ms

Reference conditions: Tested using step changed in frequency with Freq. Av Cycles setting = 0 and no intentional time delay.

Fs = start frequency - frequency setting

Ff = frequency setting - end frequency

5.5 SUPERVISED RATE OF CHANGE OF FREQUENCY PROTECTION

Accuracy	
Pick-up (f)	Setting +/- 10 mHz
Pick-up (df/dt)	Setting +/- 3% or +/- 10 mHz/s, whichever is greater
Drop-off (f, underfrequency)	(Setting + 20 mHz) +/- 10 mHz
Drop-off (f, overfrequency)	(Setting - 20 mHz) +/- 10 mHz
Drop-off (df/dt, falling, for settings between 10 mHz/s and 100 mHz/s)	(Setting + 5 mHz/s) +/- 10 mHz/s
Drop-off (df/dt, falling, for settings greater than 100 mHz/s)	(Setting + 50 mHz/s) +/- 5% or +/- 55 mHz/s, whichever is greater
Drop-off (df/dt, rising, for settings between 10 mHz/s and 100 mHz/s)	(Setting - 5 mHz/s) +/- 10 mHz/s
Drop-off (df/dt, rising, for settings greater than 100 mHz/s)	(Setting - 50 mHz/s) +/- 5% or +/- 55 mHz/s, whichever is greater

Operating and Reset time	
Instantaneous operating time (Freq AvCycles setting = 0)	<125 ms
Reset time (df/dt AvCycles setting = 0)	<400 ms

5.6 INDEPENDENT RATE OF CHANGE OF FREQUENCY PROTECTION

Accuracy	
Pick-up (df/dt)	Setting +/- 3% or +/- 10 mHz/s, whichever is greater
Drop-off (df/dt, falling, for settings between 10 mHz/s and 100 mHz/s)	(Setting + 5 mHz/s) +/- 10 mHz/s

Accuracy	
Drop-off (df/dt, falling, for settings greater than 100 mHz/s)	(Setting + 50 mHz/s) +/- 5% or +/- 55 mHz/s, whichever is greater
Drop-off (df/dt, rising, for settings between 10 mHz/s and 100 mHz/s)	(Setting - 5 mHz/s) +/- 10 mHz/s
Drop-off (df/dt, rising, for settings greater than 100 mHz/s)	(Setting - 50 mHz/s) +/- 5% or +/- 55 mHz/s, whichever is greater
Operating timer	+/- 2% or 50 ms, whichever is greater

Operating and Reset time	
Operating time (for ramps 2 x seting or greater)	<200 ms
Operating time (for ramps 1.3 x seting or greater)	<300 ms
Reset time time (df/dt AvCycles setting = 0 for df/dt settings greater than 0.1 Hz/s and no intentional time delay)	<250 ms

Referecne Conditions: Tested with df/dt Average Cycles = 0 for df/dt settings greater than 0.1 Hz/s, and no intentional time delay.

5.7 AVERAGE RATE OF CHANGE OF FREQUENCY PROTECTION

Accuracy	
Pick-up (f)	Setting +/- 10 mHz
Pick-up (Df/Dt)	Setting +/- 100 mHz/s
Drop-off (falling)	(Setting + 20 mHz) +/- 10 mHz
Drop-off (rising)	(Setting - 20 mHz) +/- 10 mHz
Operating timer	+/- 2% or 30 ms, whichever is greater

Operating time	
Operating time (Freq. Av Cycles setting = 0)	<125 ms

Reference conditions: To maintain accuracy, the minimum time delay setting should be:

Dt> $0.375 \times Df + 0.23$ (for Df setting <1 Hz)

Dt> $0.156 \times Df + 0.47$ (for Df setting >= 1 Hz)

5.8 LOAD RESTORATION

Pick-up	Setting +/- 2.5%
Drop-off	0.95% x Setting +/- 2.5%
Restoration timer	+/- 2% or 50 ms, whichever is greater
Holding timer	+/- 2% or 50 ms, whichever is greater

6 POWER PROTECTION FUNCTIONS

6.1 OVERPOWER / UNDERPOWER PROTECTION

Pick-up	Setting +/- 10%
Reverse/Overpower Drop-off	0.95 x Setting +/- 10%
Low forward power Drop-off	1.05 x Setting +/- 10%
Angle variation pick-up	+/- 2°
Angle variation drop-off	+/- 2.5°
Operating time	+/- 2% or 50 ms, whichever is greater
Repeatability	< 5%
Disengagement time	<50 ms
treset	+/- 5%
Instantaneous operating time	< 50 ms

6.2 SENSITIVE POWER PROTECTION

Pick-up	Setting +/- 10%
Reverse/Overpower Drop-off	0.9 x Setting +/- 10%
Low forward power Drop-off	1.1 x Setting +/- 10%
Angle variation pick-up	+/- 2°
Angle variation drop-off	+/- 2.5°
Operating time	+/- 2% or 50 ms, whichever is greater
Repeatability	< 5%
Disengagement time	<50 ms
treset	+/- 5%
Instantaneous operating time	< 50 ms

7 PERFORMANCE OF MONITORING AND CONTROL FUNCTIONS

7.1 VOLTAGE TRANSFORMER SUPERVISION

Fast block operation	< 1 cycle
Fast block reset	< 1.5 cycles
Time delay	+/- 2% or 20 ms, whichever is greater

7.2 STANDARD CURRENT TRANSFORMER SUPERVISION

IN> Pick-up	Setting +/- 5%
VN< Pick-up	Setting +/- 5%
IN> Drop-off	0.9 x setting +/- 5%
VN< Drop-off	$1.05 \times \text{setting} + /-5\% \text{ or } 1 \text{ V, whichever is greater}$
Time delay operation	Setting +/-2% or 20 ms, whichever is greater
CTS block operation	< 1 cycle
CTS reset	< 35 ms

7.3 CB STATE AND CONDITION MONITORING

Accuracy	
Timers	+/- 40 ms or 2%, whichever is greater
Broken current accuracy	+/- 5%
Reset time	< 30 ms

7.4 PSL TIMERS

Output conditioner timer	Setting +/- 2% or 50 ms, whichever is greater
Dwell conditioner timer	Setting +/- 2% or 50 ms, whichever is greater
Pulse conditioner timer	Setting +/- 2% or 50 ms, whichever is greater

8 MEASUREMENTS AND RECORDING

8.1 GENERAL

General Measurement Accuracy	
General measurement accuracy	Typically +/- 1%, but +/- 0.5% between 0.2 - 2 In/Vn
Phase	0° to 360° +/- 0.5%
Current (0.05 to 3 ln)	+/- 1.0% of reading, or 4mA (1A input), or 20mA (5A input)
Voltage (0.05 to 2 Vn)	+/- 1.0% of reading
Frequency (45 to 65 Hz)	+/- 0.025 Hz
Power (W) (0.2 to 2 Vn and 0.05 to 3 In)	+/- 5.0% of reading at unity power factor
Reactive power (Vars) (0.2 to 2 Vn and 0.05 to 3 ln)	+/- 5.0% of reading at zero power factor
Apparent power (VA) (0.2 to 2 Vn and 0.05 to 3 In)	+/- 5.0% of reading
Energy (Wh) (0.2 to 2 Vn and 0.2 to 3 In)	+/- 5.0% of reading at unity power factor
Energy (Varh) (0.2 to 2 Vn and 0.2 to 3In)	+/- 5.0% of reading at zero power factor

8.2 DISTURBANCE RECORDS

Disturbance Records Measurement Accuracy	
Minimum record duration	0.1 s
Maximum record duration	10.5 s
Minimum number of records at 10.5 seconds	8
Magnitude and relative phases accuracy	+/- 5% of applied quantities
Duration accuracy	+/- 2%
Trigger position accuracy	+/- 2% (minimum Trigger 100 ms)

8.3 EVENT, FAULT AND MAINTENANCE RECORDS

Event, Fault & Maintenance Records	
Record location	Battery-backed memory
Viewing method	Front panel display or Settings Application Software
Extraction method	Extracted via the front serial port
Number of Event records	Up to 512 time tagged event records (newest overwrites oldest)
Number of Fault Records	Up to 5
Number of Maintenance Records	Up to 10
Event time stamp resolution	1 ms

8.4 FAULT LOCATOR

Accuracy	
Fault Location	+/- 3.5% of line length up to SIR 30
Fault Location	Reference conditions: solid fault applied on line

9 RATINGS

9.1 AC MEASURING INPUTS

AC Measuring Inputs	
Nominal frequency	50 Hz or 60 Hz (settable)
Operating range	45 to 65 Hz
Phase rotation	ABC or CBA

9.2 CURRENT TRANSFORMER INPUTS

AC Current Inputs	
Nominal current (In)	1A or 5A
Nominal burden per phase	< 0.2 VA at In
AC current thermal withstand (5A input)	20 A (continuous operation) 150 A (for 10 s) 500 A (for 1 s)
AC current thermal withstand (1A input)	4 A (continuous operation) 30 A (for 10 s) 100 A (for 1 s)
Linearity	Linear up to 64 × In (non-offset)

9.3 **VOLTAGE TRANSFORMER INPUTS**

AC Voltage Inputs	
Nominal voltage	100 V to 120 V
Nominal burden per phase	< 0.1 VA at Vn
Thermal withstand	2 x Vn (continuous operation) 2.6 x Vn (for 10 seconds)
Linearity	Linear up to 200 V (100/120 V supply) Linear up to 800 V (380/400 V supply)

9.4 AUXILIARY SUPPLY VOLTAGE

	Cortec option (DC only) 24 to 48 V DC Cortec option (rated for AC or DC operation)
Nominal operating range	48 to 110 V DC 40 to 100 V AC rms
	Cortec option (rated for AC or DC operation) 110 to 250 V DC 100 to 240 V AC rms

Maximum operating range	Cortec option (DC only) 19 to 65 V DC Cortec option (rated for AC or DC operation) 37 to 150 V DC 32 to 110 V AC rms Cortec option (rated for AC or DC operation) 87 to 300 V DC 80 to 265 V AC rms
Frequency range for AC supply	45 to 65 Hz
Ripple	<15% for a DC supply (compliant with IEC 60255-11:2013)
Power up time	< 11 seconds

9.5 NOMINAL BURDEN

Quiescent burden	11 W
2nd rear communications port	1.25 W
Each relay output burden	0.13 W per output relay
Each opto-input burden (24 – 27 V)	0.065 W max
Each opto-input burden (30 – 34 V)	0.065 W max
Each opto-input burden (48 – 54 V)	0.125 W max
Each opto-input burden (110 – 125 V)	0.36 W max
Each opto-input burden (220 – 250 V)	0.9 W max

9.6 POWER SUPPLY INTERRUPTION

Standard	IEC 60255-26:2013 (DC and AC)
24-48V DC SUPPLY 100% interruption without de-energising	20 ms at 24 V (half and full load) 50 ms at 36 V (half and full load) 100 ms at 48 V (half and full load)
48-110V DC SUPPLY 100% interruption without de-energising	20 ms at 37V (half and full load) 50 ms at 60 V (half and full load) 100 ms at 72 V (half load) 100 ms at 85 V (full load) 200 ms at 110 V (half and full load)
110-250V DC SUPPLY 100% interruption without de-energising	20 ms at 87 V (half load) 50 ms at 110 V (half load) 50 ms at 98 V (full load) 100 ms at 160 V (half load) 100 ms at 135 V (full load) 200 ms at 210 V (half load) 200 ms at 174 V (full load)
40-100V AC SUPPLY 100% voltage dip without de-energising	50 ms at 32 V (half load) 10 ms at 32 V (full load)
100-240V AC SUPPLY 100% voltage dip without de-energising	50 ms at 80 V (full and half load)

Note:

Maximum loading = all inputs/outputs energised.

Note:

Quiescent or 1/2 loading = 1/2 of all inputs/outputs energised.

9.7 BATTERY BACKUP

Location	Front panel
Туре	1/2 AA, 3.6V Lithium Thionyly Chloride
Battery reference	LS14250
Lifetime	> 10 years (IED energised for 90% of the time)

10 INPUT / OUTPUT CONNECTIONS

10.1 ISOLATED DIGITAL INPUTS

Opto-isolated digital inputs (opto-inputs)	
Compliance	ESI 48-4
Rated nominal voltage	24 to 250 V dc
Operating range	19 to 265 V dc
Withstand	300 V dc
Recognition time with half-cycle ac immunity filter removed	< 2 ms
Recognition time with filter on	< 12 ms

10.2 NOMINAL PICKUP AND RESET THRESHOLDS

Nominal battery voltage	Logic levels: 60-80% DO/PU	Logic Levels: 50-70% DO/PU	Logic Levels: 58-75% DO/PU
24/27 V	Logic 0 < 16.2V, Logic 1 > 19.2V	Logic 0 <12V, Logic 1 > 16.8V	Logic 0 <15.7V, Logic 1 > 18V
30/34	Logic 0 < 20.4V, Logic 1 > 24V	Logic 0 < 15V, Logic 1 > 21V	Logic 0 < 19.7V, Logic 1 > 22.5V
48/54	Logic 0 < 32.4V, Logic 1 > 38.4V	Logic 0 < 24V, Logic 1 > 33.6V	Logic 0 < 31.3V, Logic 1 > 36V
110/125	Logic 0 < 75V, Logic 1 > 88V	Logic 0 < 55.V, Logic 1 > 77V	Logic 0 < 72.5V, Logic 1 > 82.5V
220/250	Logic 0 < 150V, Logic 1 > 176V	Logic 0 < 110V, Logic 1 > 154V	Logic 0 < 145V, Logic 1 > 165V

Note:

Filter is required to make the opto-inputs immune to induced AC voltages.

10.3 STANDARD OUTPUT CONTACTS

Compliance	In accordance with IEC 60255-1:2009
Use	General purpose relay outputs for signalling, tripping and alarming
Rated voltage	300 V
Maximum continuous current	10 A
Short duration withstand carry	30 A for 3 s 250 A for 30 ms
Make and break, dc resistive	50 W
Make and break, dc inductive	62.5 W (L/R = 50 ms)
Make and break, ac resistive	2500 VA resistive (cos phi = unity)
Make and break, ac inductive	2500 VA inductive (cos phi = 0.7)
Make and carry, dc resistive	30 A for 3 s, 10000 operations (subject to the above limits)
Make, carry and break, dc resistive	4 A for 1.5 s, 10000 operations (subject to the above limits)
Make, carry and break, dc inductive	0.5 A for 1 s, 10000 operations (subject to the above limits)
Make, carry and break ac resistive	30 A for 200 ms, 2000 operations (subject to the above limits)
Make, carry and break ac inductive	10 A for 1.5 s, 10000 operations (subject to the above limits)

Loaded contact	1000 operations min.
Unloaded contact	10000 operations min.
Operate time	< 5 ms
Reset time	< 10 ms

10.4 HIGH BREAK OUTPUT CONTACTS

Compliance	In accordance with IEC 60255-1:2009
Use	For applications requiring high rupture capacity
Rated voltage	300 V
Maximum continuous current	10 A DC
Short duration withstand carry	30 A DC for 3 s 250 A for 30 ms
Make and break, dc resistive	7500 W
Make and break, dc inductive	2500 W (L/R = 50 ms)
Make and carry, dc resistive	30 A for 3 s, 10000 operations (subject to the above limits)
Make, carry and break, dc resistive	30 A for 3 s, 5000 operations (subject to the above limits) 30 A for 200 ms, 10000 operations (subject to the above limits)
Make, carry and break, dc inductive	10 A for 40 ms, 10000 operations (subject to the above limits) 10 a for 20 ms (250V, 4 shots per second)
Loaded contact	10,000 operations minimum.
Unloaded contact	100,000 operations minimum.
Operate time	< 0.2 ms
Reset time	< 8 ms
MOV Protection	Maximum voltage 330 V DC

10.5 WATCHDOG CONTACTS

Use	Non-programmable contacts for relay healthy/relay fail indication
Breaking capacity, dc resistive	30 W
Breaking capacity, dc inductive	15 W (L/R = 40 ms)
Breaking capacity, ac inductive	375 VA inductive (cos phi = 0.7)

11 MECHANICAL SPECIFICATIONS

11.1 PHYSICAL PARAMETERS

Case Types*	40TE 60TE 80TE
Weight (40TE case)	7 kg - 8 kg (depending on chosen options)
Weight (60TE case)	9 kg - 12 kg (depending on chosen options)
Weight (80TE case)	13 kg - 16 kg (depending on chosen options)
Dimensions in mm (w \times h \times l) (40TE case)	W: 206.0 mm H: 177.0 mm D: 243.1 mm
Dimensions in mm (w \times h \times l) (60TE case)	W: 309.6 mm H: 177.0 mm D: 243.1 mm
Dimensions in mm (w \times h \times l) (80TE case)	W 413.2 mm H 177.0 mm D 243.1 mm
Mounting	Panel, rack, or retrofit

Note:

*Case size is product dependent.

11.2 ENCLOSURE PROTECTION

Against dust and dripping water (front face)	IP52 as per IEC 60529:2002
Protection against dust (whole case)	IP50 as per IEC 60529:2002
Protection for sides of the case (safety)	IP30 as per IEC 60529:2002
Protection for rear of the case (safety)	IP10 as per IEC 60529:2002

11.3 MECHANICAL ROBUSTNESS

Vibration test per EN 60255-21-1:1996	Response: class 2, Endurance: class 2
Shock and bump immunity per EN 60255-21-2:1995	Shock response: class 2, Shock withstand: class 1, Bump withstand: class 1
Seismic test per EN 60255-21-3: 1995	Class 2

11.4 TRANSIT PACKAGING PERFORMANCE

Primary packaging carton protection	ISTA 1C
Vibration tests	3 orientations, 7 Hz, amplitude 5.3 mm, acceleration 1.05g
Drop tests	10 drops from 610 mm height on multiple carton faces, edges and corners

12 TYPE TESTS

12.1 INSULATION

Compliance	IEC 60255-27: 2005
Insulation resistance	> 100 M ohm at 500 V DC (Using only electronic/brushless insulation tester)

12.2 CREEPAGE DISTANCES AND CLEARANCES

Compliance	IEC 60255-27: 2005
Pollution degree	3
Overvoltage category	
Impulse test voltage (not RJ45)	5 kV
Impulse test voltage (RJ45)	1 kV

12.3 HIGH VOLTAGE (DIELECTRIC) WITHSTAND

IEC Compliance	IEC 60255-27: 2005
Between all independent circuits	2 kV ac rms for 1 minute
Between independent circuits and protective earth conductor terminal	2 kV ac rms for 1 minute
Between all case terminals and the case earth	2 kV ac rms for 1 minute
Across open watchdog contacts	1 kV ac rms for 1 minute
Across open contacts of changeover output relays	1 kV ac rms for 1 minute
Between all RJ45 contacts and protective earth	1 kV ac rms for 1 minute
Between all screw-type EIA(RS)485 contacts and protective earth	1 kV ac rms for 1 minute
ANSI/IEEE Compliance	ANSI/IEEE C37.90-2005
Across open contacts of normally open output relays	1.5 kV ac rms for 1 minute
Across open contacts of normally open changeover output relays	1 kV ac rms for 1 minute
Across open watchdog contacts	1 kV ac rms for 1 minute

12.4 IMPULSE VOLTAGE WITHSTAND TEST

Compliance	IEC 60255-27: 2005
Between all independent circuits	Front time: 1.2 µs, Time to half-value: 50 µs, Peak value: 5 kV, 0.5 J
Between terminals of all independent circuits	Front time: 1.2 µs, Time to half-value: 50 µs, Peak value: 5 kV, 0.5 J
Between all independent circuits and protective earth conductor terminal	Front time: 1.2 µs, Time to half-value: 50 µs, Peak value: 5 kV, 0.5 J

Note:

Exceptions are communications ports and normally-open output contacts, where applicable.

13 ENVIRONMENTAL CONDITIONS

13.1 AMBIENT TEMPERATURE RANGE

Compliance	IEC 60255-27: 2005
Test Method	IEC 60068-2-1:2007 and IEC 60068-2-2 2007
Operating temperature range	-25°C to +55°C (continuous)
Storage and transit temperature range	-25°C to +70°C (continuous)

13.2 TEMPERATURE ENDURANCE TEST

Temperature Endurance Test	
Test Method	IEC 60068-2-1: 1993 and 60068-2-2: 2007
Operating temperature range	-40°C (96 hours) +70°C (96 hours)
Storage and transit temperature range	-40°C (96 hours) +70°C (96 hours)

13.3 AMBIENT HUMIDITY RANGE

Compliance	IEC 60068-2-78: 2001 and IEC 60068-2-30: 2005
Durability	56 days at 93% relative humidity and +40°C
Damp heat cyclic	six (12 + 12) hour cycles, 93% RH, +25 to +55°C

13.4 CORROSIVE ENVIRONMENTS

Compliance	IEC 60068-2-42: 2003, IEC 60068-2-43: 2003
Industrial corrosive environment/poor environmental control, Sulphur Dioxide	21 days exposure to elevated concentrations (25ppm) of SO_2 at 75% relative humidity and +25°C
Industrial corrosive environment/poor environmental control, Hydrogen Sulphide	21 days exposure to elevated concentrations (10ppm) of $\rm H_2S$ at 75% relative humidity and +25°C
Salt mist	IEC 60068-2-52: 1996 KB severity 3

14 ELECTROMAGNETIC COMPATIBILITY

14.1 1 MHZ BURST HIGH FREQUENCY DISTURBANCE TEST

Compliance	IEC 60255-22-1: 2008, Class III, IEC 60255-26:2013
Common-mode test voltage (level 3)	2.5 kV
Differential test voltage (level 3)	1.0 kV

14.2 DAMPED OSCILLATORY TEST

Compliance	EN61000-4-18: 2011: Level 3, 100 kHz and 1 MHz. Level 4: 3 MHz, 10 MHz and 30 MHz, IEC 60255-26:2013
Common-mode test voltage (level 3)	2.5 kV
Common-mode test voltage (level 4)	4.0 kV
Differential mode test voltage	1.0 kV

14.3 IMMUNITY TO ELECTROSTATIC DISCHARGE

Compliance	IEC 60255-22-2: 2009 Class 3 and Class 4, IEC 60255-26:2013
Class 4 Condition	15 kV discharge in air to user interface, display, and exposed metalwork
Class 3 Condition	8 kV discharge in air to all communication ports

14.4 ELECTRICAL FAST TRANSIENT OR BURST REQUIREMENTS

Compliance	IEC 60255-22-4: 2008 and EN61000-4-4:2004. Test severity level III and IV, IEC 60255-26:2013
Applied to communication inputs	Amplitude: 2 kV, burst frequency 5 kHz and 100 KHz (level 4)
Applied to power supply and all other inputs except for communication inputs	Amplitude: 4 kV, burst frequency 5 kHz and 100 KHz (level 4)

14.5 SURGE WITHSTAND CAPABILITY

Compliance	IEEE/ANSI C37.90.1: 2002
Condition 1	4 kV fast transient and 2.5 kV oscillatory applied common mode and differential mode to opto inputs, output relays, CTs, VTs, power supply
Condition 2	4 kV fast transient and 2.5 kV oscillatory applied common mode to communications, IRIG-B $$

14.6 SURGE IMMUNITY TEST

Compliance	IEC 61000-4-5: 2005 Level 4, IEC 60255-26:2013
Pulse duration	Time to half-value: 1.2/50 µs
Between all groups and protective earth conductor terminal	Amplitude 4 kV
Between terminals of each group (excluding communications ports, where applicable)	Amplitude 2 kV

14.7 IMMUNITY TO RADIATED ELECTROMAGNETIC ENERGY

Compliance	IEC 60255-22-3: 2007, Class III, IEC 60255-26:2013
Frequency band	80 MHz to 3.0 GHz
Spot tests at	80, 160, 380, 450, 900, 1850, 2150 MHz
Test field strength	10 V/m
Test using AM	1 kHz @ 80%
Compliance	IEEE/ANSI C37.90.2: 2004
Frequency band	80 MHz to 1 GHz
Spot tests at	80, 160, 380, 450 MHz
Waveform	1 kHz @ 80% am and pulse modulated
Field strength	35 V/m

14.8 RADIATED IMMUNITY FROM DIGITAL COMMUNICATIONS

Compliance	IEC 61000-4-3: 2006, Level 4, IEC 60255-26:2013
Frequency bands	800 to 960 MHz, 1.4 to 2.0 GHz
Test field strength	30 V/m
Test using AM	1 kHz / 80%

14.9 RADIATED IMMUNITY FROM DIGITAL RADIO TELEPHONES

Compliance	IEC 61000-4-3: 2006, IEC 60255-26:2013
Frequency bands	900 MHz and 1.89 GHz
Test field strength	10 V/m

14.10 IMMUNITY TO CONDUCTED DISTURBANCES INDUCED BY RADIO FREQUENCY FIELDS

Compliance	IEC 61000-4-6: 2008, Level 3, IEC 60255-26:2013
Frequency bands	150 kHz to 80 MHz

Test disturbance voltage	10 V rms
Test using AM	1 kHz @ 80%
Spot tests	27 MHz and 68 MHz

14.11 MAGNETIC FIELD IMMUNITY

Compliance	IEC 61000-4-8: 2009 Level 5 IEC 61000-4-9/10: 2001 Level 5
IEC 61000-4-8 test	100 A/m applied continuously, 1000 A/m applied for 3 s
IEC 61000-4-9 test	1000 A/m applied in all planes
IEC 61000-4-10 test	100 A/m applied in all planes at 100 kHz/1 MHz with a burst duration of 2 seconds

14.12 CONDUCTED EMISSIONS

Compliance	EN 55022: 2010, IEC 60255-26:2013
Power supply test 1	0.15 - 0.5 MHz, 79 dBµV (quasi peak) 66 dBµV (average)
Power supply test 2	0.5 – 30 MHz, 73 dBµV (quasi peak) 60 dBµV (average)
RJ45 test 1 (where applicable)	0.15 - 0.5 MHz, 97 dBµV (quasi peak) 84 dBµV (average)
RJ45 test 2 (where applicable)	0.5 – 30 MHz, 87 dBµV (quasi peak) 74 dBµV (average)

14.13 RADIATED EMISSIONS

Compliance	EN 55022: 2010, IEC 60255-26:2013
Test 1	30 – 230 MHz, 40 dBµV/m at 10 m measurement distance
Test 2	230 – 1 GHz, 47 dBµV/m at 10 m measurement distance
Test 3	1 – 2 GHz, 76 dBμV/m at 10 m measurement distance

14.14 POWER FREQUENCY

Compliance	IEC 60255-22-7:2003, IEC 60255-26:2013
Opto-inputs (Compliance is achieved using the opto-input filter)	300 V common-mode (Class A) 150 V differential mode (Class A)

Note:

Compliance is achieved using the opto-input filter.

15 REGULATORY COMPLIANCE

Compliance with the European Commission Directive on EMC and LVD is demonstrated using a technical file.



15.1 EMC COMPLIANCE: 2014/30/EU

The product specific Declaration of Conformity (DoC) lists the relevant harmonised standard(s) or conformity assessment used to demonstrate compliance with the EMC directive.

15.2 LVD COMPLIANCE: 2014/35/EU

The product specific Declaration of Conformity (DoC) lists the relevant harmonized standard(s) or conformity assessment used to demonstrate compliance with the LVD directive.

Safety related information, such as the installation I overvoltage category, pollution degree and operating temperature ranges are specified in the Technical Data section of the relevant product documentation and/or on the product labelling.

Unless otherwise stated in the Technical Data section of the relevant product documentation, the equipment is intended for indoor use only. Where the equipment is required for use in an outdoor location, it must be mounted in a specific cabinet or housing to provide the equipment with the appropriate level of protection from the expected outdoor environment.

15.3 R&TTE COMPLIANCE: 2014/53/EU

Radio and Telecommunications Terminal Equipment (R&TTE) directive 2014/53/EU.

Conformity is demonstrated by compliance to both the EMC directive and the Low Voltage directive, to zero volts.

15.4 UL/CUL COMPLIANCE

If marked with this logo, the product is compliant with the requirements of the Canadian and USA Underwriters Laboratories.

The relevant UL file number and ID is shown on the equipment.



15.5 ATEX COMPLIANCE: 2014/34/EU

Products marked with the 'explosion protection' Ex symbol (shown in the example, below) are compliant with the ATEX directive. The product specific Declaration of Conformity (DoC) lists the Notified Body, Type Examination Certificate, and relevant harmonized standard or conformity assessment used to demonstrate compliance with the ATEX directive.

The ATEX Equipment Protection level, Equipment group, and Zone definition will be marked on the product.

For example:



Where:

'II' Equipment Group: Industrial.

'(2)G' High protection equipment category, for control of equipment in gas atmospheres in Zone 1 and 2.

This equipment (with parentheses marking around the zone number) is not itself suitable for operation

within a potentially explosive atmosphere.

APPENDIX A

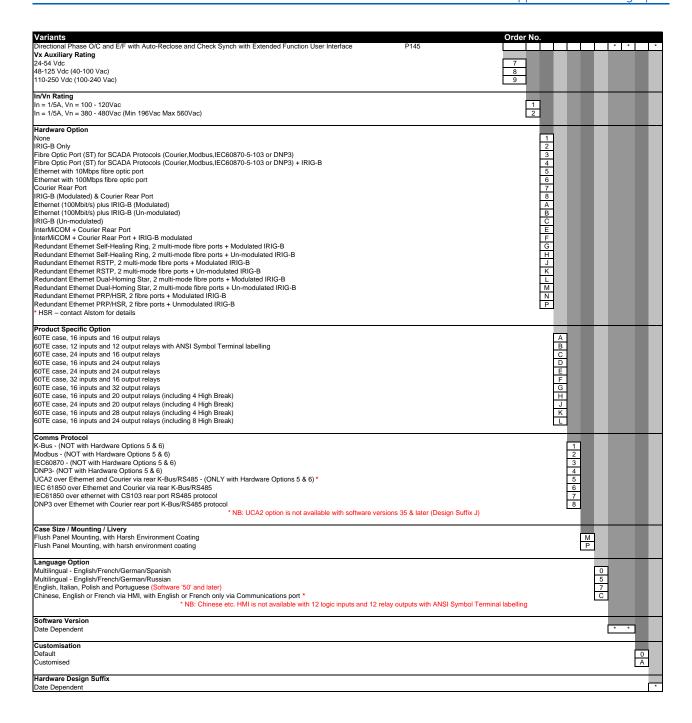
ORDERING OPTIONS

Variants			Order No.	
Feeder Management			P141	**
Design Suffix				
CPU3 with extended memory, dual characteristic opto inputs, IEC61850, InterMICOM CPU3, dual characteristic opto inputs, IEC61850, InterMICOM			_	P
Phase 2 CPU, UCA2			_	G
Second comms card, IEC60870 private codes, P144, improved power supply			_	C
Expansion I/o and IDMT characteristic enhancements Original Release - Phase 1			_	J G C B
				<u> </u>
Vx Auxiliary Rating 24-54 Vdc			7	_
48-125 Vdc (40-100 Vac)			7 8	_
110-250 Vdc (100-240 Vac)			9	_
In/Vn Rating				
In = 1/5A, Vn = 100 - 120Vac			1	_
In = 1/5A, Vn = 380 - 480Vac (Min 196Vac Max 560Vac)			2	_
Hardware Options	Protocol Compatibility	Design Suffix Compatibility		
Standard - None IRIG-B - (Modulated) Only	1, 2, 3 & 4 1, 2, 3 & 4	All All	1 2	_
Fibre Optic Port (ST) for SCADA Protocols (Courier, Modbus, IEC60870-5-103 or DNP3)	3	All	3	_
Fibre Optic Port (ST) for SCADA Protocols (Courier, Modbus, IEC60870-5-103 or DNP3) +	1, 2 & 4	J/P		_
IRIG-B (Modulated)	3 1, 2 & 4	All J/P	4	_
Ethernet (10 Mbps)	5	G/J/P *	5	_
Ethernet (100 Mbps)	5, 6, 7 & 8	G/J/P *	6	_
Courier Rear Port IRIG-B (Modulated) & Courier Rear Port	1, 2, 3 & 4 1, 2, 3 & 4	C, G, J or P C, G, J or P	7 8	
Ethernet (100Mbit/s) plus IRIG-B (Modulated)	6, 7 & 8	J/P *	8 A B C E F G H J K	
Ethernet (100Mbit/s) plus IRIG-B (Un-modulated)	6,7 & 8	J/P *	B	_
IRIG-B (Un-modulated) InterMiCOM + Courier Rear Port	1, 2, 3 & 4 1, 2, 3 & 4	J/P J/P	1	_
InterMiCOM + Courier Rear Port + IRIG-B modulated	1, 2, 3 & 4	J/P	1	_
Redundant Ethernet Self-Healing Ring, 2 multi-mode fibre ports + Modulated IRIG-B	6, 7 & 8	J/P **	G	_
Redundant Ethernet Self-Healing Ring, 2 multi-mode fibre ports + Un-modulated IRIG-B Redundant Ethernet RSTP, 2 multi-mode fibre ports + Modulated IRIG-B	6, 7 & 8 6, 7 & 8	J/P **	┥ <u></u>	_
Redundant Ethernet RSTP, 2 multi-mode fibre ports + Un-modulated IRIG-B	6, 7 & 8	J/P **	T K	_
Redundant Ethernet Dual-Homing Star, 2 multi-mode fibre ports + Modulated IRIG-B	6,7 & 8	J/P **		_
Redundant Ethernet Dual-Homing Star, 2 multi-mode fibre ports + Un-modulated IRIG-B Redundant Ethernet PRP/HSR, 2 fibre ports + Modulated IRIG-B	6, 7 & 8 6, 7 & 8	J/P ** J/P ***	M	_
Redundant Ethernet PRP/HSR, 2 fibre ports + Unmodulated IRIG-B	6, 7 & 8	J/P ***	P	_
0.00				
* Options are not available with software versions 32 or 34 except for 100Mbi ** Only available with software v		tware version 35 or later (Design	_	
*** Only available with software			_	
Product Specific Option				
40TE Case, 8 inputs & 7 relay outputs			A	_
40TE Case, 8 inputs & 8 relay outputs			N	
* Only Available with software versions 44 and later			_	_
Protocol / Communications Options	Hardware Compatibility	Design Suffix Compatibility		
K-Bus/Courier	1 & 2	All	1	_
	7 or 8	C, G, J or P	1	_
	C, E & F 3 & 4	J/P J/P	_	_
	1 & 2	All	1	_
Modbus	7or 8	C, G, J or P	2	_
	C, E & F 3 & 4	J/P J/P	-	_
	1, 2, 3 & 4	All		_
IEC 60870-5-103 (VDEW)	7or 8	C, G, J or P	3	_
	C, E & F 1 & 2	J/P All		_
DND0 0	7 or 8	C, G, J or P	1	_
DNP3.0	C, E & F	J/P	_ 4	_
UCA2	3 & 4	J/P	5	_
IEC 61850 over Ethernet and Courier via rear K-Bus/RS485	6, A, B, G, H , J, K, L, M, N, P	J/P	6	_
IEC61850 over ethernet with CS103 rear port RS485 protocol	6, A, B, G, H , J, K, L, M, N, P	J/P	7	_
DNP3 over Ethernet with Courier rear port K-Bus/RS485 protocol	6, A, B, G, H , J, K, L, M, N, P	J/P	8	_
* NB: UCA2 option is not available with software versions 32, and later (Design	Suffix J)		_	_
Mounting Option				
Flush Panel Mounting, with Harsh Environment Coating				М
Flush Panel Mounting, with harsh environment coating				P
Multilingual Language Option		Design Suffix Compatibility		
English, French, German, Spanish		All		0
English, French, German, Russian		G, J or P		5
English, Italian, Polish and Portuguese (Software '50' and later)		J/P		7
Chinese, English or French via HMI, with English or French only via Communications port		J/P		С
Software Issue				
Customisation				
Default				0
Customer specific				A

Variants			Order No.
Feeder Management			P142 ** **
Design Suffix			
CPU3 with extended memory, dual characteristic opto inputs, IEC61850, InterMICOM Dual characteristic opto inputs, IEC61850, InterMICOM			P J
Phase 2 CPU, UCA2			G
Second comms card, IEC60870 private codes, P144, improved power supply Expansion I/o and IDMT characteristic enhancements			G C B A
Original Release - Phase 1			A
Vx Auxiliary Rating			
24 - 54Vdc			7
48 - 125Vdc (40 - 100Vac)			8
110 - 250Vdc (100 - 240Vac)			9
In/Vn Rating In = 1/5A, Vn = 100 - 120Vac			1
In = 1/5A, Vn = 380 - 480Vac (Min 196Vac Max 560Vac)			2
Hardware Options	Protocol Compatibility	Design Suffix Compatibility	
Standard - None	1, 2, 3 & 4	All	
IRIG-B Only (Modulated)	1, 2, 3 & 4	All All	2
Fibre Optic Port (ST) for SCADA Protocols (Courier, Modbus, IEC60870-5-103 or DNP3)	1, 2 & 4	J/P only	3
Fibre Optic Port (ST) for SCADA Protocols (Courier, Modbus, IEC60870-5-103 or DNP3) + IRIG-B modulated	3 1, 2 & 4	All J/P only	- 4
Ethernet (10 Mbps)	1, 2 & 4	G, J or P *	5
Ethernet (100 Mbps)	5, 6, 7 & 8	G, J or P *	5 6
Second Rear Comms Port Second Rear Comms Port + IRIG-B (modulated)	1, 2, 3 & 4 1, 2, 3 & 4	C, G, J or P C, G, J or P	7 8
Ethernet (100Mbit/s) plus IRIG-B (Modulated)	6, 7 & 8	J/P *	8 A B C E F G H J K
Ethernet (100Mbit/s) plus IRIG-B (Un-modulated)	6, 7 & 8	J/P *	В
IRIG-B (Un-modulated) InterMiCOM + Courier Rear Port	1, 2, 3 & 4 1, 2, 3 & 4	J/P J/P	- C
InterMiCOM + Courier Rear Port + IRIG-B modulated	1, 2, 3 & 4	J/P	- F
Redundant Ethernet Self-Healing Ring, 2 multi-mode fibre ports + Modulated IRIG-B	6, 7 & 8	J/P **	G
Redundant Ethernet Self-Healing Ring, 2 multi-mode fibre ports + Un-modulated IRIG-B Redundant Ethernet RSTP, 2 multi-mode fibre ports + Modulated IRIG-B	6, 7 & 8 6, 7 & 8	J/P ** J/P **	-
Redundant Ethernet RSTP, 2 multi-mode fibre ports + Un-modulated IRIG-B	6, 7 & 8	J/P **	K K
Redundant Ethernet Dual-Homing Star, 2 multi-mode fibre ports + Modulated IRIG-B	6, 7 & 8	J/P **	L
Redundant Ethernet Dual-Homing Star, 2 multi-mode fibre ports + Un-modulated IRIG-B Redundant Ethernet PRP/HSR, 2 fibre ports + Modulated IRIG-B	6, 7 & 8 6, 7 & 8	J/P ** J/P ***	- M
Redundant Ethernet PRP/HSR, 2 fibre ports + Modulated IRIG-B	6, 7 & 8	J/P ***	N P
Product Specific Option 8 logic inputs & 7 relay outputs 12 logic inputs & 11 relay outputs 16 logic inputs & 7 relay outputs 8 logic inputs & 7 relay outputs 8 logic inputs & 15 relay outputs 8 logic inputs & 11 relay outputs (8 logic inputs & 11 relay outputs (including 4 High Break)			A B C D
	11-1	D	
Protocol / Communications Options	Hardware Compatibility 1 & 2	Design Suffix Compatibility All	
K-Bus	7 or 8	C, G, J or P	1
	C, E & F 3 & 4	J/P only J/P only	
	1 & 2	All	
Modbus	7 or 8	C, G J or P	2
	C, E & F 3 & 4	J/P only J/P only	
	1, 2, 3 & 4	All	
IEC 60870-5-103 (VDEW)	7 or 8 C. E & F	C, G, J or P J/P only	3
	1 & 2	All	
DNP3.0	7 or 8	J/P only	4
DN 3.0	C, E & F	C, G, J or P	1
UCA2	3 & 4 5 & 6	G, J or P *	5
IEC 61850 over Ethernet and Courier via rear K-Bus/RS485	6, A, B, G, H , J, K, L, M, N, P	J/P *	6
IEC61850 over ethernet with CS103 rear port RS485 protocol	6, A, B, G, H , J, K, L, M, N, P	J/P	7
DNP3 over Ethernet with Courier rear port K-Bus/RS485 protocol	6, A, B, G, H , J, K, L, M, N, P	J/P	8
* NB: UCA2 option is not a	vailable with software versions 32	2, and later (Design Suffix J)	
Mounting Option Flush Panel Mounting, with Harsh Environment Coating Flush Panel Mounting, with harsh environment coating			MP
Multilingual Language Option		Design Suffix Compatibility	
English, French, German, Spanish		All	0
English, French, German, Russian English, Italian, Polish and Portuguese (Software '50' and later)		G, J or P	5
English, Italian, Polish and Portuguese (Software '50' and later) Chinese, English or French via HMI, with English or French only via Communications port		J/P J/P	7 C
Software Issue		J. 1	1 2
Customisation Default			
Customer specific			A

Variants		0	rder No.
Feeder Management Design Suffix			143
CPU3 with extended memory, dual characteristic opto inputs, IEC61850, InterMICOM			P
CPU3, dual characteristic opto inputs, IEC61850, InterMICOM Phase 2 CPU, UCA2			J G
Second comms card, IEC60870 private codes, P144, improved power supply			J G C B
Expansion I/O and IDMT characteristic enhancements Original Release - Phase 1			BA
Vx Auxiliary Rating			
24-54 Vdc 48-125 Vdc (40-100 Vac)			7 8
110-250 Vdc (100-240 Vac)			9
In/Vn Rating			
In = 1/5A, Vn = 100 - 120Vac In = 1/5A, Vn = 380 - 480Vac (Min 196Vac Max 560Vac)			1 2
Hardware Options	Protocol Compatibility	Design Suffix Compatibility	
Standard - None IRIG-B Only (Modulated)	1, 2, 3 & 4 1, 2, 3 & 4	All All	1 2
Fibre Optic Port (ST) for SCADA Protocols (Courier, Modbus, IEC60870-5-103 or DNP3)	3 1, 2 & 4	All J/P only	3
Fibre Optic Port (ST) for SCADA Protocols (Courier, Modbus, IEC60870-5-103 or DNP3) +	3	All	4
IRIG-B modulated Ethernet (10 Mbps)	1, 2 & 4 5	J/P only G, J or P *	5
Ethernet (100 Mbps) Rear Comms	5, 6 & 7 1, 2, 3 & 4	G or J * C, G, J or P	6 7
IRIG-B (Modulated) & Rear Comms	1, 2, 3 & 4	C, G or J	8
Ethernet (100Mbit/s) plus IRIG-B (Modulated) Ethernet (100Mbit/s) plus IRIG-B (Un-modulated)	5, 6 & 7 5, 6 & 7	J/P * J/P *	A B
IRIG-B (Un-modulated)	1, 2, 3 & 4	J/P	B C
InterMiCOM + Courier Rear Port InterMiCOM + Courier Rear Port + IRIG-B modulated	1, 2, 3 & 4 1, 2, 3 & 4	J/P J/P	E F
Redundant Ethernet Self-Healing Ring, 2 multi-mode fibre ports + Modulated IRIG-B	6, 7 & 8	J/P **	G
Redundant Ethernet Self-Healing Ring, 2 multi-mode fibre ports + Un-modulated IRIG-B Redundant Ethernet RSTP, 2 multi-mode fibre ports + Modulated IRIG-B	6, 7 & 8 6, 7 & 8	J/P ** J/P **	H
Redundant Ethernet RSTP, 2 multi-mode fibre ports + Un-modulated IRIG-B Redundant Ethernet Dual-Homing Star, 2 multi-mode fibre ports + Modulated IRIG-B	6, 7 & 8 6, 7 & 8	J/P ** J/P **	K
Redundant Ethernet Dual-Homing Star, 2 multi-mode fibre ports + Un-modulated IRIG-B	6, 7 & 8	J/P **	M
Redundant Ethernet PRP/HSR, 2 fibre ports + Modulated IRIG-B Redundant Ethernet PRP/HSR, 2 fibre ports + Unmodulated IRIG-B	6, 7 & 8 6, 7 & 8	J/P *** J/P ***	N P
·			
Options are not available with software versions 32 or 34 <u>EXCEPT</u> for 100Mb Only Available with software Only Available with software	versions 43 and later	ftware version 35 or later (Design	
Product Specific Options 60TE Case, 16 inputs & 14 relay outputs			A
60TE Case, 24 inputs & 14 relay outputs			C
60TE Case, 16 inputs & 22 relay outputs 60TE case, 24 inputs & 22 relay outputs			D E
60TE case, 32 inputs & 14 relay outputs			F
60TE Case, 16 logic inputs & 30 relay outputs 60TE Case, 16 inputs & 18 relay outputs (including 4 High Break)			G H
60TE Case, 24 inputs & 18 relay outputs (including 4 High Break)			J
60TE Case, 16 inputs & 26 relay outputs (including 4 High Break) 60TE Case, 16 inputs & 22 relay outputs (including 8 High Break)			K L
80TE Case, 32 inputs & 32 relay outputs 80TE Case, 48 inputs & 16 relay outputs			M
			-
Protocol / Communications Options	Hardware Compatibility 1 & 2	Design Suffix Compatibility All	
K-Bus	7 & 8 C, E & F	C, G, J or P J/P	1
	3 & 4	J/P	
	1 & 2 7 & 8	All C, G, J or P	
Modbus	C, E & F	J/P	2
	3 & 4 1, 2, 3 & 4	J/P All	
IEC 60870-5-103 (VDEW)	7 & 8	C, G, J or P	3
	C, E & F 1 & 2	J/P All	
DNP3.0	7 & 8	C, G, J or JP	4
	C, E & F 3 & 4	J/P J/P	
UCA2	5 & 6	G, J or P *	5
IEC 61850 over Ethernet and Courier via rear K-Bus/RS485 IEC61850 over ethernet with CS103 rear port RS485 protocol	6, A, B, G, H, J, K, L, M, N, P 6, A, B, G, H, J, K, L, M, N, P	J/P J/P	6 7
DNP3 over Ethernet with Courier rear port K-Bus/RS485 protocol	6, A, B, G, H , J, K, L, M, N, P	J/P	8
	available with software versions 32	2 and later (Design Suffix J)	
Mounting Option Flush Panel Mounting, with Harsh Environment Coating			M
Rack Mounting, (80TE only) with Harsh Environmental Coating			N
Flush Panel Mounting, with harsh environment coating Rack Mounting, (80TE only) with harsh environmental coating			PQ
		Decise Of the Committee	
Multilingual Language Option English, French, German, Spanish		Design Suffix Compatibility All	0
English, French, German, Russian		G, J or P	5 7
English, Italian, Polish and Portuguese (Software '50' and later) Chinese, English or French via HMI, with English or French only via Communications port		J/P J/P	7 C
Software Issue			-
Settings/Customisation			
Default			0 A
Customised			

Variants			Order No.
Feeder Management			P144
Design Suffix CPU3 with extended memory, dual characteristic opto inputs, IEC61850, InterMICOM			P
Dual characteristic opto inputs, IEC61850, InterMICOM			The second secon
Phase 2 CPU, UCA2			J G C
Second comms card, IEC60870 private codes, P144, improved power supply			C
Vx Auxiliary Rating			
24-54 Vdc			7
48-125 Vdc (40-100 Vac) 110-250 Vdc (100-240 Vac)			8
·			3
In/Vn Rating In = 1/5A, Vn (Ph) = 100-120Vac, Vn (E/f) = 380-440Vac (Min 196Vac Max 560Vac)			4
Hardware Options	Protocol Compatibility	Design Suffix Compatibility	
Standard - None IRIG-B Only (Modulated)	1, 2, 3 & 4 1, 2, 3 & 4	All All	1 2
Fibre Optic Port (ST) for SCADA Protocols (Courier, Modbus, IEC60870-5-103 or DNP3)	3	All	3
Fibre Optic Port (ST) for SCADA Protocols (Courier, Modbus, IEC60870-5-103 or DNP3) +	1, 2 & 4	J/P only All	
IRIG-B (Modulated)	1, 2 & 4	J/P only	4
Ethernet (10 Mbps) Ethernet (100 Mbps)	5 5, 6, 7 & 8	G G, J or P *	5 6
Rear Comms	1, 2, 3 & 4	C, G, J or P	7
IRIG-B (Modulated) & Rear Comms	1, 2, 3 & 4	C, G, J or P	8
Ethernet (100Mbit/s) plus IRIG-B (Modulated) Ethernet (100Mbit/s) plus IRIG-B (He-modulated)	6,7 & 8	J/P J/P	A
Ethernet (100Mbit/s) plus IRIG-B (Un-modulated) IRIG-B (Un-modulated)	6, 7 & 8 1, 2, 3 & 4	J/P J/P	7 8 A B C E F G H J K
InterMiCOM + Courier Rear Port	1, 2, 3 & 4	J/P	E B
InterMiCOM + Courier Rear Port + IRIG-B modulated	1, 2, 3 & 4	J/P J/P **	F
Redundant Ethernet Self-Healing Ring, 2 multi-mode fibre ports + Modulated IRIG-B Redundant Ethernet Self-Healing Ring, 2 multi-mode fibre ports + Un-modulated IRIG-B	6, 7 & 8 6, 7 & 8	J/P **	H H
Redundant Ethernet RSTP, 2 multi-mode fibre ports + Modulated IRIG-B	6, 7 & 8	J/P **	i i
Redundant Ethernet RSTP, 2 multi-mode fibre ports + Un-modulated IRIG-B	6, 7 & 8	J/P **	K
Redundant Ethernet Dual-Homing Star, 2 multi-mode fibre ports + Modulated IRIG-B Redundant Ethernet Dual-Homing Star, 2 multi-mode fibre ports + Un-modulated IRIG-B	6, 7 & 8 6, 7 & 8	J/P ** J/P **	L M
Redundant Ethernet PRP/HSR, 2 fibre ports + Modulated IRIG-B	6, 7 & 8	J/P ***	N
Redundant Ethernet PRP/HSR, 2 fibre ports + Unmodulated IRIG-B	6, 7 & 8	J/P ***	P
Product Specific Option 40TE Case, 8 inputs & 7 relay outputs 40TE Case, 12 inputs & 11 relay outputs 40TE Case, 16 inputs & 7 relay outputs 40TE Case, 6 inputs & 15 relay outputs 40TE Case, 8 inputs & 15 relay outputs 40TE Case, 8 inputs & 11 relay outputs 40TE Case, 8 inputs & 11 relay outputs (including 4 High Break)			A B C D H
Protocol / Communications Options	Hardware Compatibility	Design Suffix Compatibility	
	1 & 2 7 & 8	All C, G, J or P	
K-Bus	C, E & F	J/P	1
	3 & 4 1 & 2	J/P All	
Madhia	7 & 8	C, G, J or P	2
Modbus	C, E & F	J/P	
	3 & 4 1, 2, 3 & 4	J/P All	
IEC 60870-5-103 (VDEW)	C, E & F	J/P	3
	7 & 8	C, G, J or P	
	1 & 2 7 & 8	All C, G, J or P	
DNP3.0	C, E & F	J/P	4
UCA2	3 & 4	J/P	
IEC 61850 over Ethernet and Courier via rear K-Bus/RS485	5 & 6 6, A, B, G, H , J, K, L, M, N, P	G or J * J/P	5 6
IEC61850 over ethernet with CS103 rear port RS485 protocol	6, A, B, G, H , J, K, L, M, N, P	J/P	7
DNP3 over Ethernet with Courier rear port K-Bus/RS485 protocol	6, A, B, G, H , J, K, L, M, N, P	J/P	8
·	not available with software version	s ≥ 32 (Design Suffix J)	
Mounting Option Flush Panel Mounting, with Harsh Environment Coating			M M
Flush Panel Mounting, with harsh environment coating			MP
Multilingual Language Option		Desire Coffin Compatibility	
		Design Suffix Compatibility	
English, French, German, Spanish		All	0 5
			0 5 7
English, French, German, Spanish English, French, German, Russian		All G, J or P	5
English, French, German, Spanish English, French, German, Rusaian English, Italian, Polish and Portuguese (Software '50' and later)		All G, J or P J/P	<u>5</u> 7
English, French, German, Spanish English, French, German, Russian English, Italian, Polish and Portuguese (Software '50' and later) Chinese, English or French via HMI, with English or French only via Communications port Software Issue Customisation		All G, J or P J/P	5 7 C
English, French, German, Spanish English, French, German, Russian English, French, German, Russian English, Italian, Polish and Portuguese (Software '50' and later) Chinese, English or French via HMI, with English or French only via Communications port Software Issue		All G, J or P J/P	5 7 C



APPENDIX B

SETTINGS AND SIGNALS

Tables, containing a full list of settings, measurement data and DDB signals for each product model, are provided in a separate interactive PDF file attached as an embedded resource.

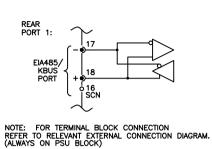
Tables are organized into a simple menu system allowing selection by language (where available), model and table type, and may be viewed and/or printed using an up-to-date version of Adobe Reader.

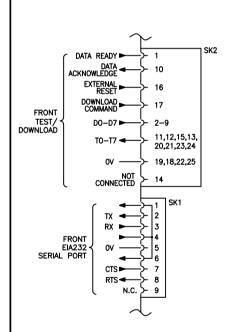
APPENDIX C

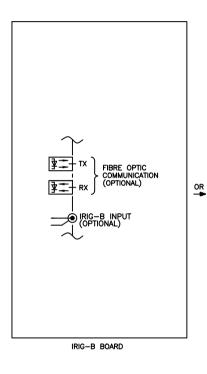
WIRING DIAGRAMS

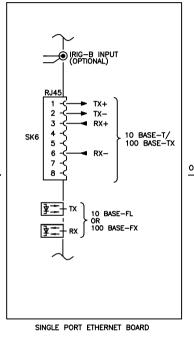
MODEL	CORTEC OPTION*	EXTERNAL CONNECTION DIAGRAM TITLE	DRAWING-SHEET	ISSUE	
P14x		COMMS OPTIONS MICOM PX40 PLATFORM	10Px4001-1	J	
-	IO Option A	(40TE) DIRECTIONAL PHASE O/C & E/F (8 I/P & 7 O/P)	<u>10P14101-1</u> , <u>10P14101-4</u>	N, G	
		(40TE) DIRECTIONAL PHASE O/C, E/F & SBEF + HIGH IMPEDANCE REF (8 I/P & 7 0/P)	<u>10P14101-2</u>	Р	
P141		(40TE) DIRECTIONAL PHASE O/C & E/F + LOW IMPEDANCE REF (8 I/P & 7 O/P)	<u>10P14101-3</u>	Р	
		(40TE) DIRECTIONAL PH O/C & E/F USING VEE CON. VT's (8 I/P & 7 O/P)	<u>10P14101-5</u>	Н	
	I/O Option N	(40TE) DIRECTIONAL PHASE O/C & E/F (8 I/P & 8 O/P)	<u>10P14102-1</u>	E	
	I/O option A	(40TE) DIRECT'AL PHASE O/C & E/F WITH AUTO-RECLOSE (8 I/P & 7 O/P)	<u>10P14201-1</u> , <u>10P14201-2</u>	R, F	
	I/O option B	(40TE) DIRECTIONAL PHASE O/C & E/F WITH AUTO-RECLOSE (12 I/P & 11 0/P)	<u>10P14202-1</u> , <u>10P14202-2</u>	F, E	
P142	I/O option C	(40TE) DIRECTIONAL PHASE O/C & E/F WITH AUTO-RECLOSE (16 I/P & 7 O/P)	<u>10P14203-1</u> , <u>10P14203-2</u>	F, E	
	I/O option D	(40TE) DIRECTIONAL PHASE O/C & E/F WITH AUTO-RECLOSE (8 I/P & 15 0/P)	<u>10P14204-1</u> , <u>10P14204-2</u>	F, E	
	I/O option H	(40TE) DIRECTIONAL PHASE O/C & E/F WITH AUTO-RECLOSE (8 I/P & 11 O/P)	<u>10P14205-1</u> , <u>10P14205-2</u>	F, C	
	I/O option A	(60TE) DIRECT'AL PHASE O.C. & S.E.F. AUTO-RECLOSE & CHECK SYNCH (16 I/P & 14 0/P)	<u>10P14301-1</u> , <u>10P14301-2</u>	0, G	
	I/O option C	(60TE) DIRECT'AL PH O.C. & S.E.F. AUTO-RECLOSE & CHECK SYNCH (24 I/P & 14 O/P)	<u>10P14302-1</u> , <u>10P14302-2</u>	F, E	
P143	I/O option D	(60TE) DIRECT'AL PHASE O.C. & S.E.F. AUTO-RECLOSE & CHECK SYNCH (16 I/P & 22 0/P)	<u>10P14303-1</u> , <u>10P14303-2</u>	F, E	
	I/O option E	(60TE) DIRECT'L PHASE O.C. & S.E.F. AUTO-RECLOSE & CHECK SYNCH (24 I/P & 22 0/P)	<u>10P14304-1</u> , <u>10P14304-2</u>	F, E	
	I/O option F	(60TE) DIRECT'L PHASE O.C. & S.E.F. AUTO-RECLOSE & CHECK SYNCH (32 I/P & 14 0/P)	<u>10P14305-1</u> , <u>10P14305-2</u>	F, E	
	I/O option G	(60TE) DIRECT'L PHASE O.C. & S.E.F. AUTO-RECLOSE & CHECK SYNCH (16 I/P & 32 O/P)	<u>10P14306-1</u> , <u>10P14306-2</u>	F, E	
P143	I/O option H	(60TE) DIRECTIONAL PHASE O/C & E/F WITH AUTO-RECLOSE (16 I/P & 18 O/P)	<u>10P14307-1</u> , <u>10P14307-2</u>	E, D	
	I/O option J	(60TE) DIRECTIONAL PHASE O/C & E/F WITH AUTO-RECLOSE (24 I/P & 18 O/P)	<u>10P14308-1</u> , <u>10P14308-2</u>	E, D	
	I/O option K	(60TE) DIRECTIONAL PHASE O/C & E/F WITH AUTO-RECLOSE (16 I/P & 26 O/P)	<u>10P14309-1</u> , <u>10P14309-2</u>	E, D	
	I/O option L	(60TE) DIRECTIONAL PHASE O/C & E/F WITH AUTO-RECLOSE (16 I/P & 22 O/P)	<u>10P14310-1</u> , <u>10P14310-2</u>	E, D	
	I/O option M	(80TE) DIRECTIONAL PHASE O/C & E/F WITH AUTO-RECLOSE (32 I/P & 32 O/P)	<u>10P14311-1</u> , <u>10P14311-2</u>	D, C	
	I/O option P	(80TE) DIRECTIONAL PHASE O/C & E/F WITH AUTO-RECLOSE (48 I/P & 16 O/P)	<u>10P14312-1</u>	В	
	I/O option A	(8 I/P & 7 O/P) USING VEE CONNECTED VTs, 2 LINE CTs AND A CORE BALANCE CT	<u>10P14401-1</u> , <u>10P14401-2</u>	G, D	
	I/O option B	(12 I/P & 11 O/P) USING VEE CONNECTED VTs, 2 LINE CTs AND A CORE BALANCE CT	10Px4001-1 10P14101-1, 10P14101-4 10P14101-2 10P14101-3 10P14101-5 10P14102-1 10P14201-1, 10P14201-2 10P14202-1, 10P14202-2 10P14203-1, 10P14203-2 10P14203-1, 10P14203-2 10P14205-1, 10P14205-2 10P14301-1, 10P14301-2 10P14302-1, 10P14302-2 10P14303-1, 10P14303-2 10P14304-1, 10P14303-2 10P14306-1, 10P14306-2 10P14308-1, 10P14308-2 10P14309-1, 10P14309-2 10P14310-1, 10P14310-2 10P14311-1, 10P14311-2 10P14312-1	H, D	
P144	I/O option C	(16 I/P & 7 O/P) USING VEE CONNECTED VTs, 2 LINE CTs AND A CORE BALANCE CT	<u>10P14403-1</u> , <u>10P14403-2</u>	G, D	
	I/O option D	(8 I/P & 15 O/P) USING VEE CONNECTED VTs, 2 LINE CTs AND A CORE BALANCE CT	<u>10P14404-1</u> , <u>10P14404-2</u>	G, D	
	I/O option H	(40TE) DIRECTIONAL PHASE O/C & E/F WITH AUTO-RECLOSE (8 I/P & 11 O/P)	<u>10P14405-1</u> , <u>10P14405-2</u>	E, C	
	I/O option A	(60TE) DIRECT'L PHASE O/C & S.E.F. AUTORECLOSE & CHECK SYNCH. (16 I/P & 16 O/P)	<u>10P14501-1</u>	D	
	I/O option B	(60TE) DIRECT'L PHASE O/C & S.E.F. AUTO-RECLOSE & CHECK SYNCH. (12 I/P & 12 O/P)	<u>10P14502-1</u>	D	
P145	I/O option C	(60TE) DIRECT'L PHASE O/C & S.E.F. AUTORECLOSE & CHECK SYNCH. (24 I/P & 16 O/P)	<u>10P14503-1</u>	D	
	I/O option D	(60TE) DIRECT'L PHASE O/C & S.E.F. AUTORECLOSE & CHECK SYNCH. (16 I/P & 24 O/P)	<u>10P14504-1</u>	D	
	I/O option E	(60TE) DIRECT'L PHASE O/C & S.E.F. AUTORECLOSE & CHECK SYNCH. (24 I/P & 24 O/P)	<u>10P14505-1</u>	D	
	I/O option F	(60TE) DIRECT'L PHASE O/C & S.E.F. AUTORECLOSE & CHECK SYNCH. (32 I/P & 16 O/P)	<u>10P14506-1</u>	D	
	I/O option G	(60TE) DIRECT'L PHASE O/C & S.E.F. AUTORECLOSE & CHECK SYNCH. (16 I/P & 32 O/P)	<u>10P14507-1</u>	D	
	I/O option H	(60TE) DIRECTIONAL PHASE O/C & E/F WITH AUTO-RECLOSE (16 I/P & 20 O/P)	<u>10P14508-1</u> , <u>10P14508-2</u>	E, D	
	I/O option J	(60TE) DIRECTIONAL PHASE O/C & E/F WITH AUTO-RECLOSE (24 I/P & 20 O/P)	<u>10P14509-1</u> , <u>10P14509-2</u>	E, D	
	I/O option K	(60TE) DIRECTIONAL PHASE O/C & E/F WITH AUTO-RECLOSE (16 I/P & 28 O/P)	<u>10P14510-1</u> , <u>10P14510-2</u>	E, D	
	I/O option L	(60TE) DIRECTIONAL PHASE O/C & E/F WITH AUTO-RECLOSE (16 I/P & 24 O/P)	<u>10P14511-1</u> , <u>10P14511-2</u>	E, D	

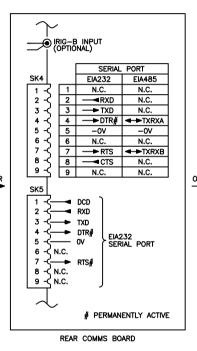
^{*} When selecting the applicable wiring diagram(s), refer to appropriate model's CORTEC.



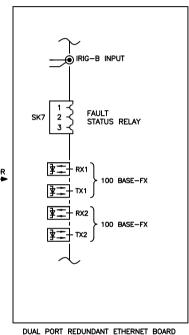








EXTERNAL CONNECTION DIAGRAM: COMMS OPTIONS



Issue:		Revision: DRAWING OUTLINE UPDATED. CID BLIN-8BHLDT				
Date:	30/11/2010	Name: W.LINTERN	CAD DATA 1:1 DIMENSIONS: mm			

Chkd: S KELSALL

DO NOT SCALE

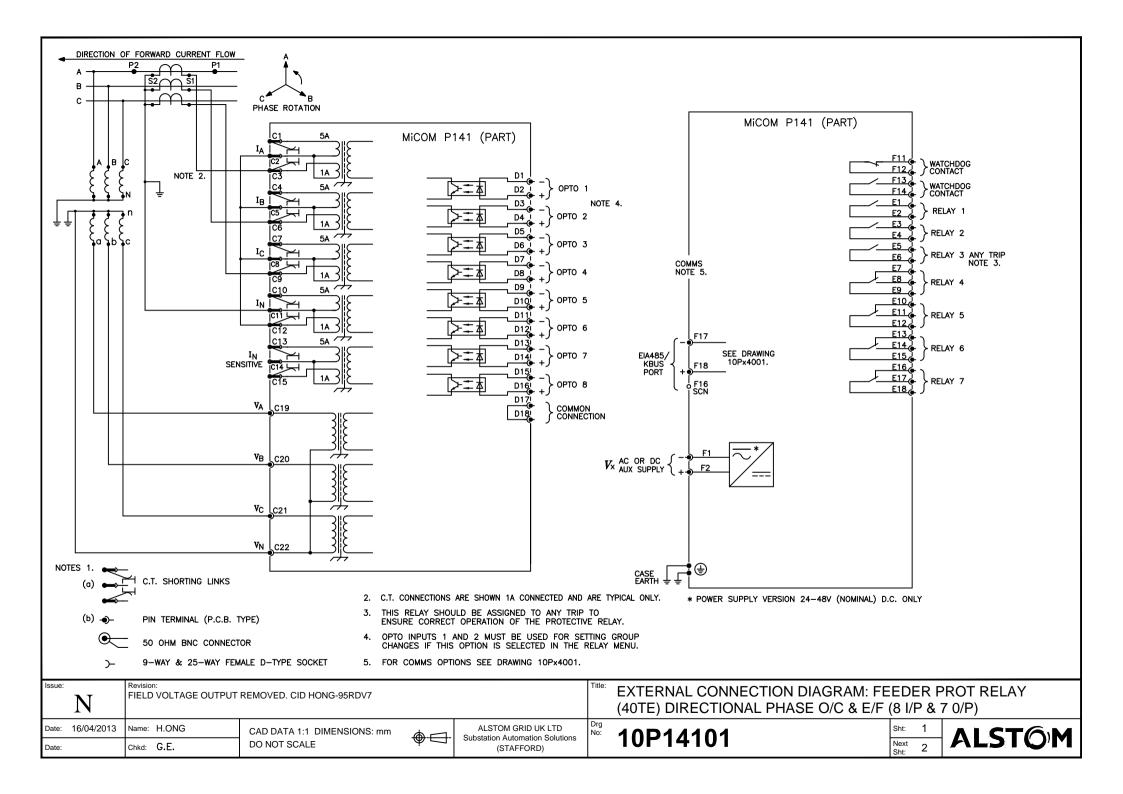
MICOM Px40 PLATFORM

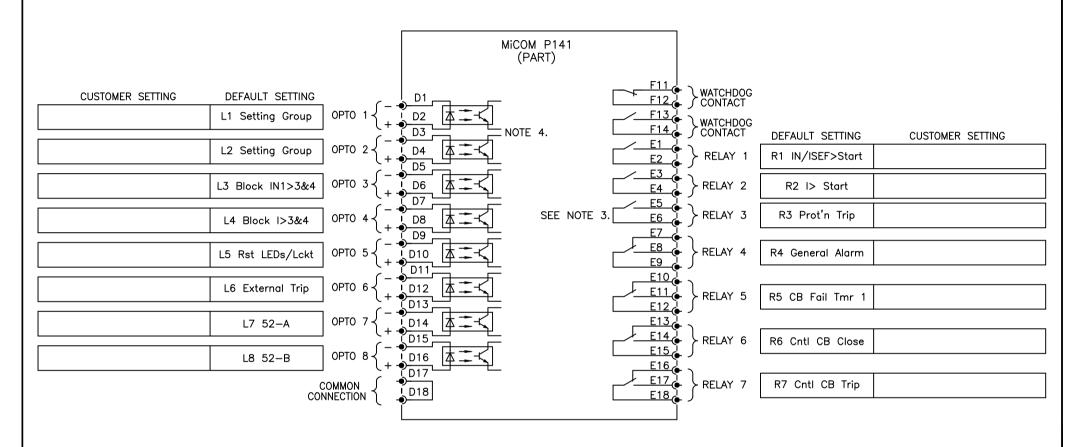
10Px4001

Sht: 1
Next Sht: Sht: ALSTO'M

mm	+	ALSTOM GRID UK LTD Substation Automation Solutions

(STAFFORD)

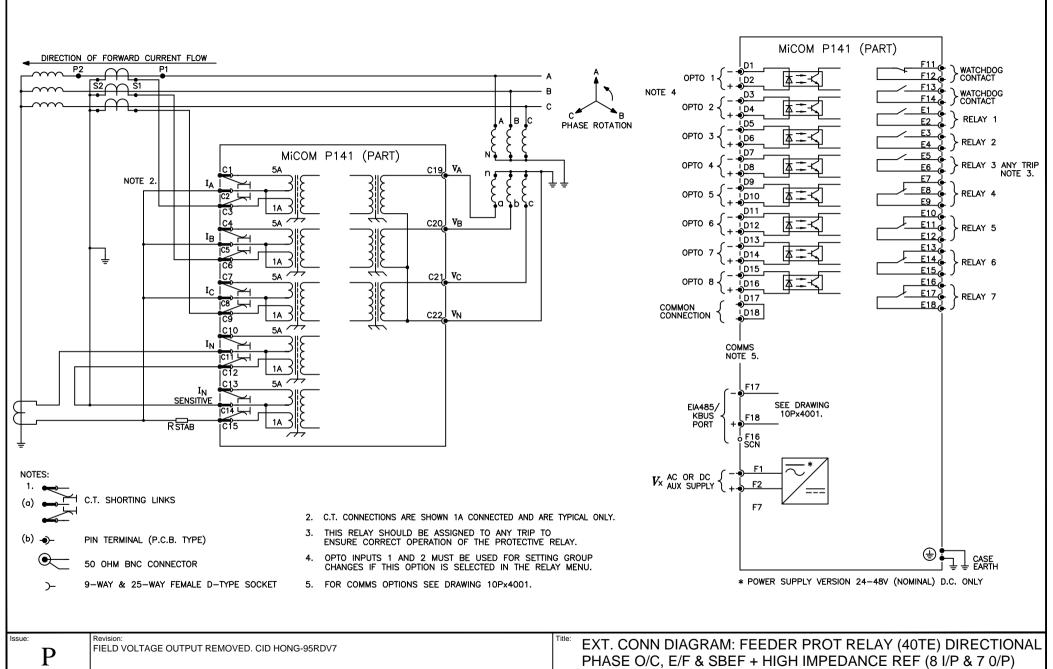




NOTE 3. THIS RELAY SHOULD BE ASSIGNED TO ANY TRIP TO ENSURE CORRECT OPERATION OF THE PROTECTIVE RELAY.

 OPTO INPUTS 1 AND 2 MUST BE USED FOR SETTING GROUP CHANGES IF THIS OPTION IS SELECTED IN THE RELAY MENU.

Issue:	Revision: DRAWING OUTLINE UPDATED . CID BLIN-8BHLDT			EXTERNAL CONNECTION DIAGRAM: FEEDER PROT RELAY (40TE) DIRECTIONAL PHASE O/C & E/F (8 I/P & 7 0/P)				
Date: 25/11/2010	Name: W.LINTERN	CAD DATA 1:1 DIMENSIONS: mm	*	ALSTOM GRID UK LTD Substation Automation Solutions	Drg No:	10P14101	Sht: 4	ALSTOM
Date:	Chkd: G.E.	DO NOT SCALE	₩ U	(STAFFORD)		10714101	Next Sht: 5	AL3 I OM



PHASE O/C, E/F & SBEF + HIGH IMPEDANCE REF (8 I/P & 7 O/P)

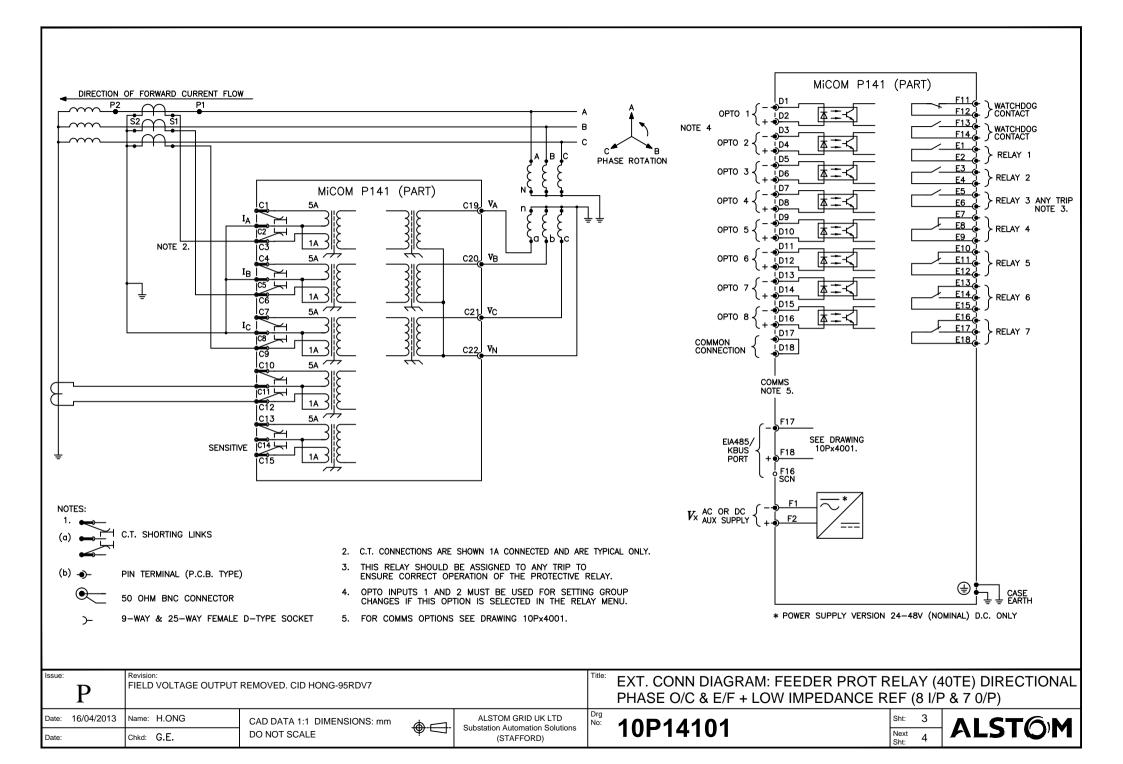
Date: 16/04/2013 Name: H.ONG
Date: Chkd: M.S.

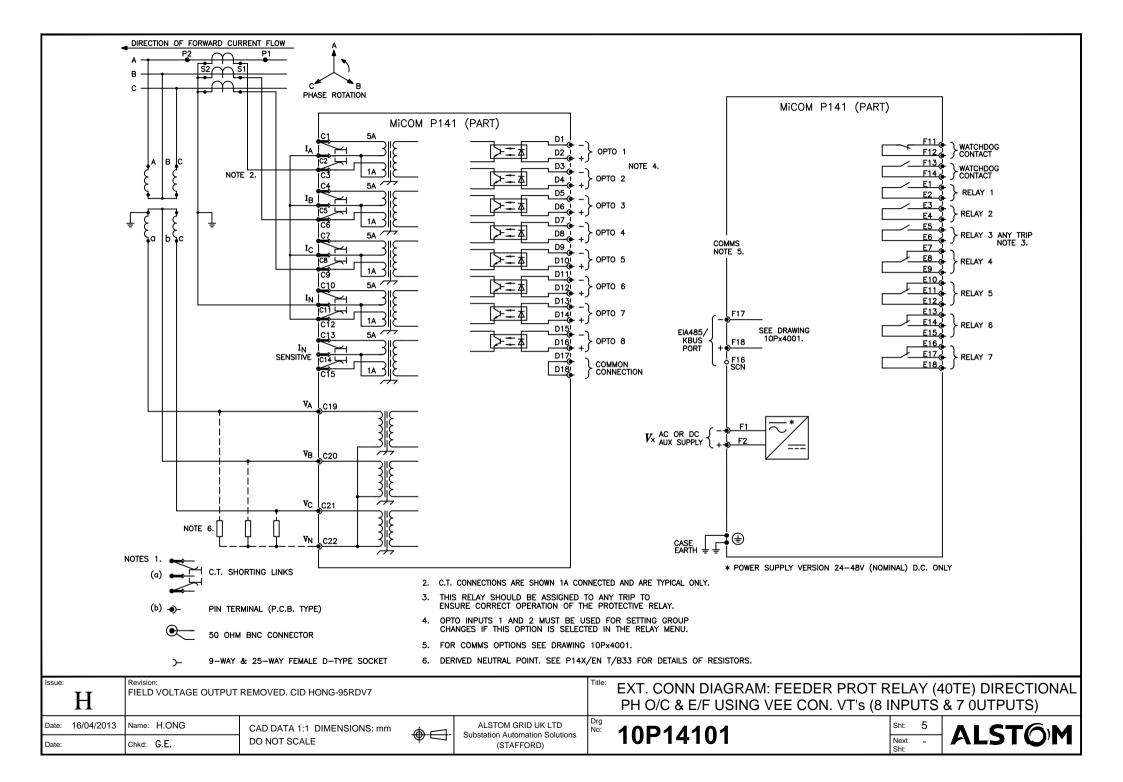
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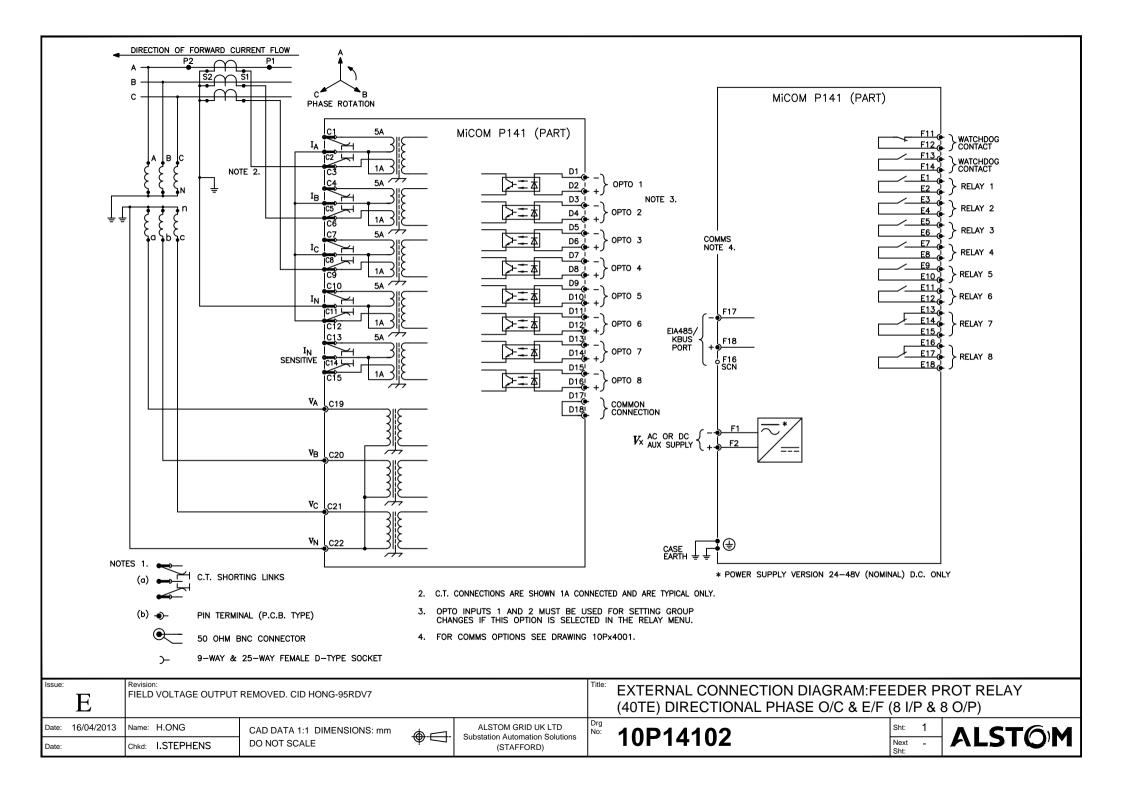
ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)

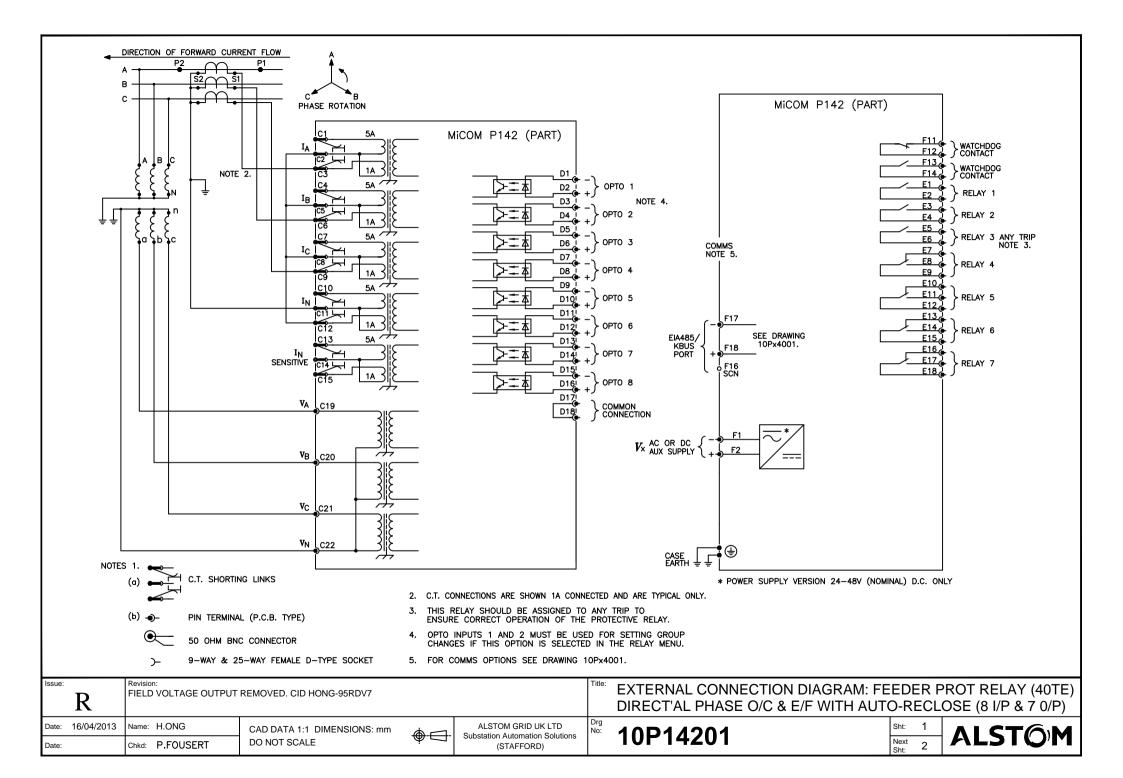
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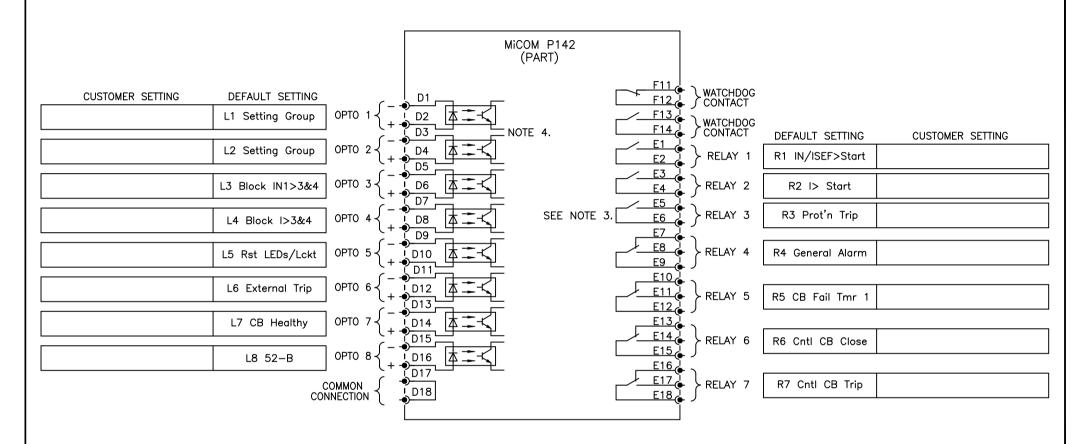
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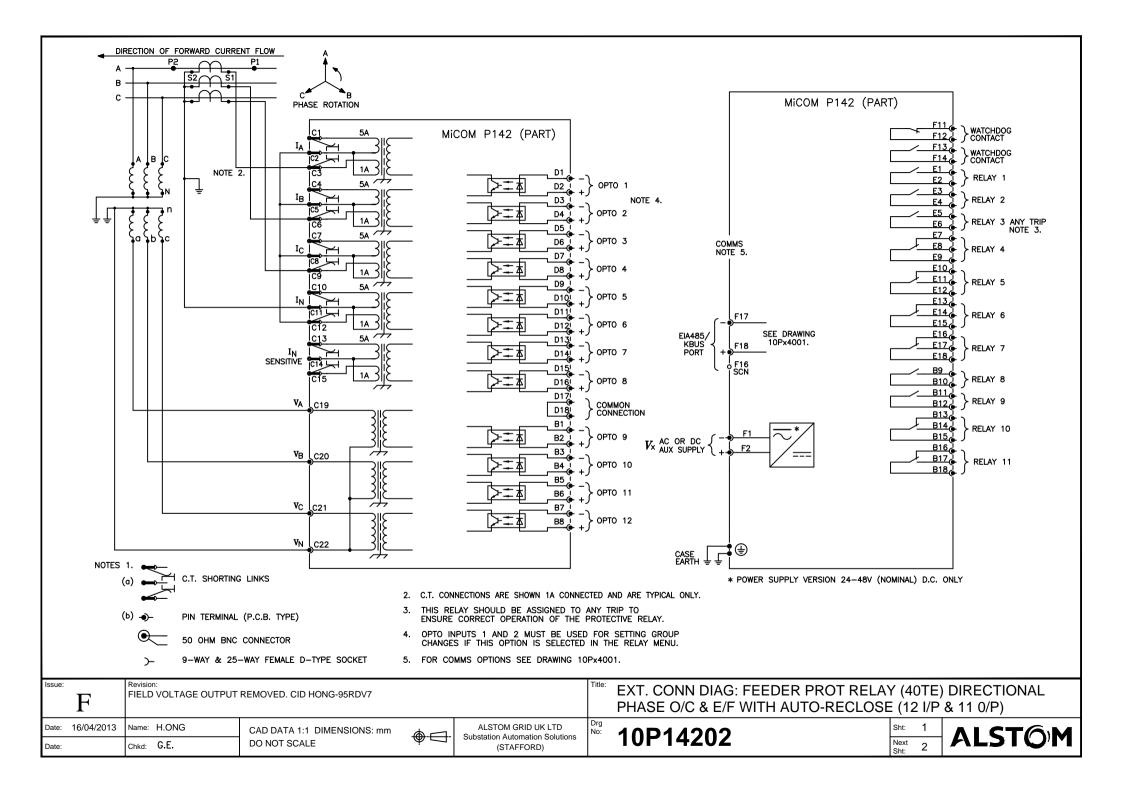
NOTE 3. THIS RELAY SHOULD BE ASSIGNED TO ANY TRIP TO ENSURE CORRECT OPERATION OF THE PROTECTIVE RELAY.

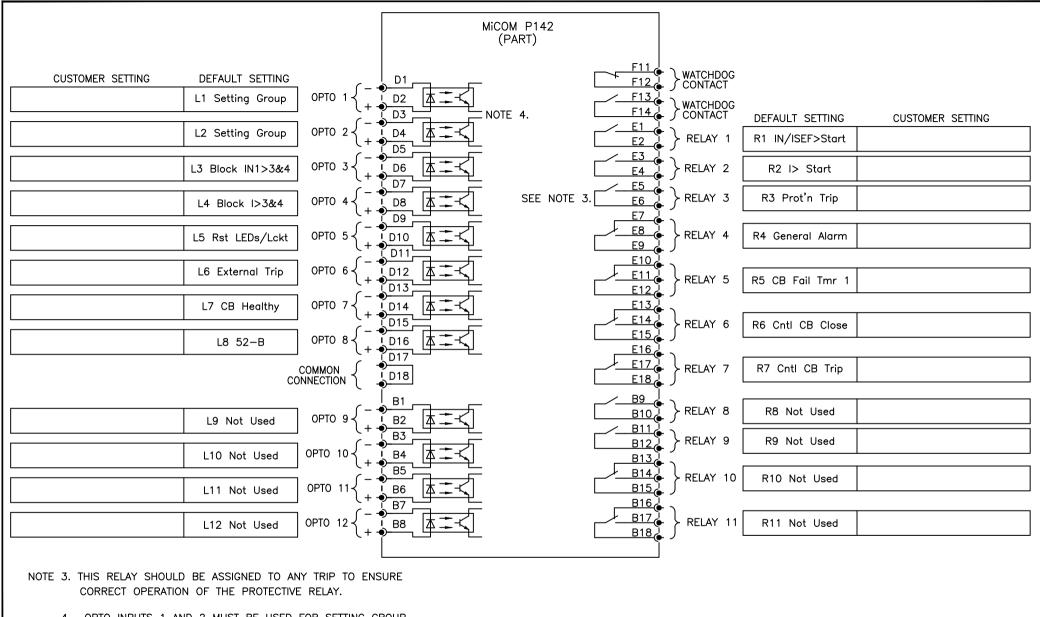
Chkd: G.E.

4. OPTO INPUTS 1 AND 2 MUST BE USED FOR SETTING GROUP CHANGES IF THIS OPTION IS SELECTED IN THE RELAY MENU.

ı									
I	Issue:	Revision: DRAWING OUTLINE UPDATED . CID BLIN-8BHLDT					EXTERNAL CONNECTION DIAGRAM: F DIRECT'AL PHASE O/C & E/F WITH AU		`
	Date: 25/11/2010	Name: W.LINTERN	CAD DATA 1:1 DIMENSIONS: mm	A .	ALSTOM GRID UK LTD Substation Automation Solutions	Drg No:	10P14201	Sht: 2	ALSTON
ı	Date:	Chkd: G.F.	DO NOT SCALE	Ψ —	(STAFFORD)		106 14201	Next -	IFILDIO

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4. OPTO INPUTS 1 AND 2 MUST BE USED FOR SETTING GROUP CHANGES IF THIS OPTION IS SELECTED IN THE RELAY MENU.

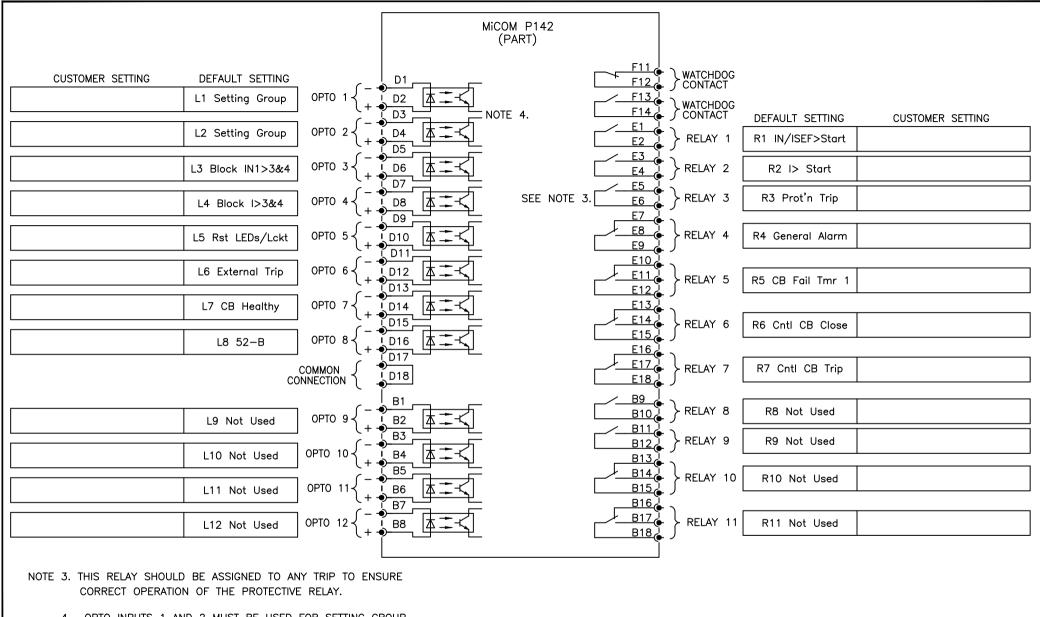
Chkd: G.E.

Issue: Revision: DRAWING OUTLINE UPDATED . CID BLIN-8BHLDT E Date: 25/11/2010 Name: W.LINTERN ALSTOM GRID UK LTD CAD DATA 1:1 DIMENSIONS: mm Substation Automation Solutions DO NOT SCALE

EXT.CONN DIAG: FEEDER PROT RELAY (40TE) DIRECTIONAL PHASE O/C & E/F WITH AUTO-RECLOSE (12 I/P & 11 0/P)

10P14202

ALSTOM Next



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4. OPTO INPUTS 1 AND 2 MUST BE USED FOR SETTING GROUP CHANGES IF THIS OPTION IS SELECTED IN THE RELAY MENU.

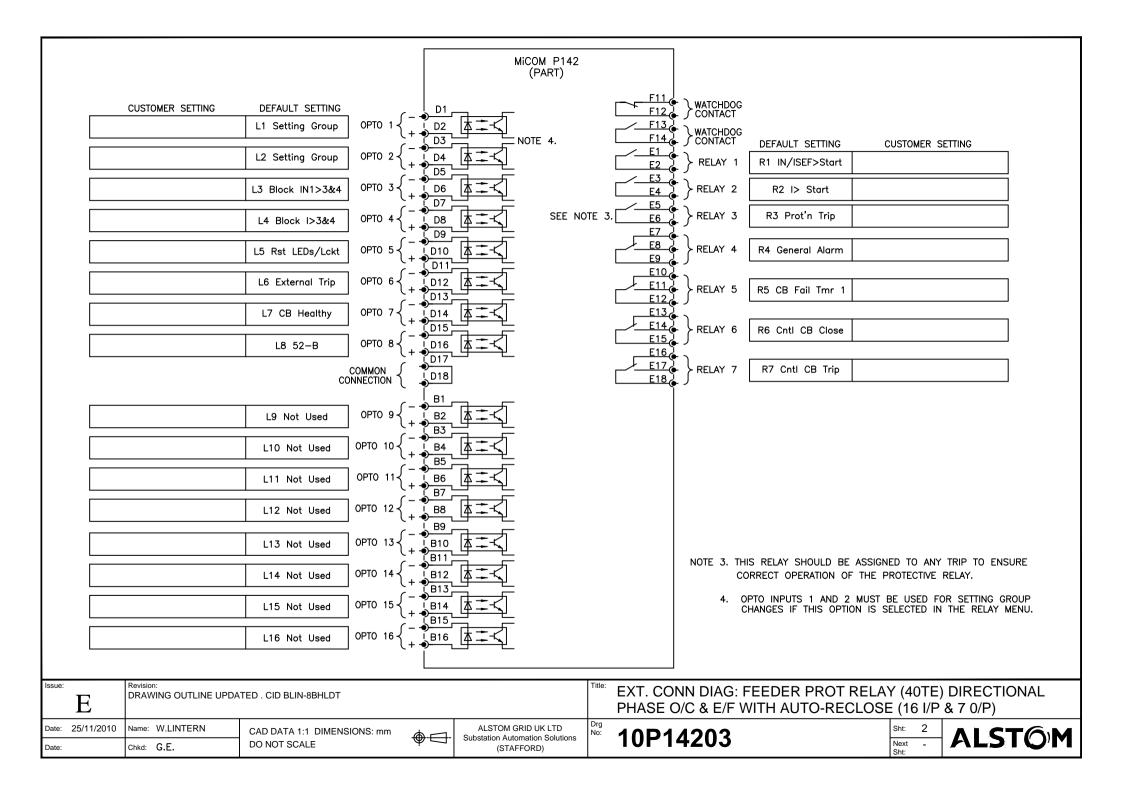
Chkd: G.E.

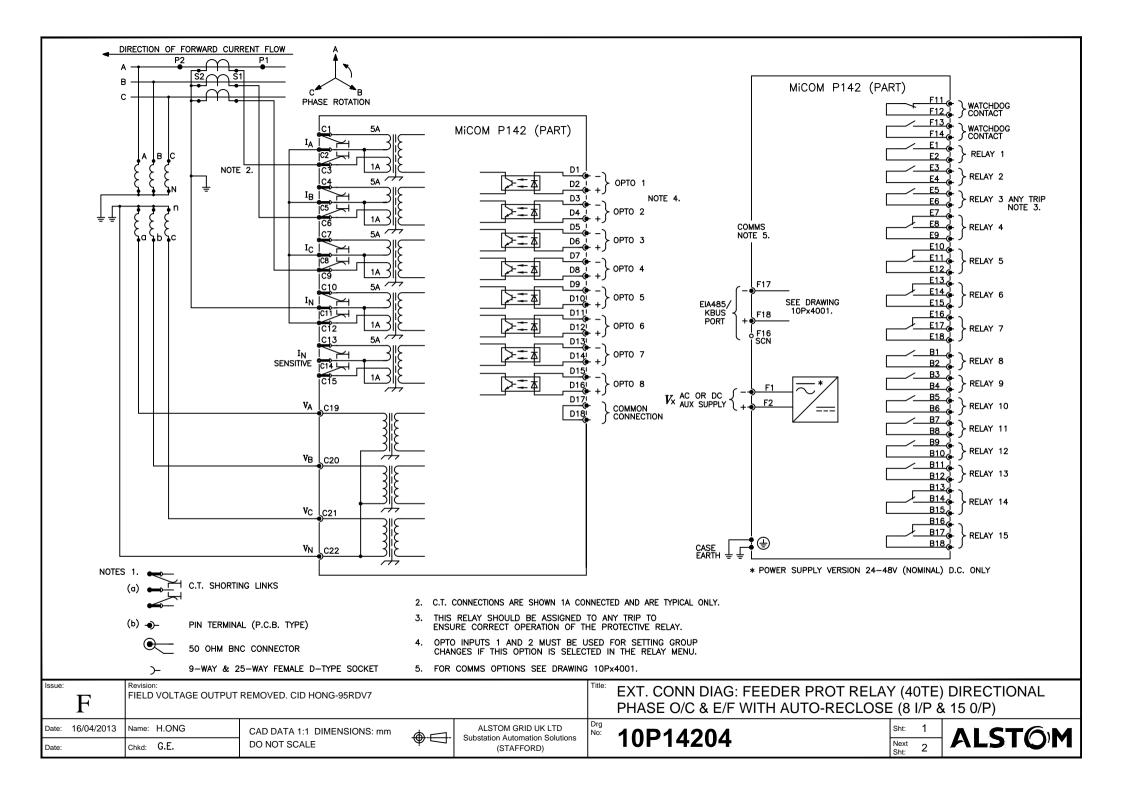
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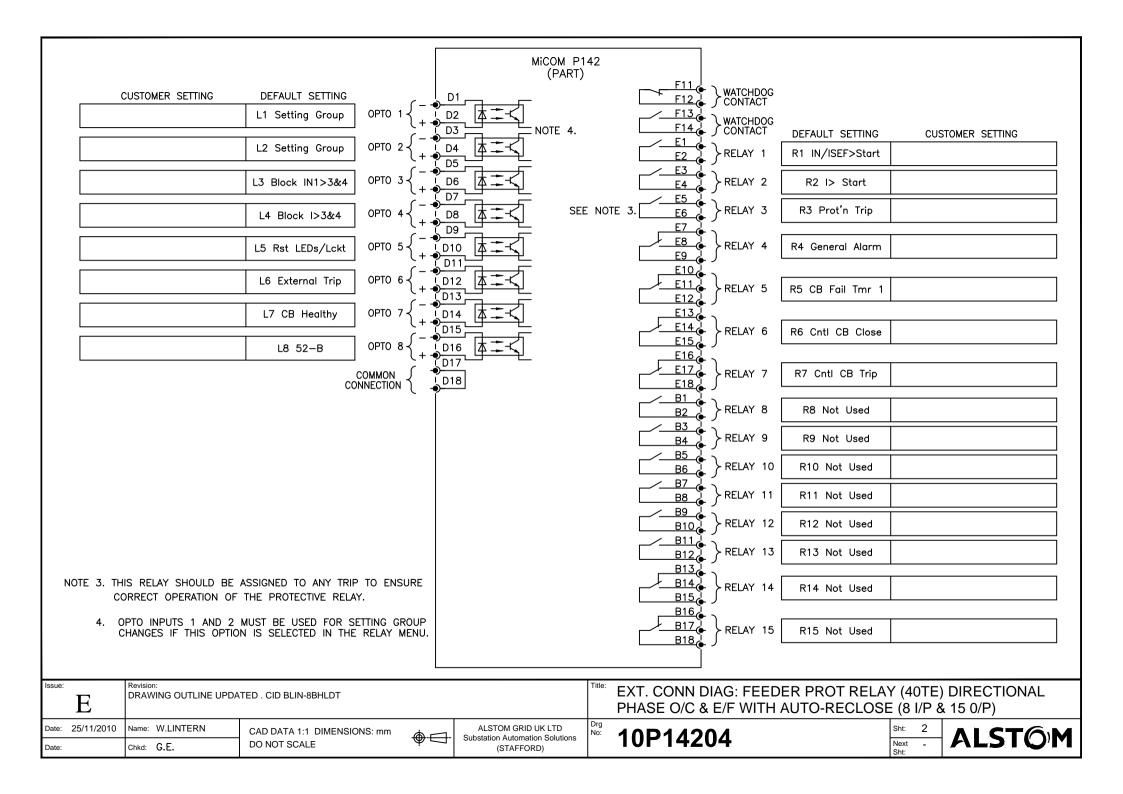
EXT.CONN DIAG: FEEDER PROT RELAY (40TE) DIRECTIONAL PHASE O/C & E/F WITH AUTO-RECLOSE (12 I/P & 11 0/P)

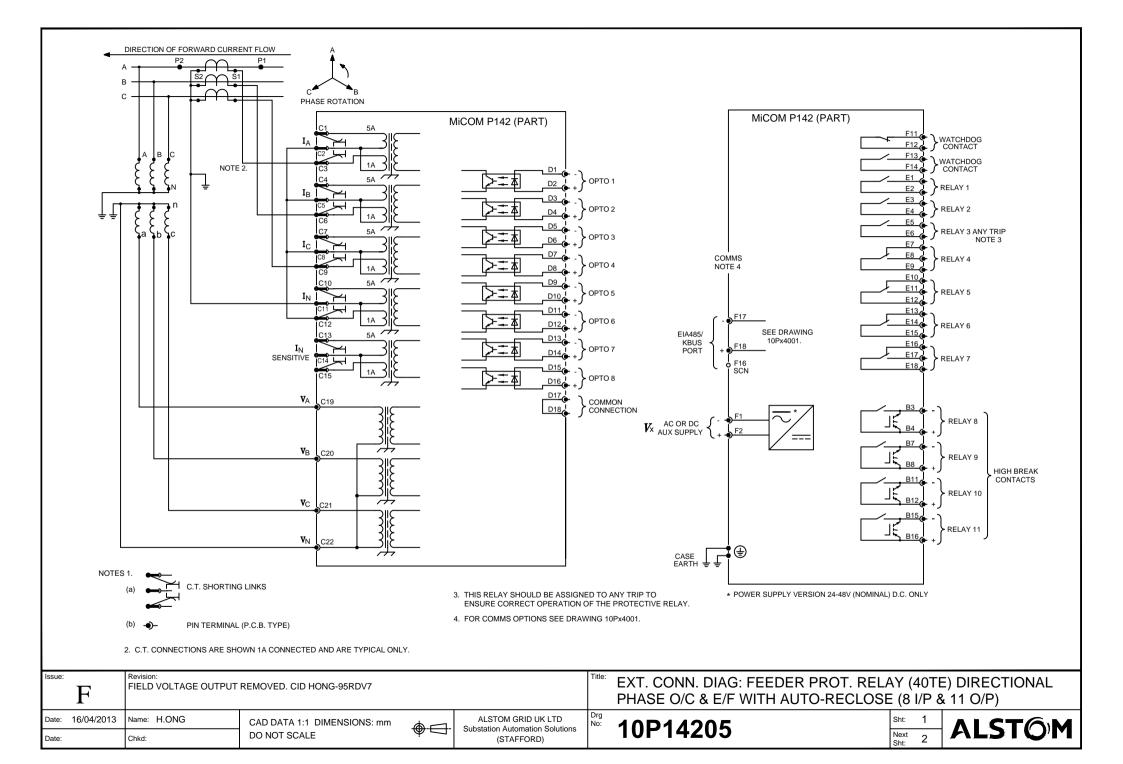
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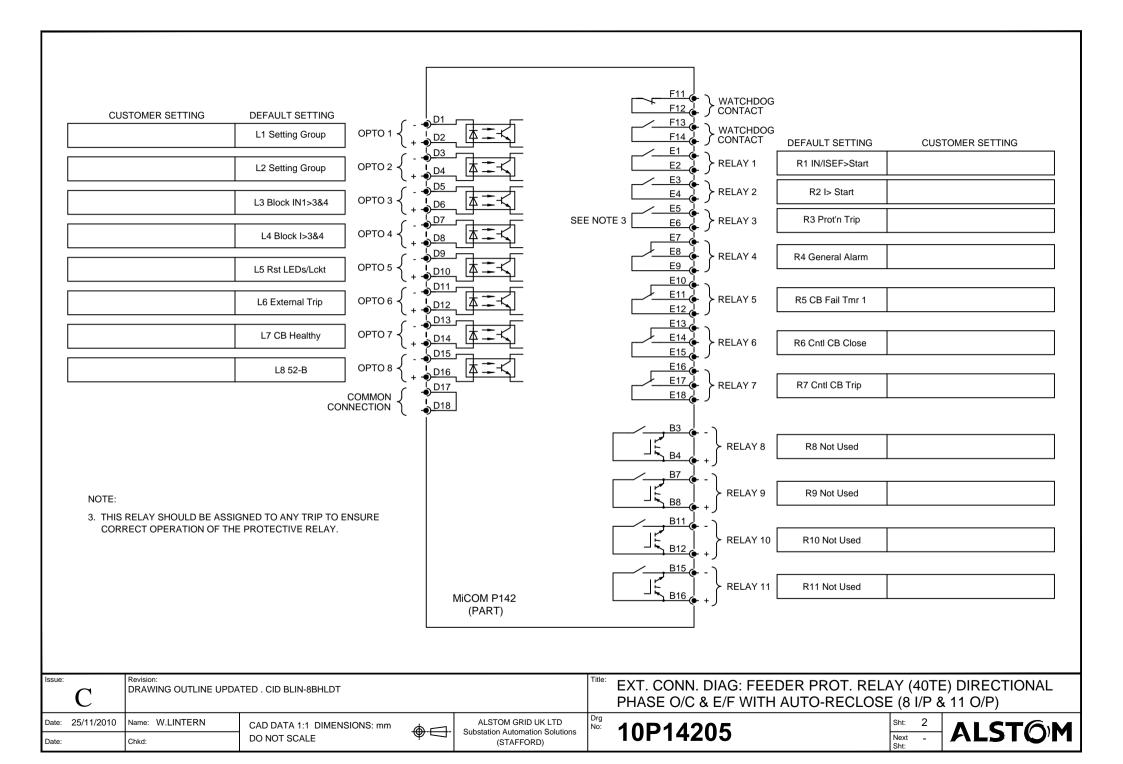
ALSTOM Next

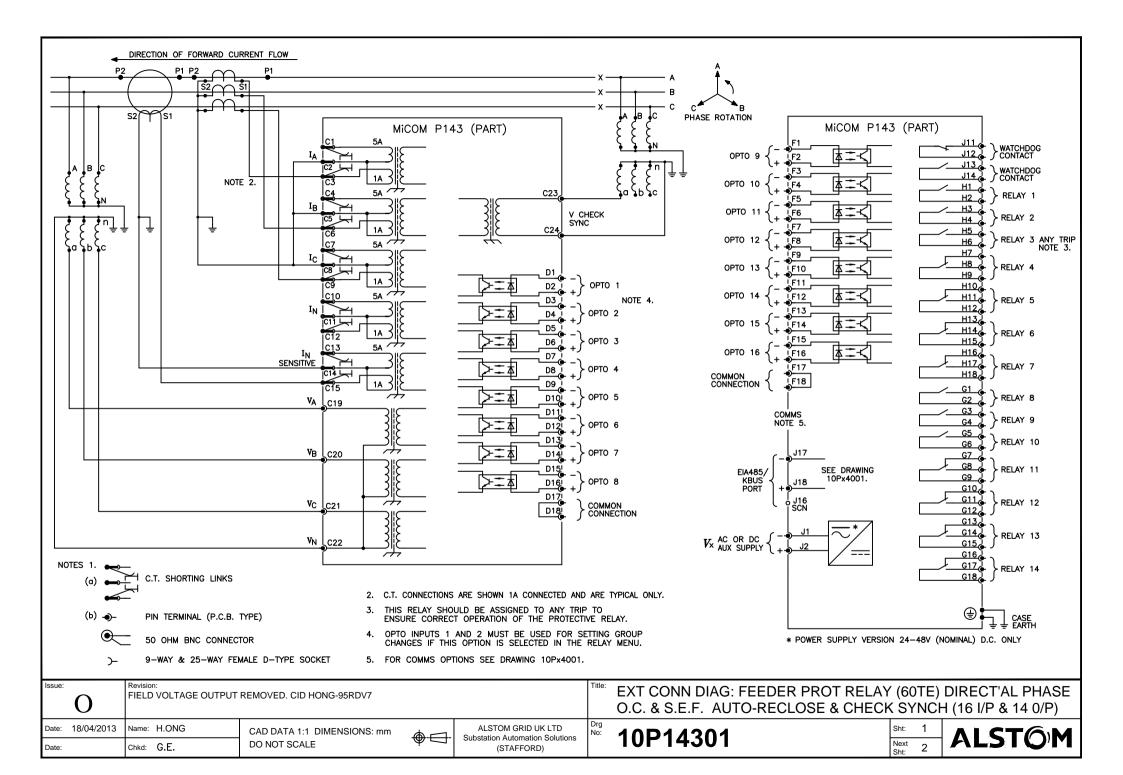


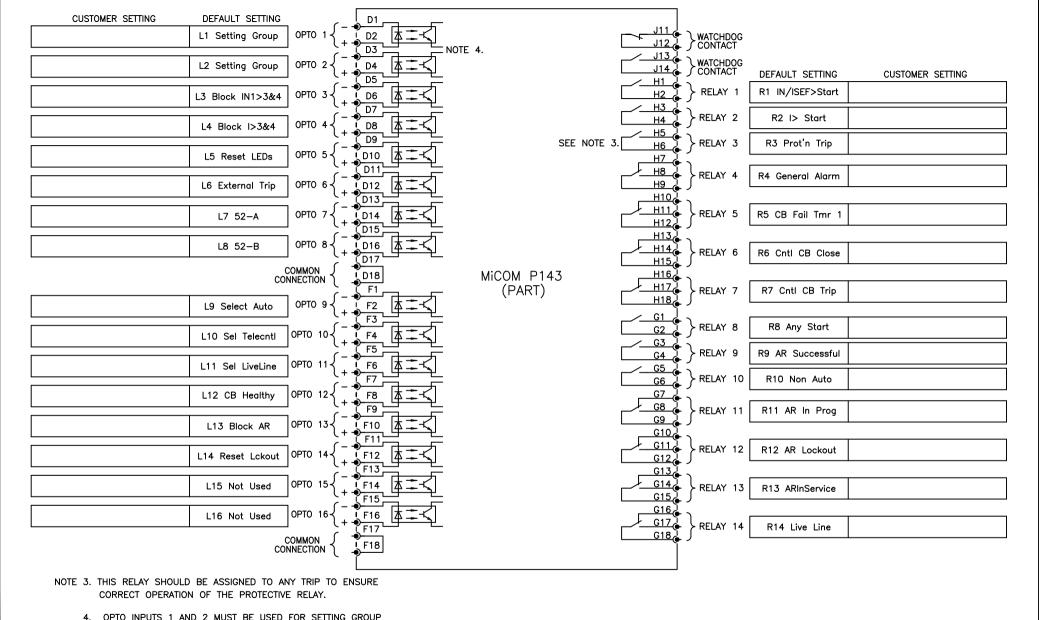












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4. OPTO INPUTS 1 AND 2 MUST BE USED FOR SETTING GROUP

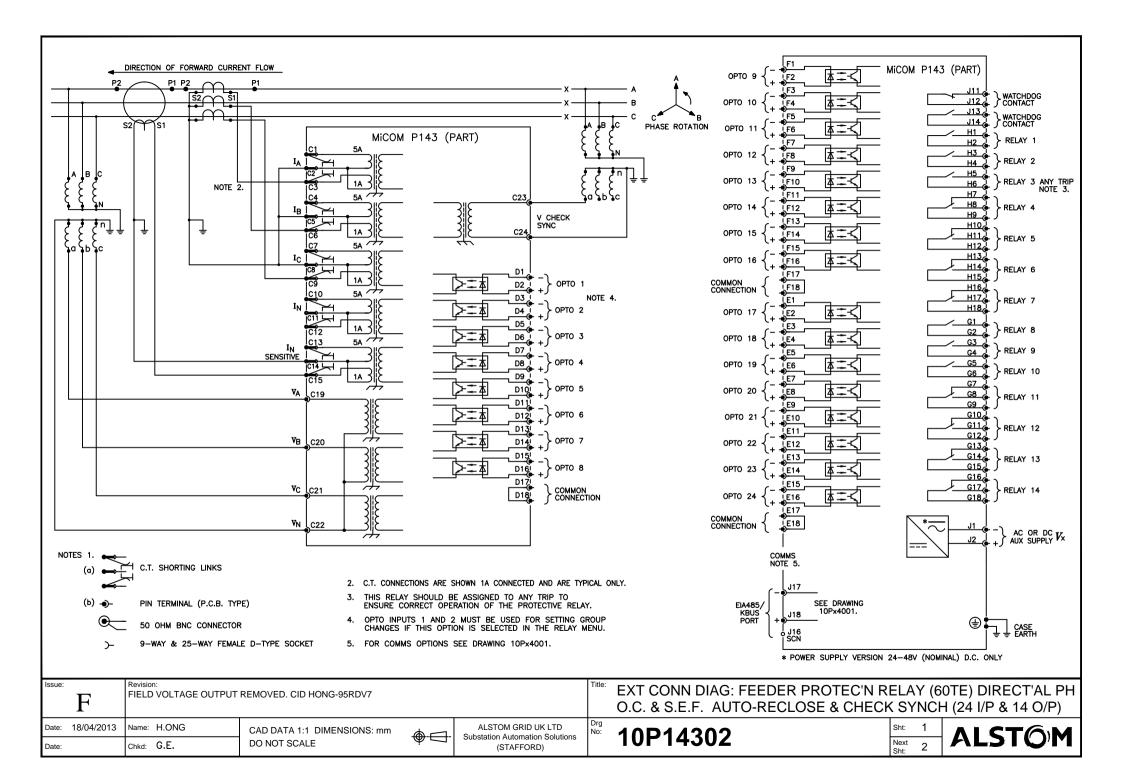
CHANGES IF THIS OPTION IS SELECTED IN THE RELAY MENU.

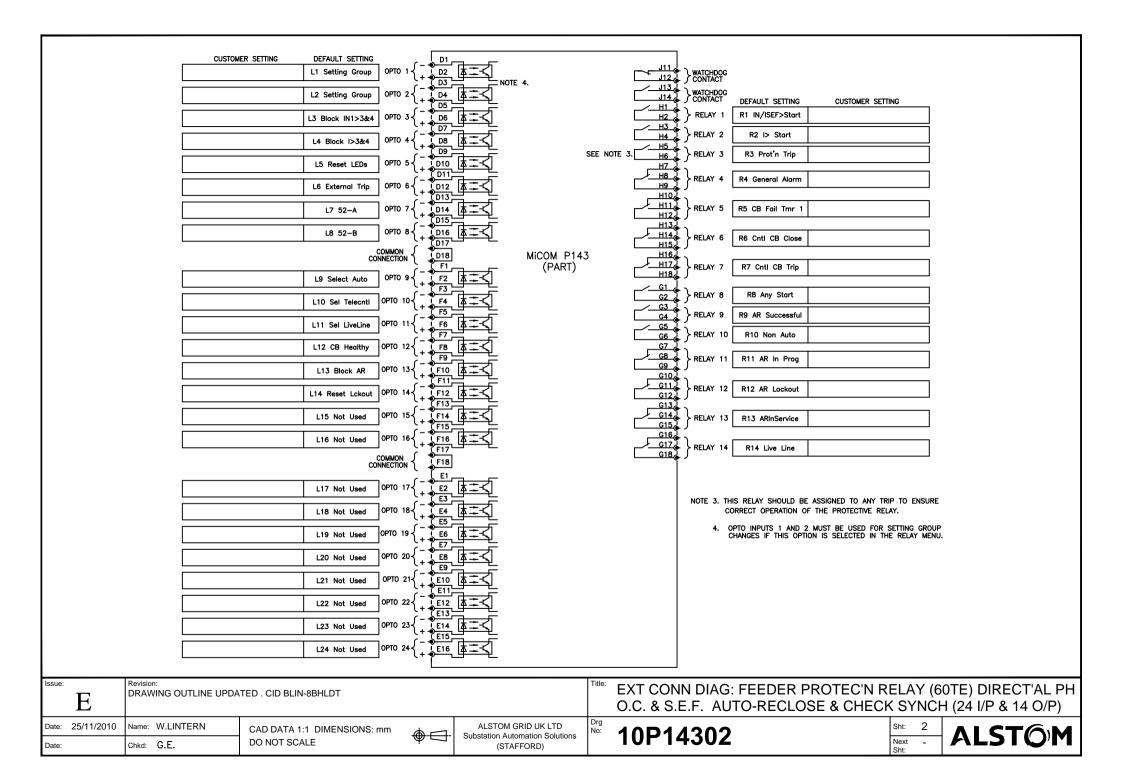
Issue: DRAWING OUTLINE UPDATED . CID BLIN-8BHLDT (ì Date: 25/11/2010 Name: W.LINTERN ALSTOM GRID UK LTD CAD DATA 1:1 DIMENSIONS: mm Substation Automation Solutions DO NOT SCALE Chkd: G.E.

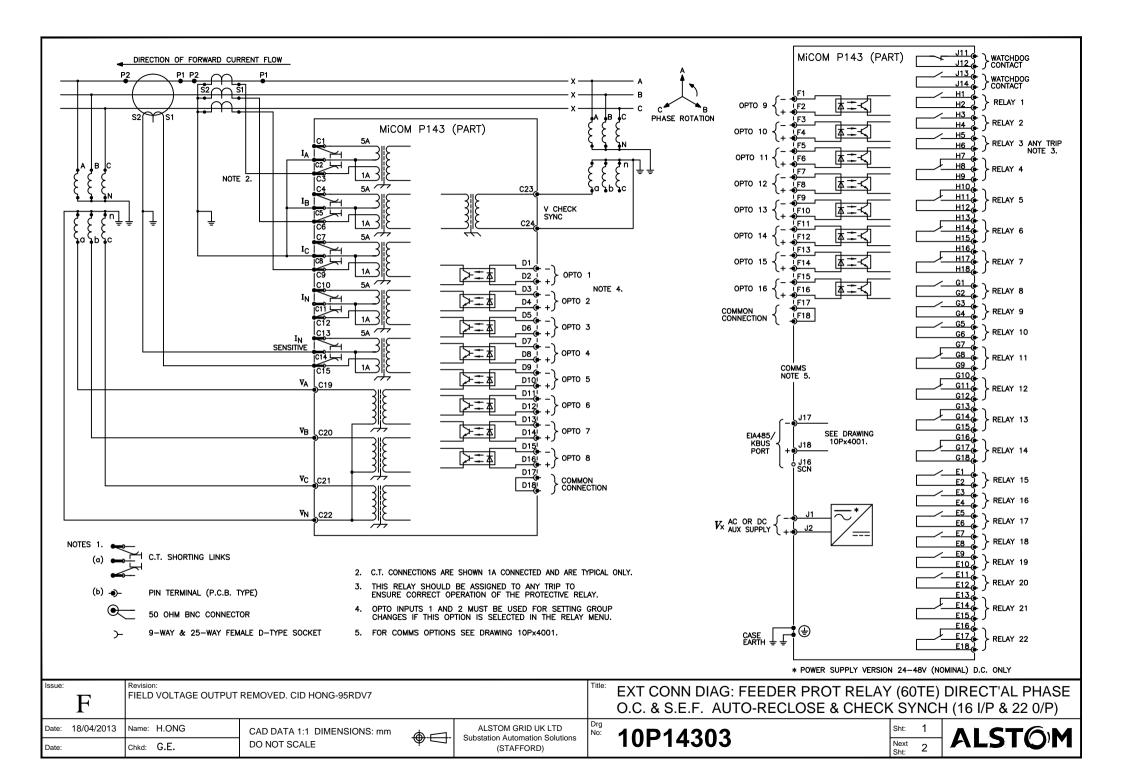
EXT CONN DIAG: FEEDER PROT RELAY (60TE) DIRECT'AL PHASE O.C. & S.E.F. AUTO-RECLOSE & CHECK SYNCH (16 I/P & 14 0/P)

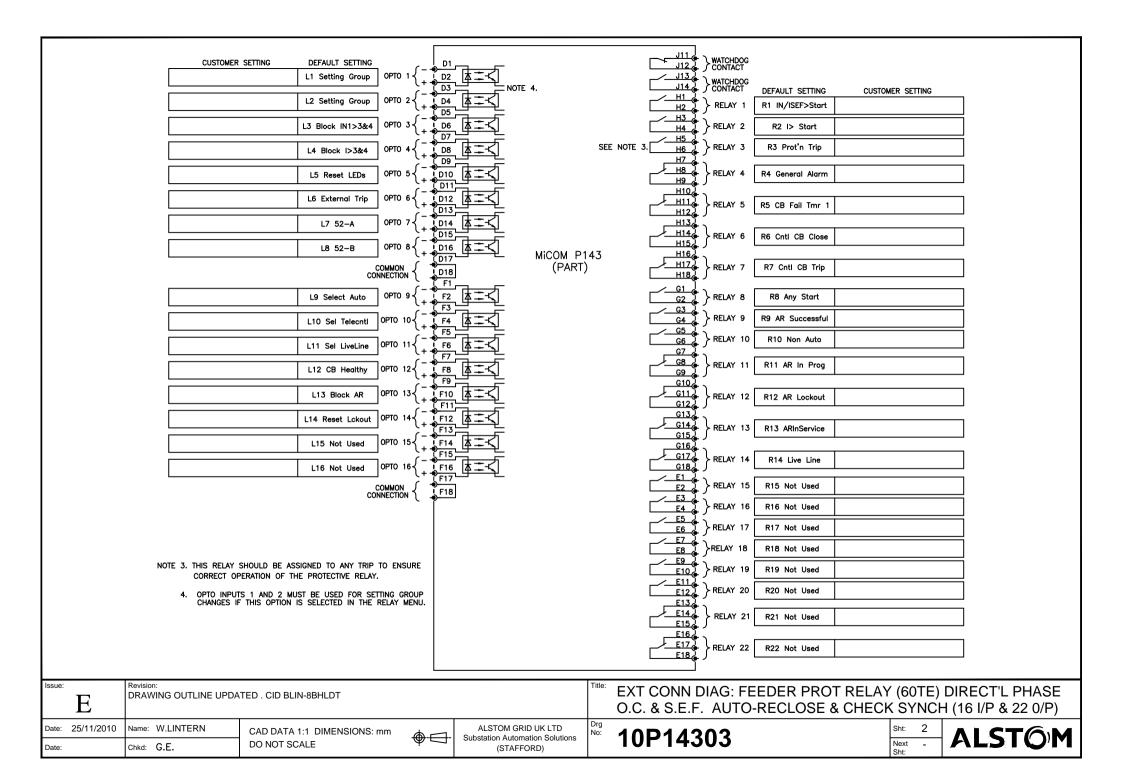
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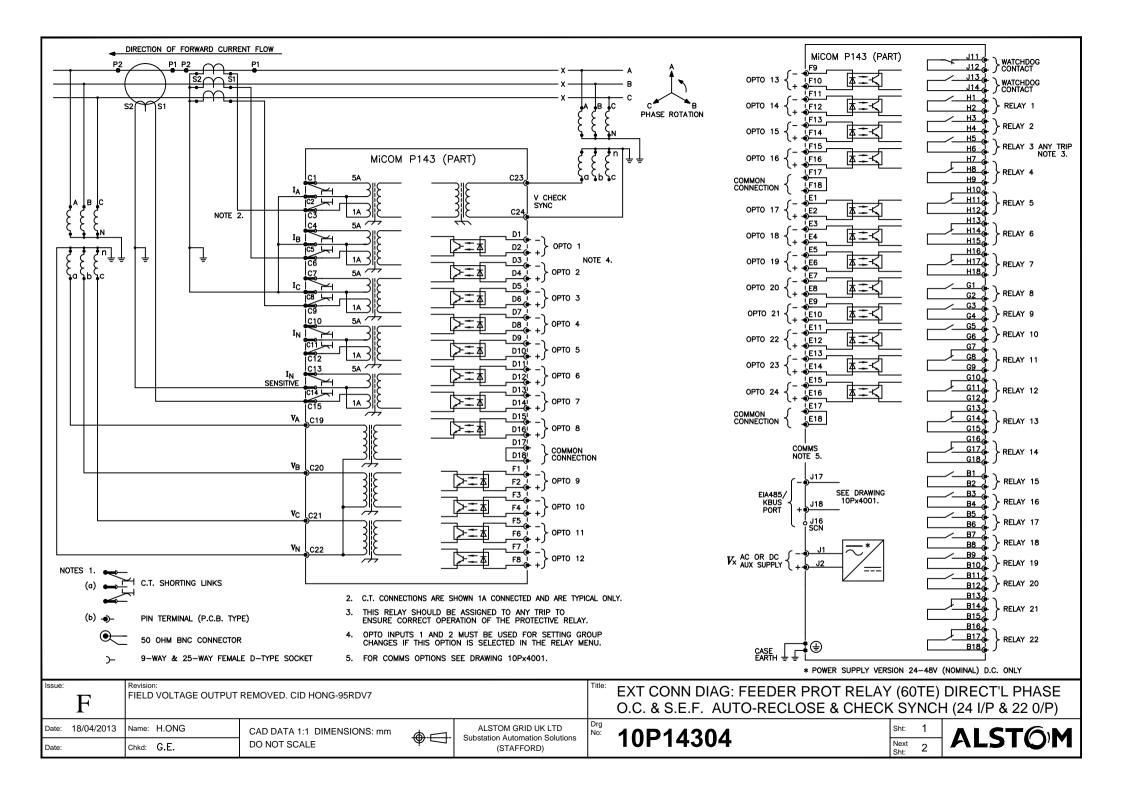
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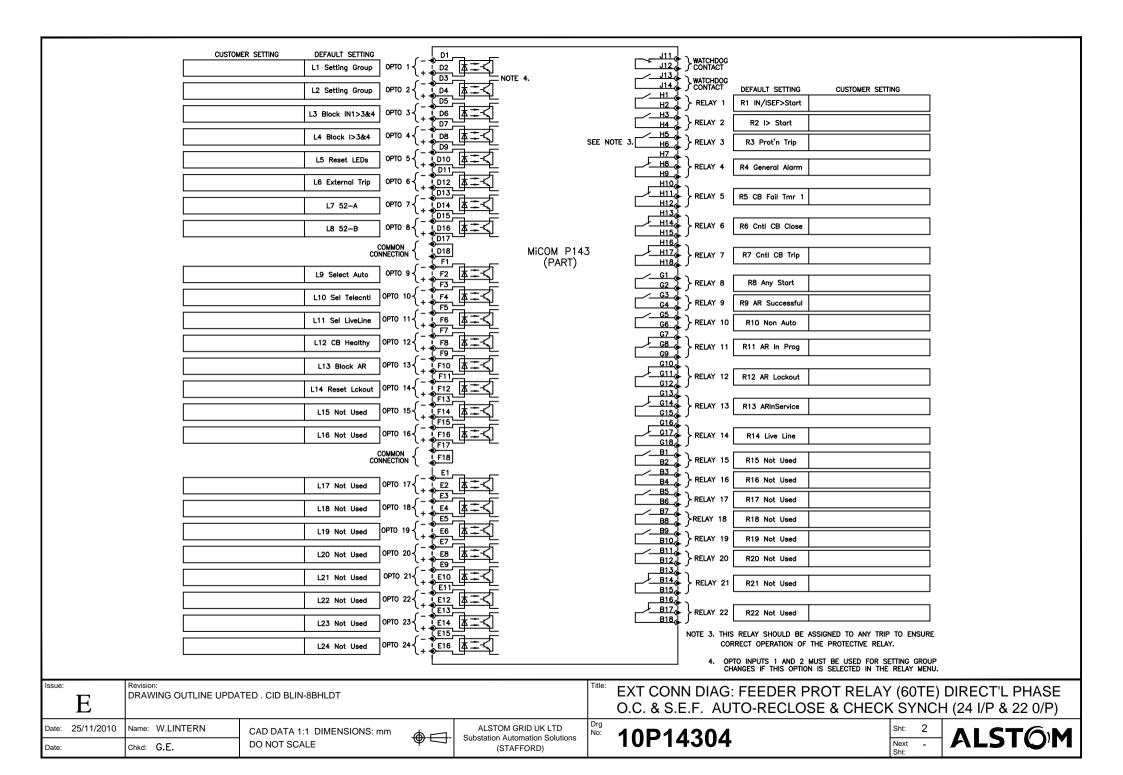


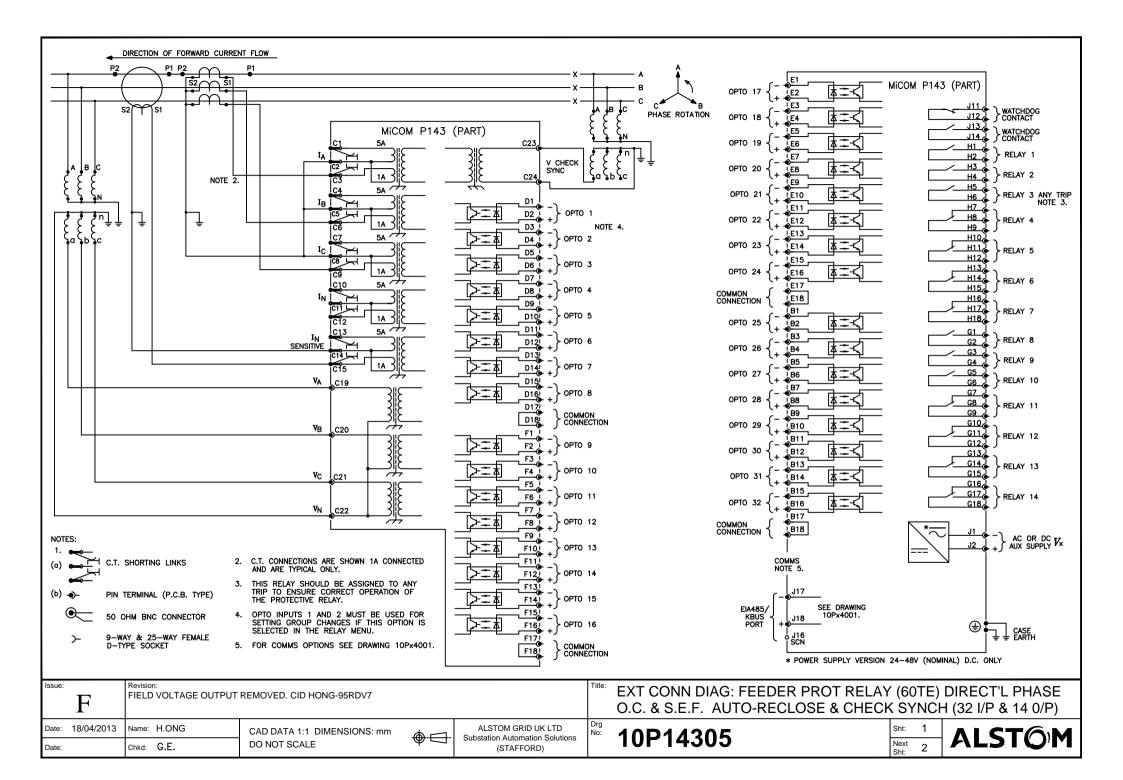












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10P14305

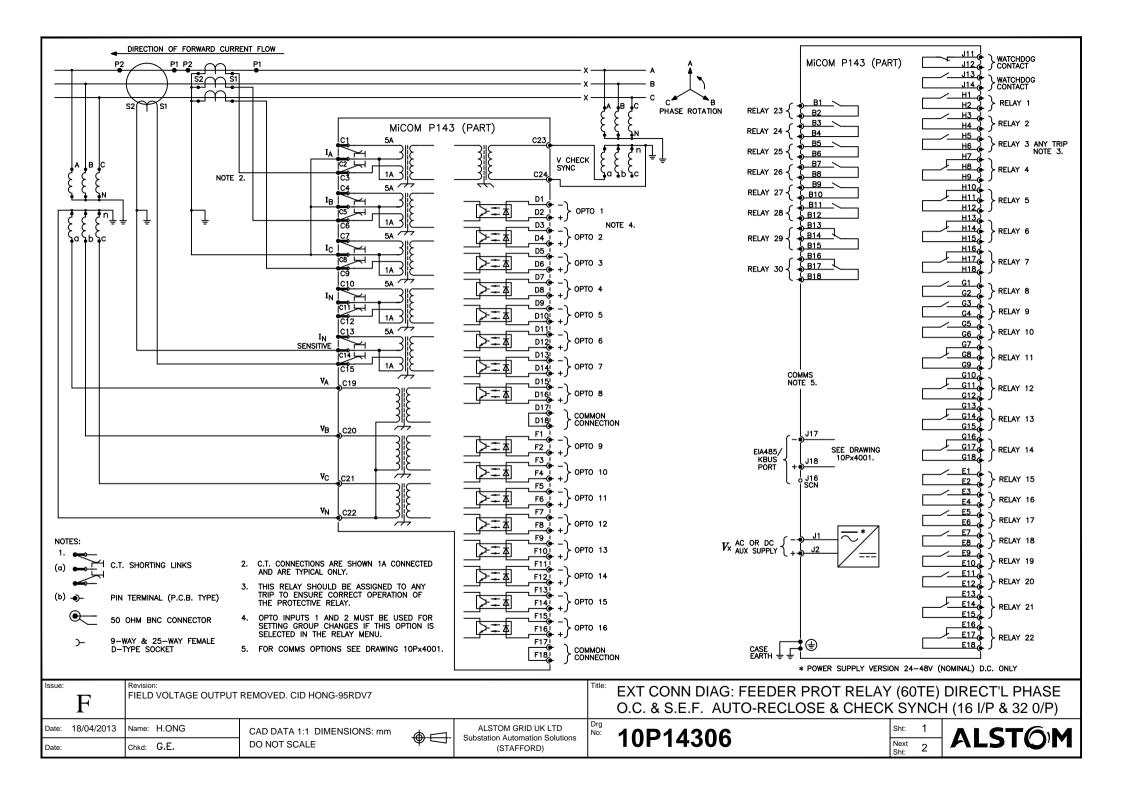
7 Sht: Next Sht:

ALSTOM EXT CONN DIAG: FEEDER PROT RELAY (60TE) DIRECT'L PHASE

O.C. & S.E.F. WITH AUTO-RECLOSE & CHECK SYNCH

WITCHINGE CUSTOMER SETTING CUSTOMER SETTING CUSTOMER SETTING CUSTOMER SETTING CUSTOMER SETTING RELAY RELAX R	
MICON P143 MICON	
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lssne:		Revision:		
	口	DRAWING OUTLINE UPDATED . CID BLIN-8BHLDT	TED . CID BLIN-8BHLDT	
Date:	Date: 25/11/2010	Name: W.LINTERN	CAD DATA 1:1 DIMENSIONS: mm A ALSTOM GRID UK LTD	ALSTOM GRID UK LTD
Date:		Chkd: G.E.	DO NOT SCALE	Substation Automation Solutions (STAFFORD)



Drg No:

10P14306

7 Next Sht: Sht:

ALSTOM

EXTERNAL CONN. DIAGRAM: FEEDER PROTECTION RELAY (60TE) Title:

O.C. & S.E.F. WITH AUTO—RECLOSE & CHECK SYNCH (16 I/P & 32 0/P)

VWYCHDOG VWYCHDOG COWTACT COWT	R1 IN/ISEF>Start	RELAY 2 R2 I> Start	RELAY 3 R3 Prot'n Trip	RELAY 4 R4 General Alarm	RELAY 5 R5 C8 Fail Tmr 1	RELAY 6 R6 Cntl CB Close] [RELAY 7 R7 Cntl CB Trip	RELAY 8 R8 Any Start	RELAY 9 R9 AR Successful	RELAY 10 R10 Non Auto	RELAY 11 R11 AR In Prog	RELAY 12 R12 AR Lockout	RELAY 13 R13 ARInService	」 !	RELAY 14 R14 Live Line	RELAY 15 R15 Not Used	RELAY 16 R16 Not Used	RELAY 17 R17 Not Used	-RELAY 18 R18 Not Used	RELAY 19 R19 Not Used	RELAY 20 R20 Not Used	RELAY 21 R21 Not Used	RELAY 22 R22 Not Used	RELAY 23 R23 Not Used	⅃Ĺ	RELAY 25 R25 Not Used
01 			SEE NOTE 3.	·			DIF ATT MICOM P143	(PARI)							∏.					^_ ••	╱╴╭ ┷╼┷┈	╱╲ ╽ ╱┪╱	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		<u> </u>	╮╭∕╮ ₅╌ፅ╌ፅ	
CUSTOMER SETTING DEFAULT SETTING LI Setting Group OPTO 1 { - •	12 Setting Group OPTO 2 + +	L3 Block IN1>3&4 OPTO 3 { + 4	L4 Block I>3&4 OPTO 4 { +	L5 Reset LEDs OPTO 5 { - **	L6 External Trip OPTO 6 +		٠ ــــــــــــــــــــــــــــــــــــ	COMMON	L9 Select Auto OPTO 9 { -	L10 Sel Telecntl OPTO 10	L11 Sel LiveLine OPTO 11	CB Healthy					COMMON										NOTE 3. THIS RELAY SHOULD BE ASSIGNED TO ANY TRIP TO ENSURE CORRECT OPERATION OF THE PROTECTIVE RELAY.

4. OPTO INPUTS 1 AND 2 MUST BE USED FOR SETTING GROUP CHANGES IF THIS OPTION IS SELECTED IN THE RELAY MENU.

-	

R29 Not Used R30 Not Used

| B10 | RELAY 27 | E110 | B110 | B110

R26 Not Used R27 Not Used R28 Not Used

RELAY 26

Re		
lssue:	E	

Date:

Date:

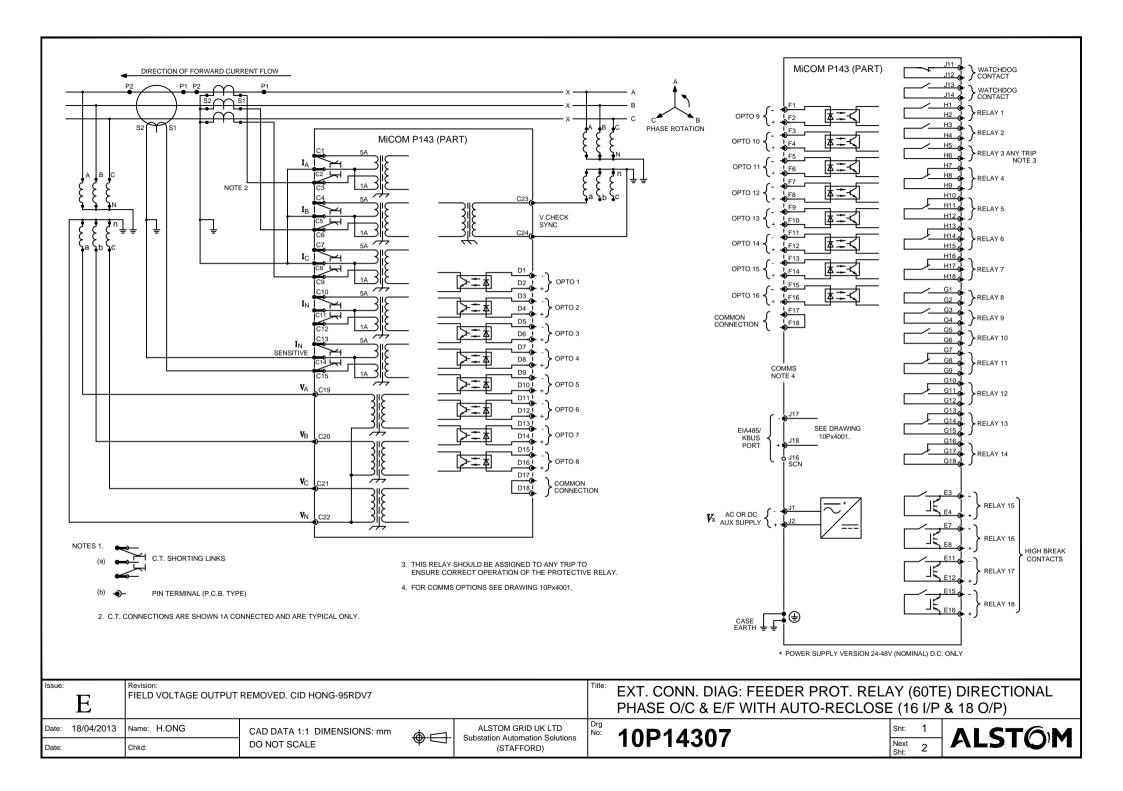
Revision: DRAWING OUTLINE UPDATED . CID BLIN-8BHLDT

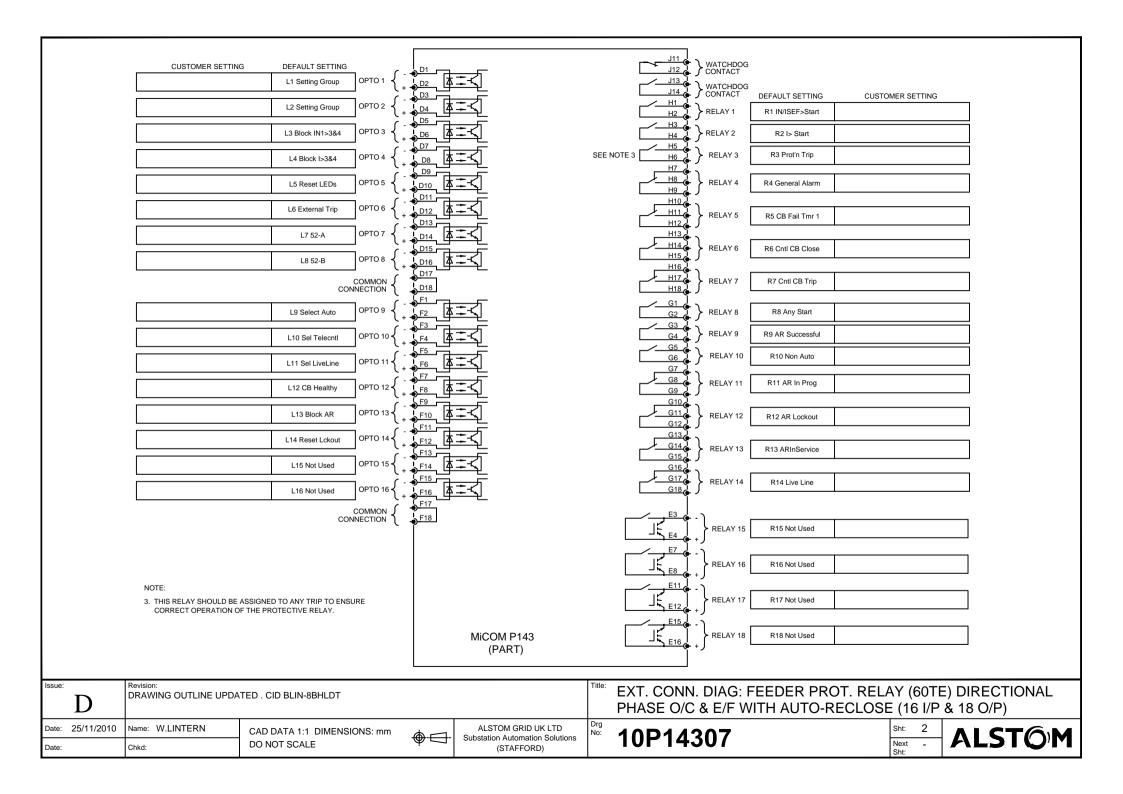
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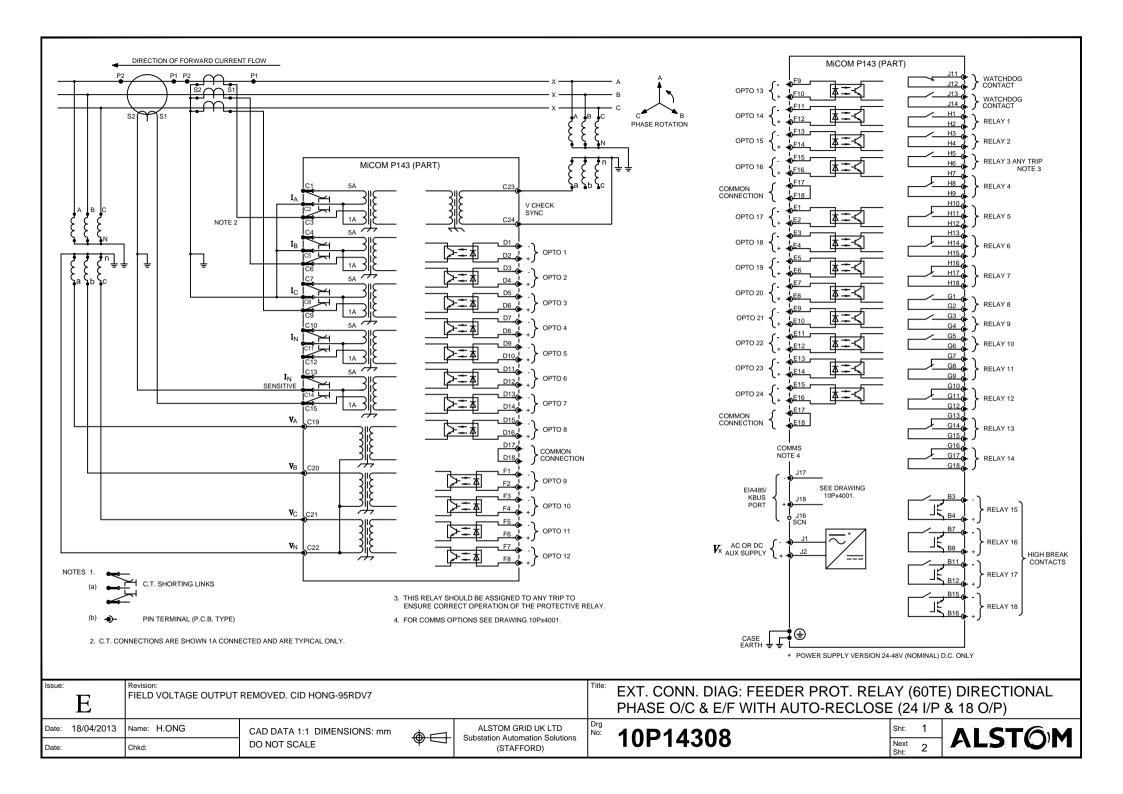
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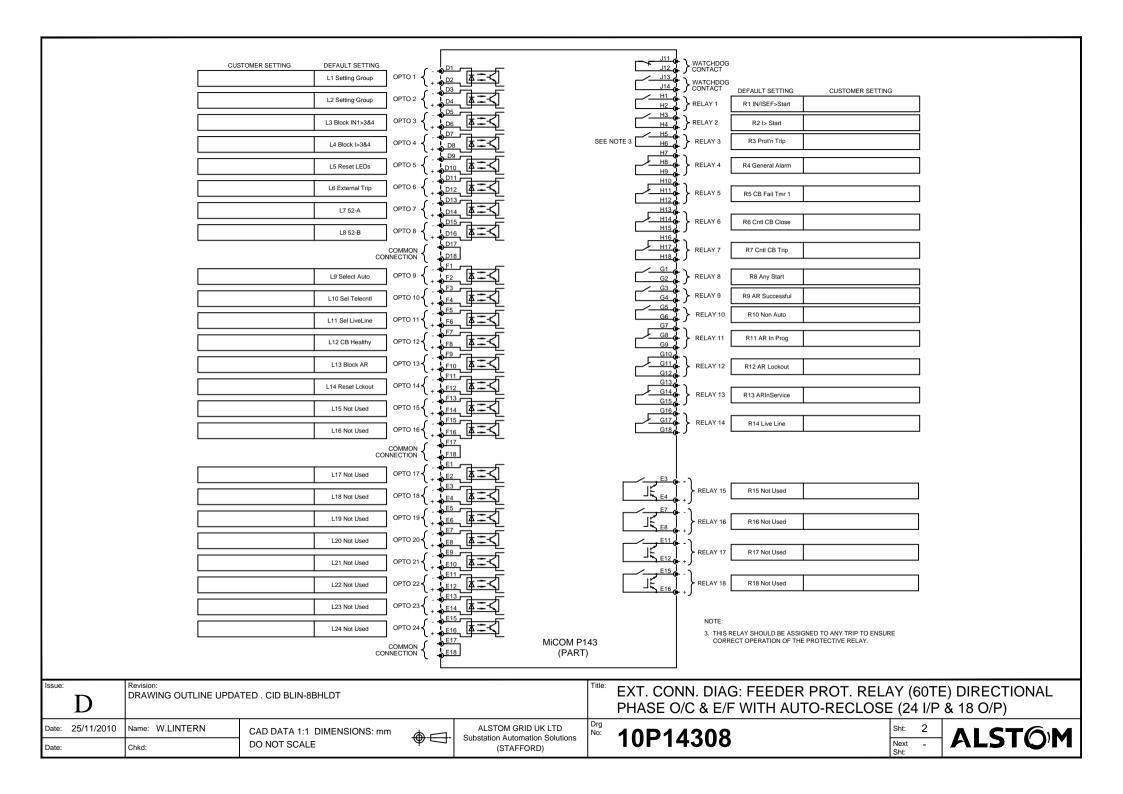


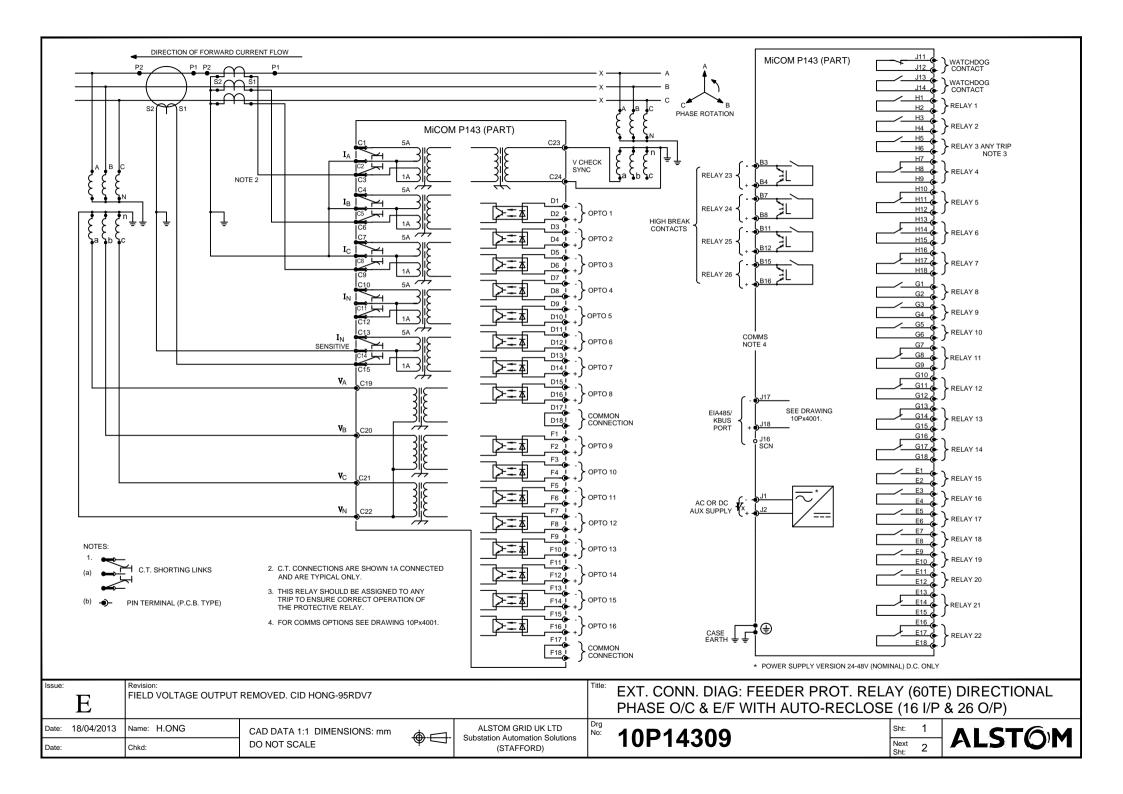
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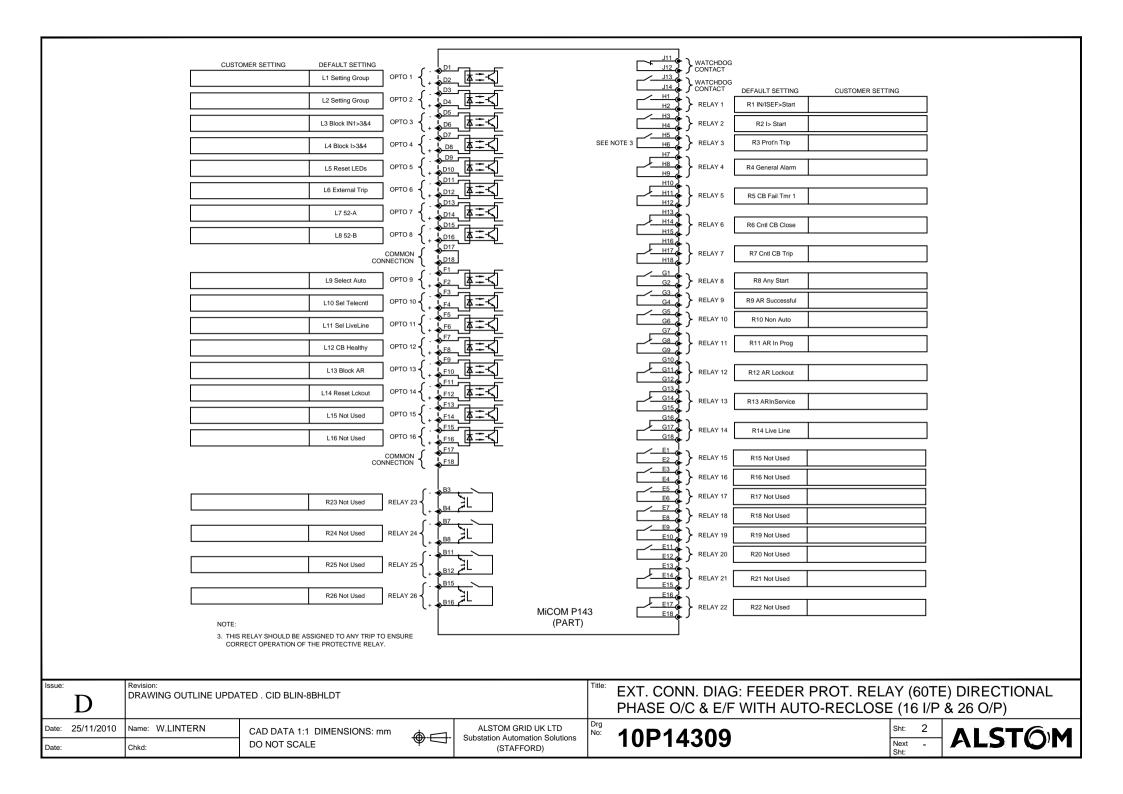


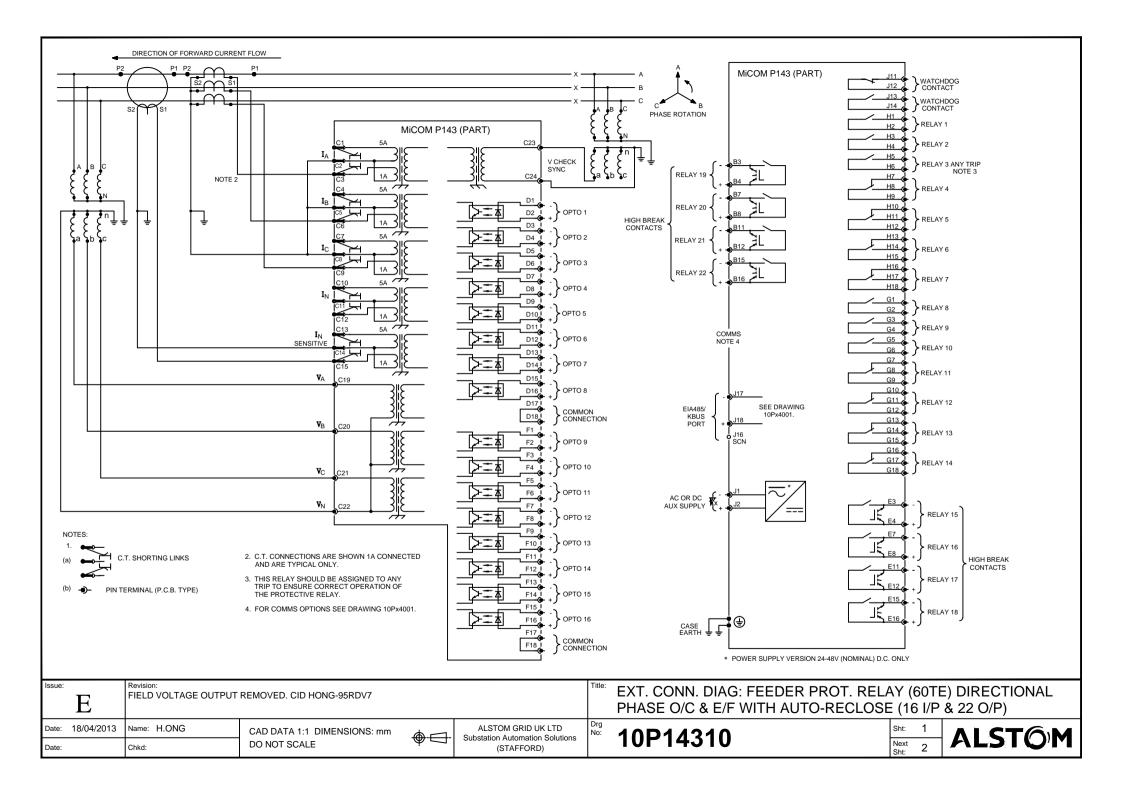


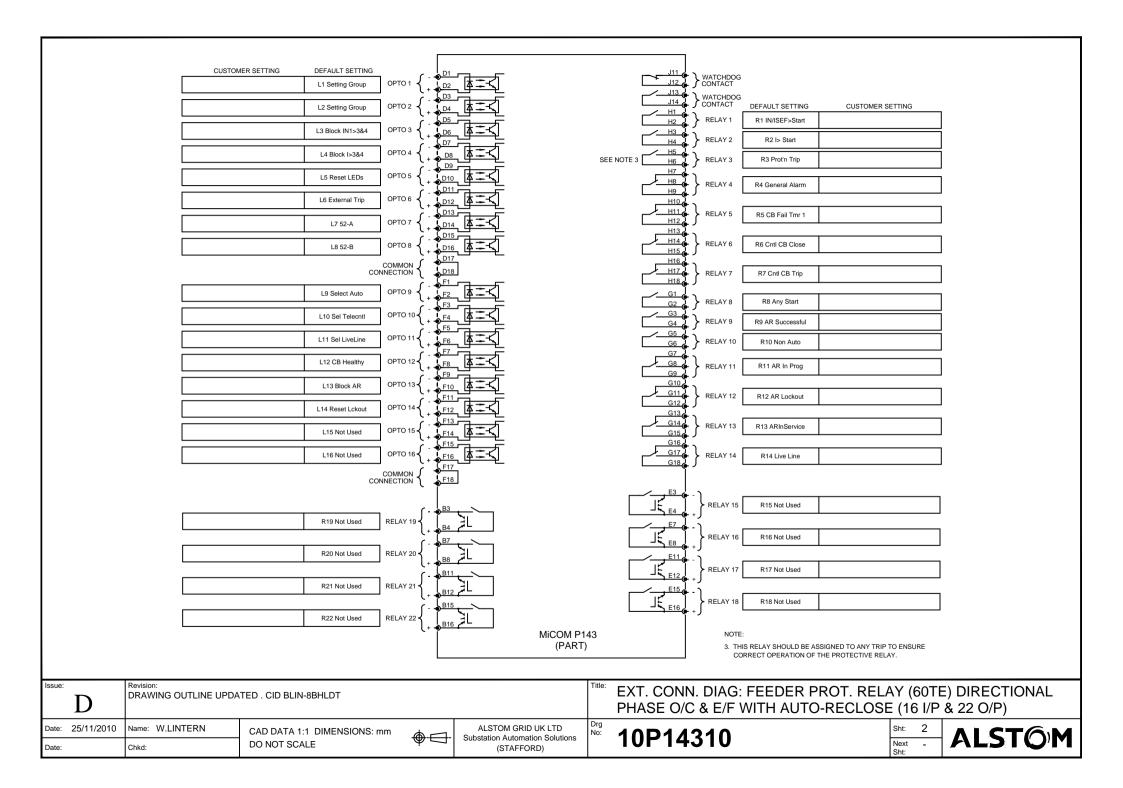


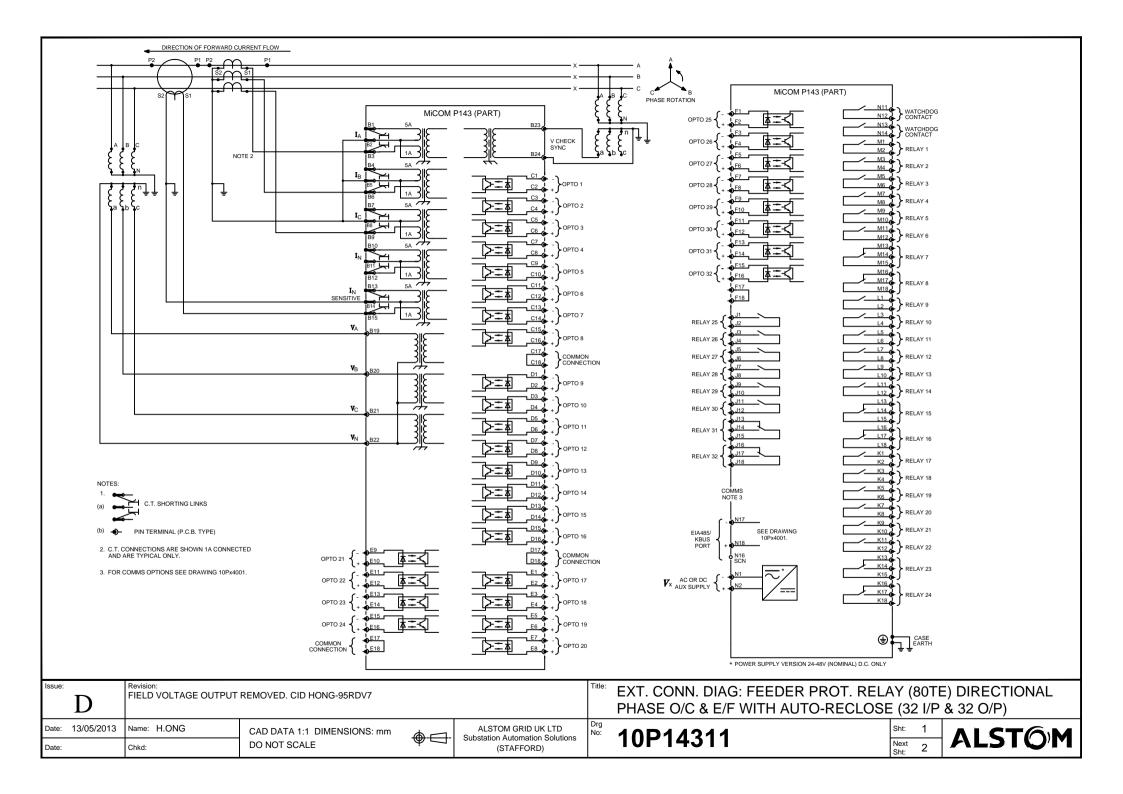


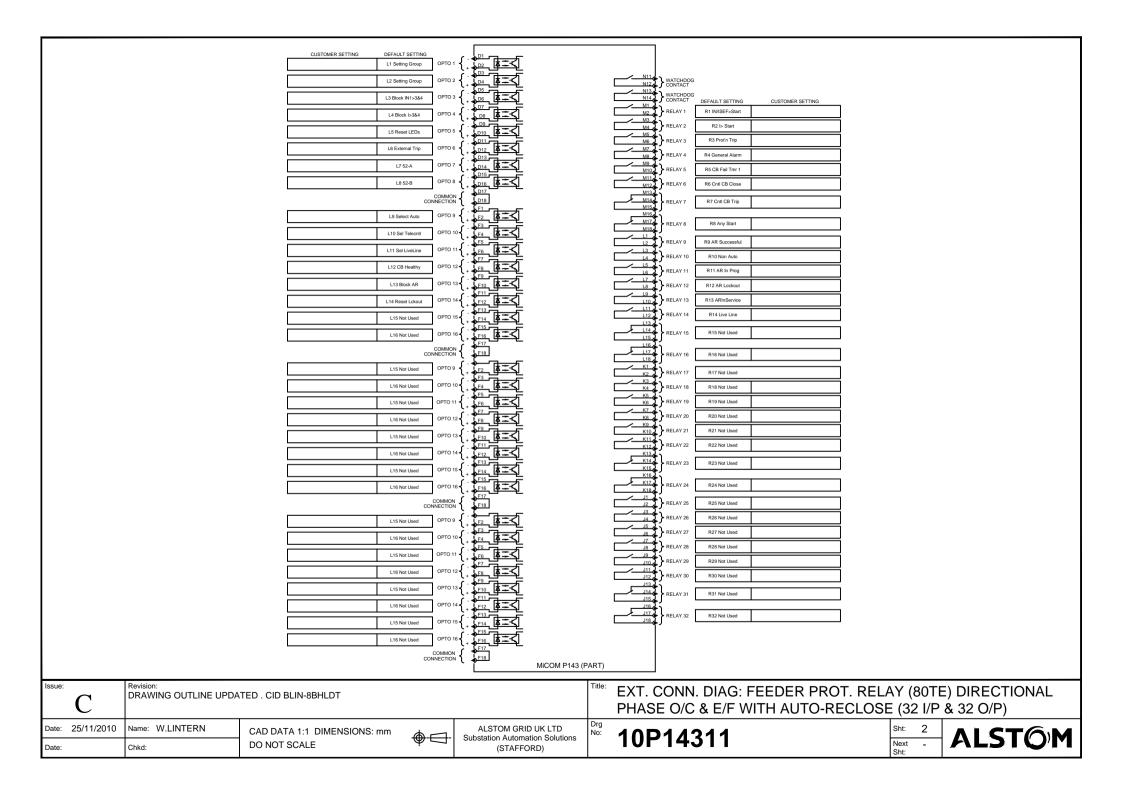


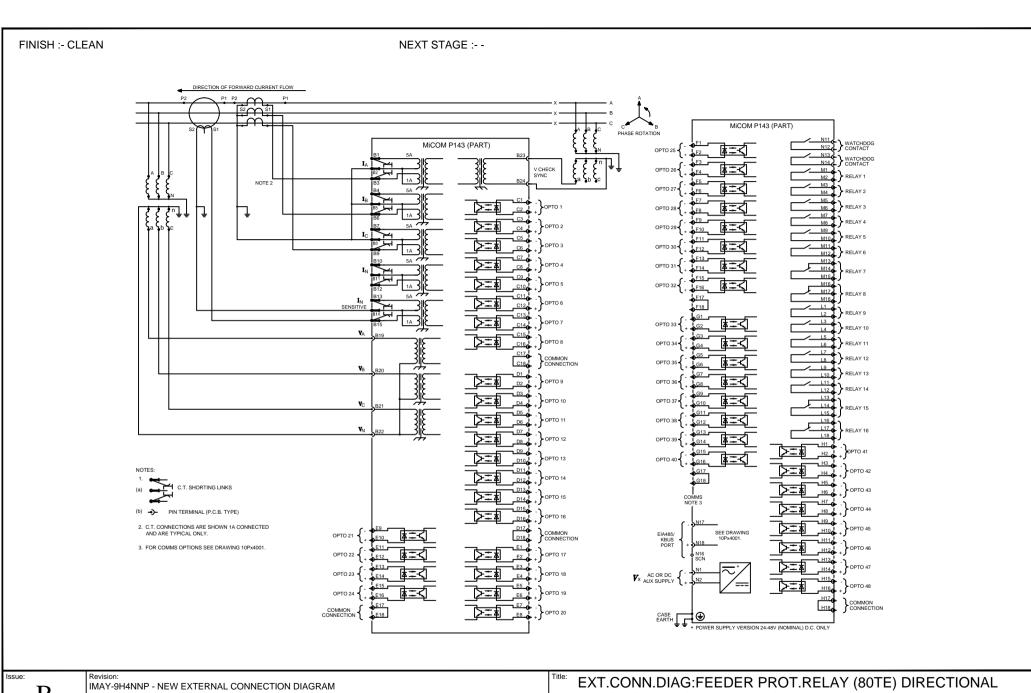




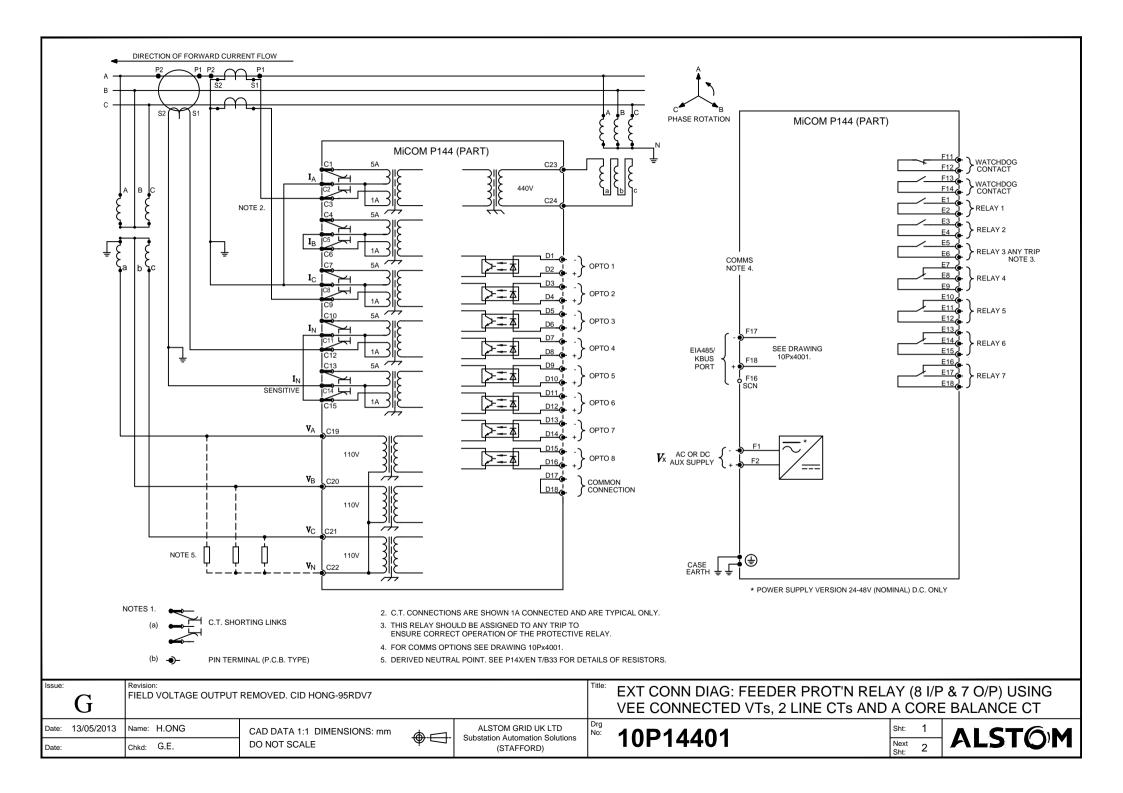


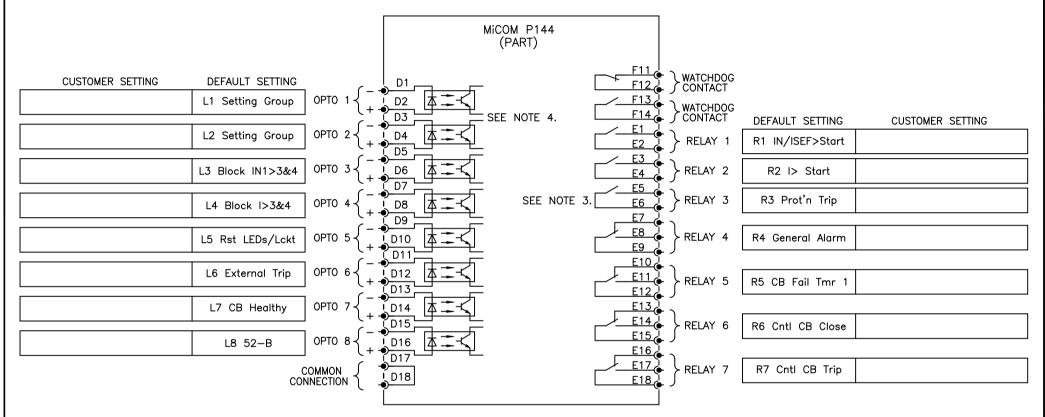






В	IMAY-9H4NNP - NEW EXT	ERNAL CONNECTION DIAGRAM				PHASE O/C & E/F WITH AUTO-RECLOS	,	
Date: 11/04/2014	Name: I.MAYER	CAD DATA 1:1 DIMENSIONS: mm	9	ALSTOM GRID UK LTD	Drg No:	10P14312	Sht: 1	ALCT
Date:	Chkd:	DO NOT SCALE	W -	(STAFFORD)		10F 143 1Z	Next 2	MLSI





NOTE 3. THIS RELAY SHOULD BE ASSIGNED TO ANY TRIP TO ENSURE CORRECT OPERATION OF THE PROTECTIVE RELAY.

Chkd: G.E.

4. OPTO INPUTS 1 AND 2 MUST BE USED FOR SETTING GROUP CHANGES IF THIS OPTION IS SELECTED IN THE RELAY MENU.

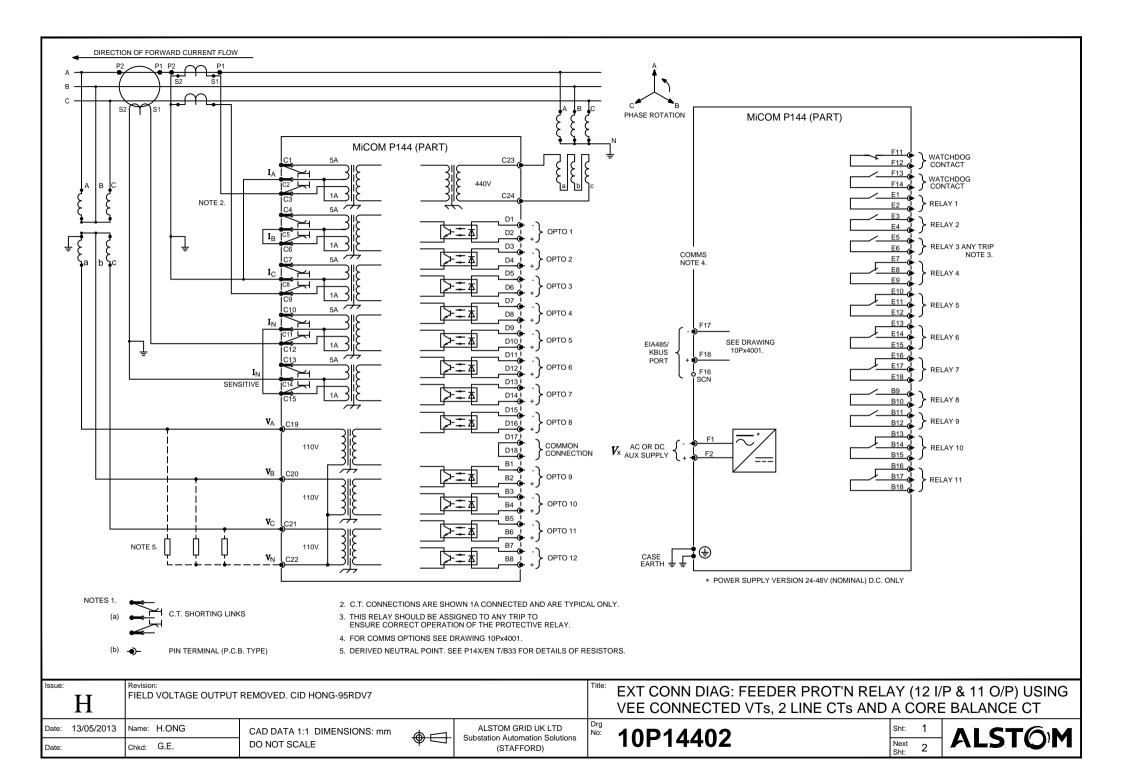
L									
		Revision: DRAWING OUTLINE UPDATED . CID BLIN-8BHLDT					EXT CONN DIAG: FEEDER PROT'N RELAY VEE CONNECTED VT's, 2 LINE CT's AND A		
	Date: 25/11/2010	Name: W.LINTERN	CAD DATA 1:1 DIMENSIONS: mm	+	ALSTOM GRID UK LTD Substation Automation Solutions	Drg No:	10P14401	Sh	
	Date:	Chkd: G.F.	DO NOT SCALE	\$	(STAFFORD)		IUF 1440 I		

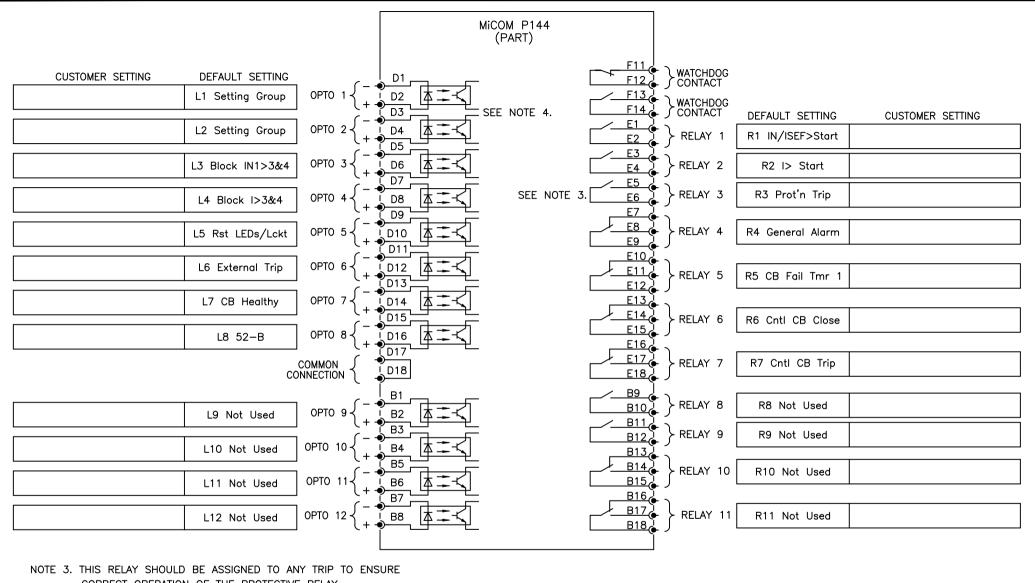
(STAFFORD)

AY (8 I/P & 7 O/P) USING A CORE BALANCE CT

Next







(STAFFORD)

CORRECT OPERATION OF THE PROTECTIVE RELAY.

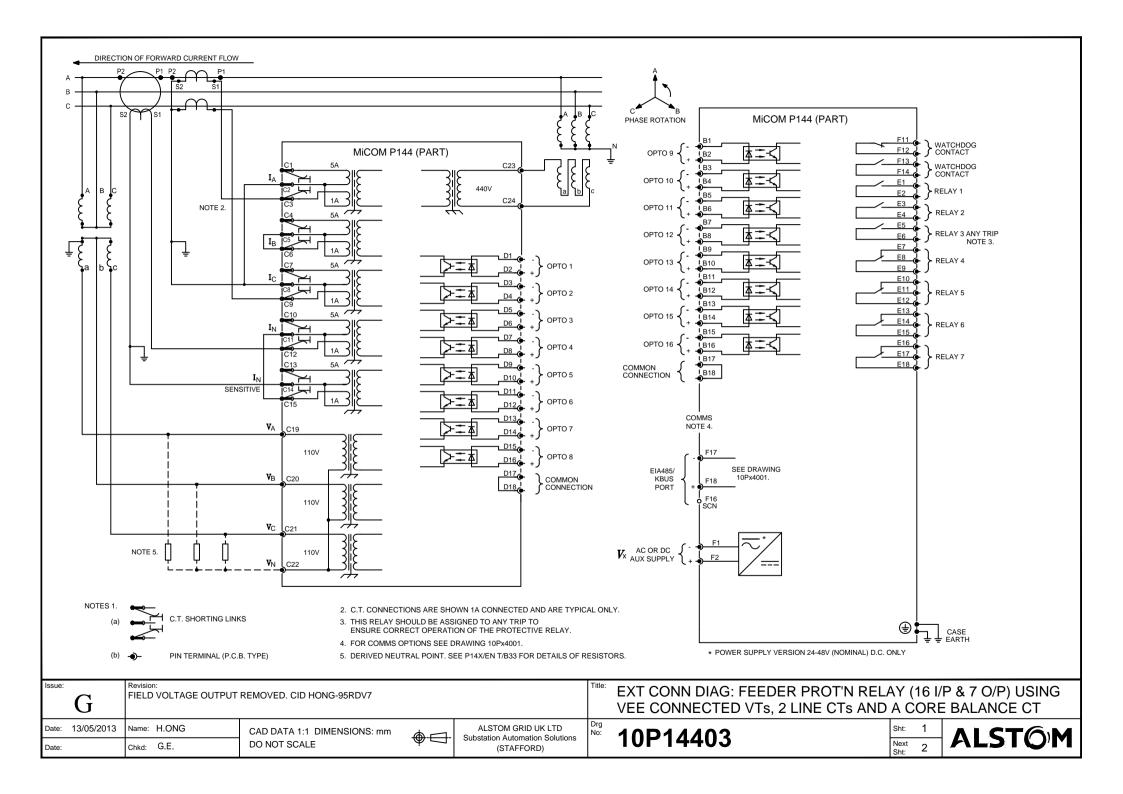
4. OPTO INPUTS 1 AND 2 MUST BE USED FOR SETTING GROUP CHANGES IF THIS OPTION IS SELECTED IN THE RELAY MENU.

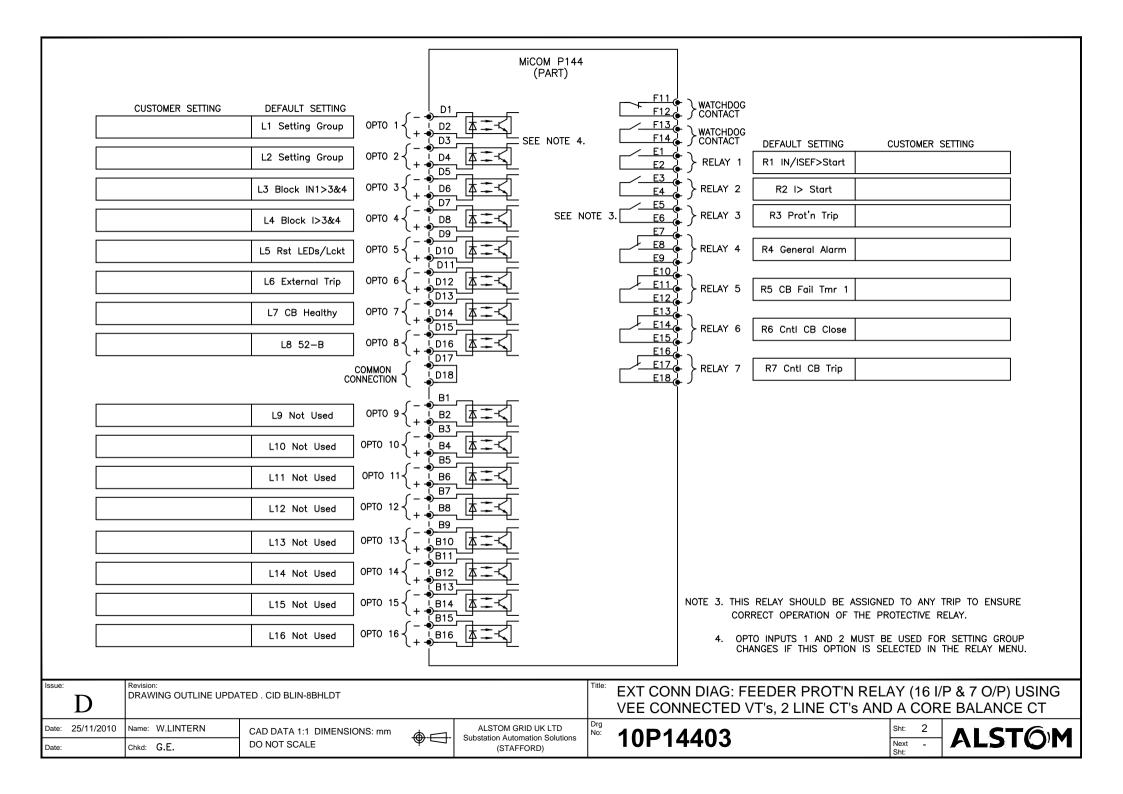
Issue: Revision: DRAWING OUTLINE UPDATED . CID BLIN-8BHLDT Date: 25/11/2010 Name: W.LINTERN ALSTOM GRID UK LTD CAD DATA 1:1 DIMENSIONS: mm Substation Automation Solutions DO NOT SCALE Chkd: G.E.

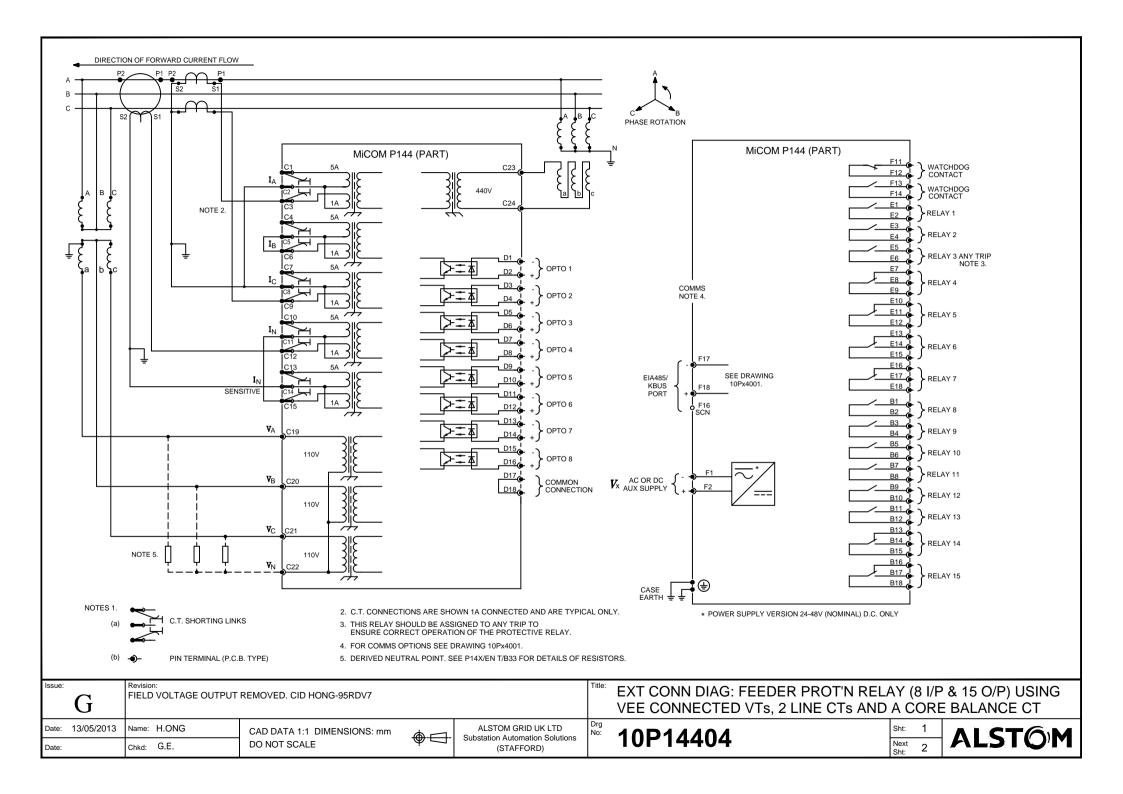
EXT CONN DIAG: FEEDER PROT'N RELAY (12 I/P & 11 O/P) USING VEE CONNECTED VT's, 2 LINE CT's AND A CORE BALANCE CT

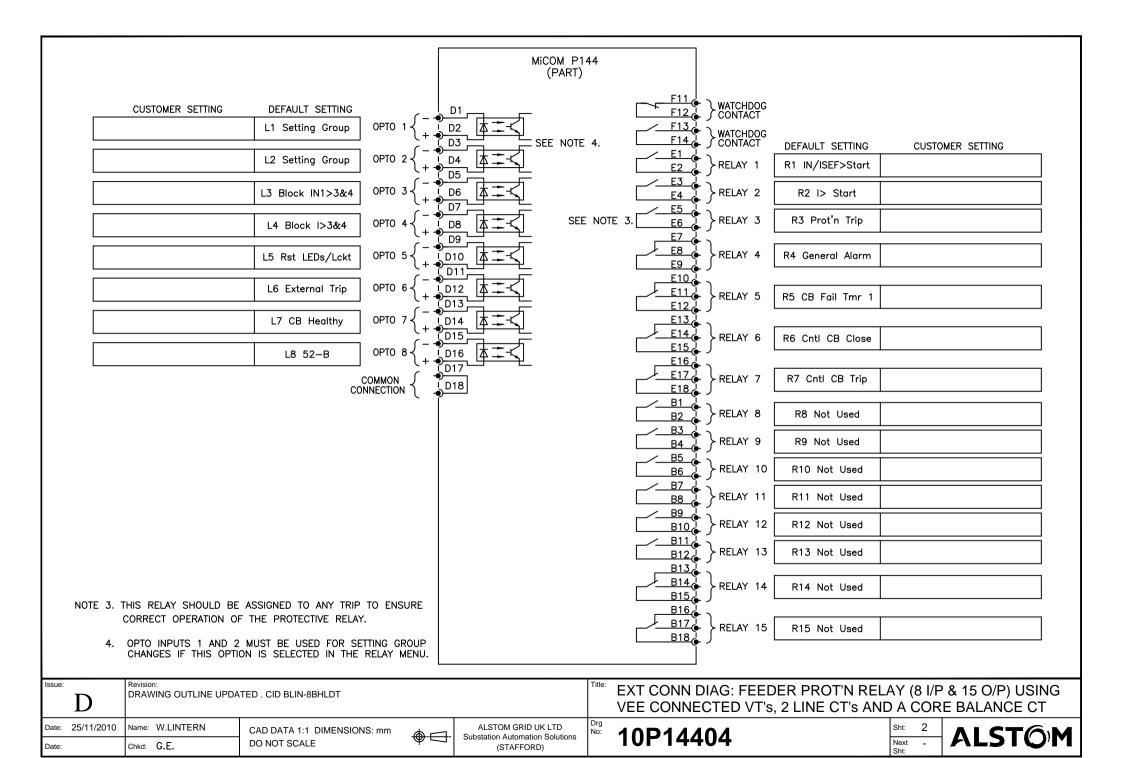
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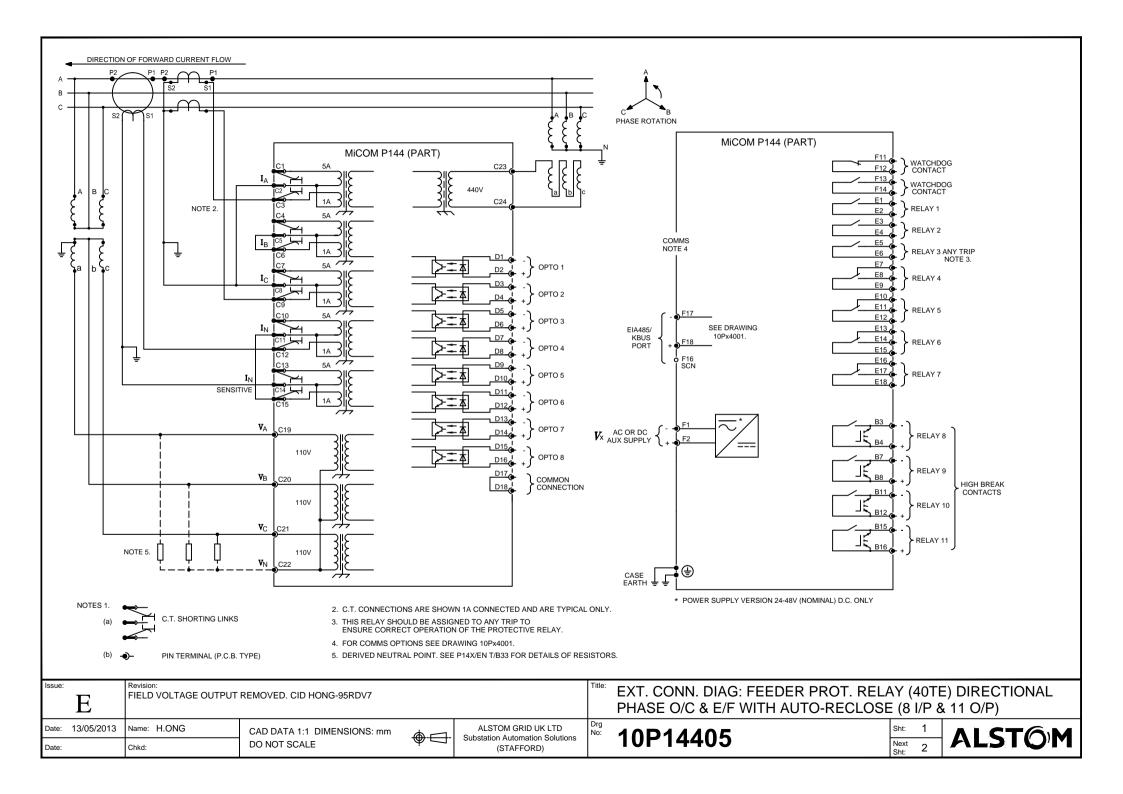
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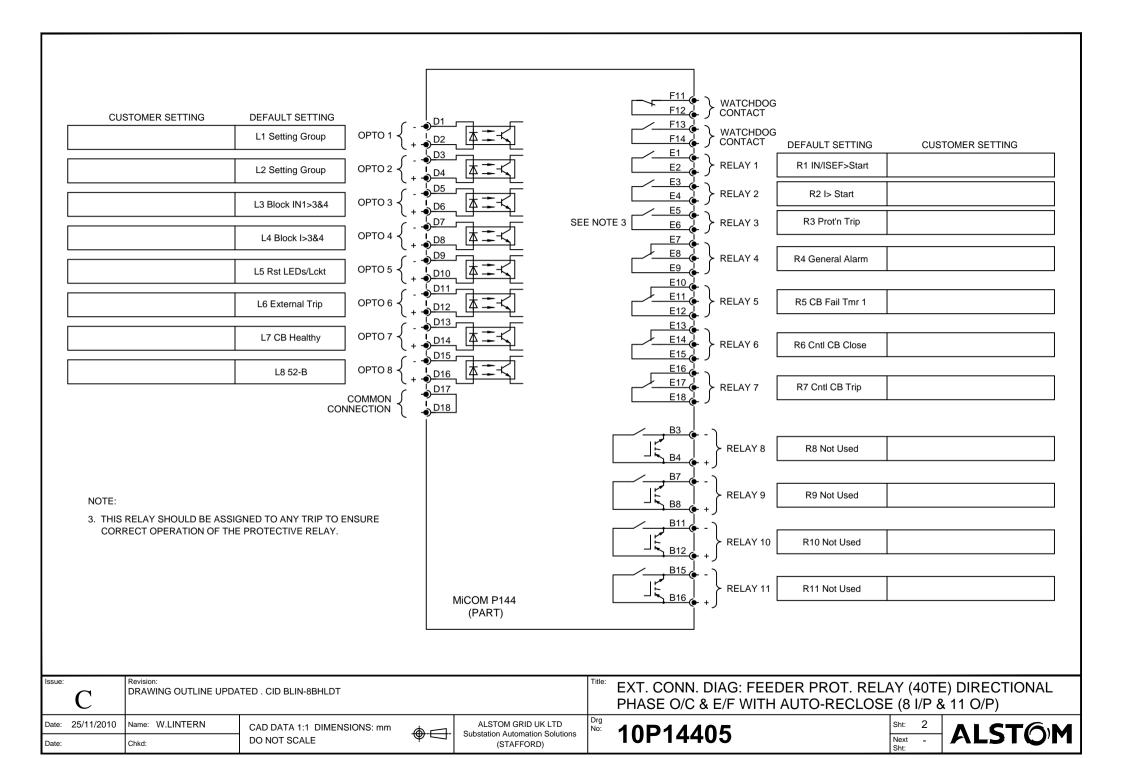


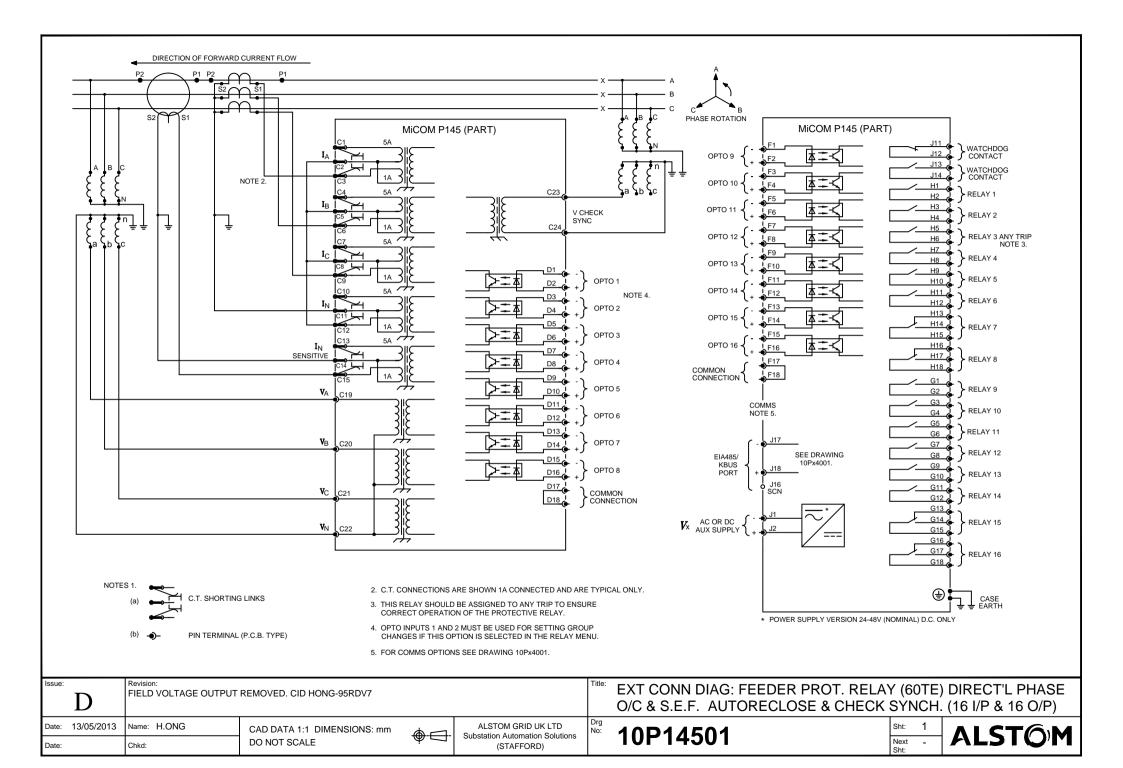


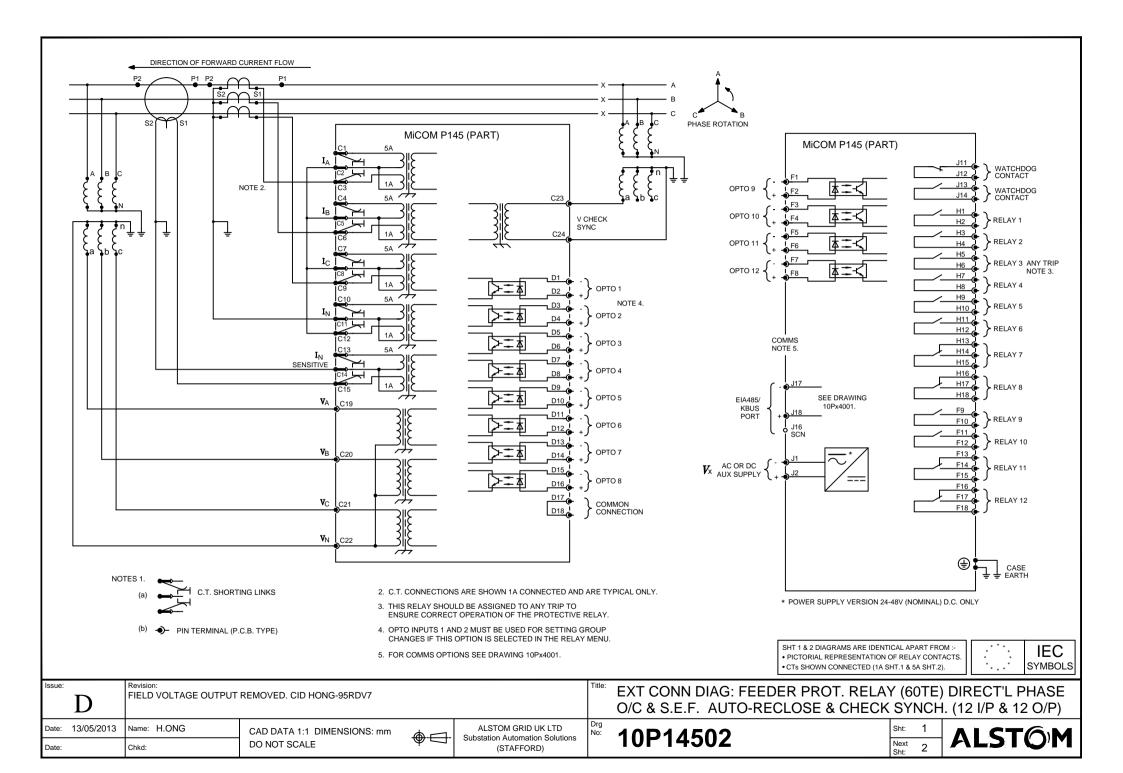


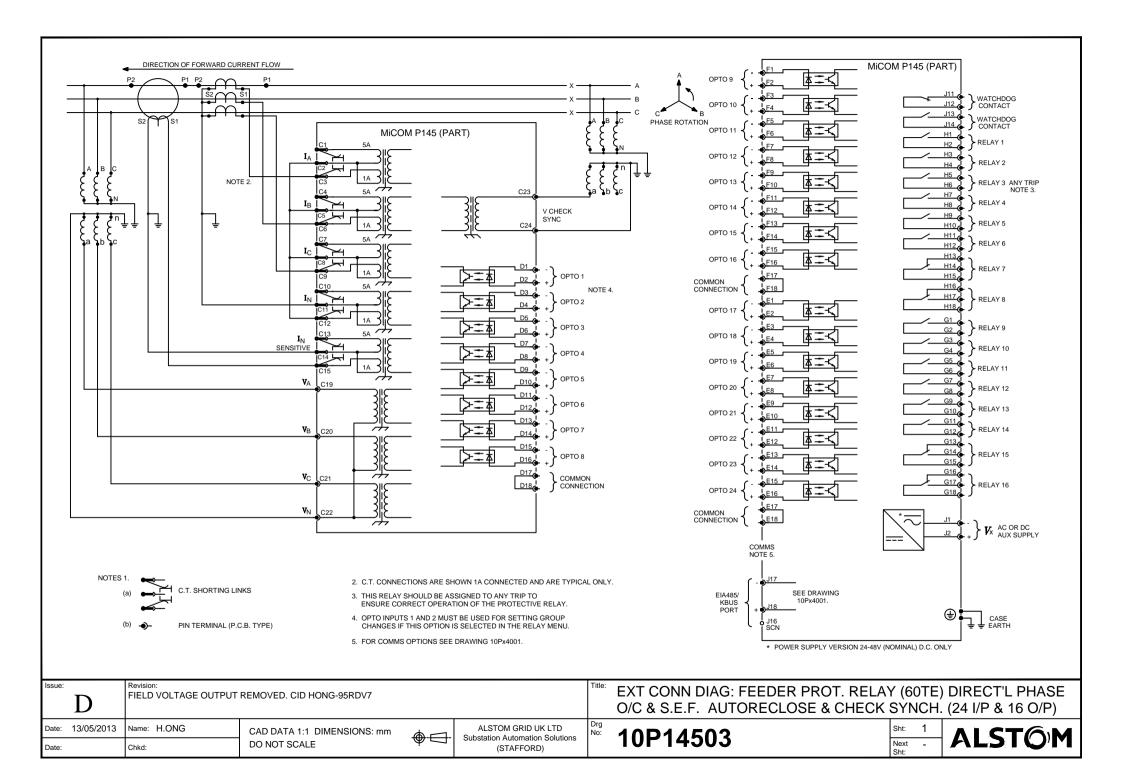


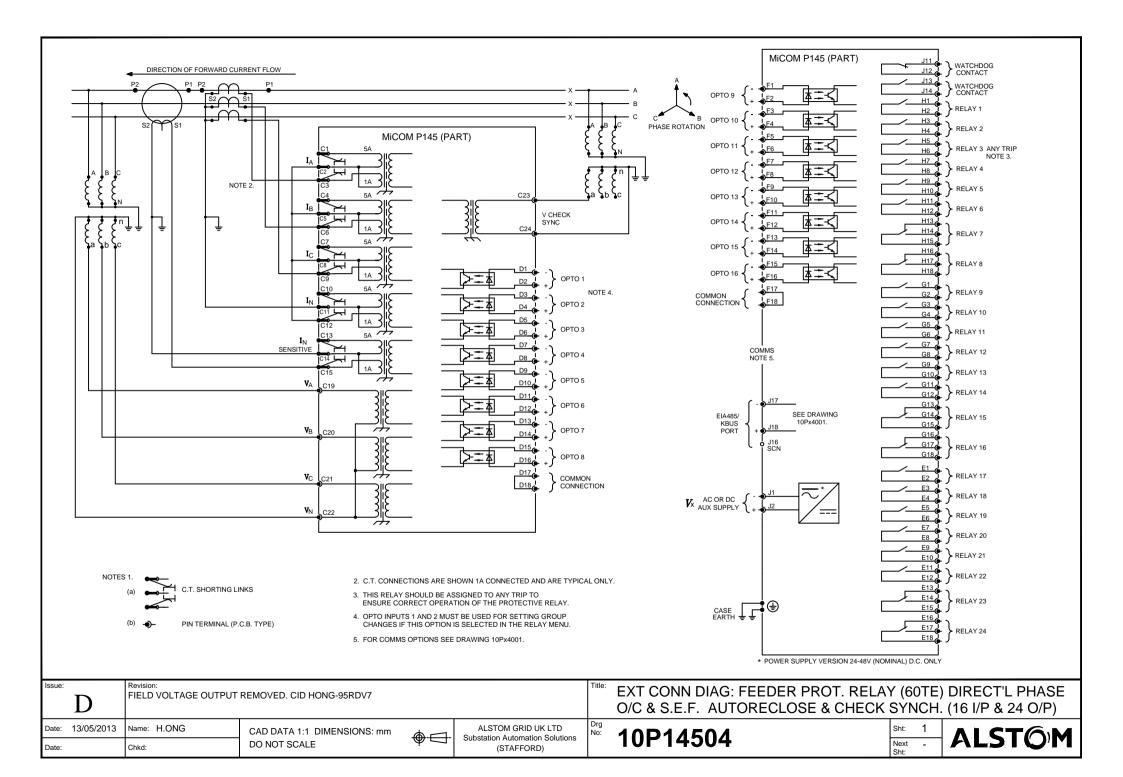


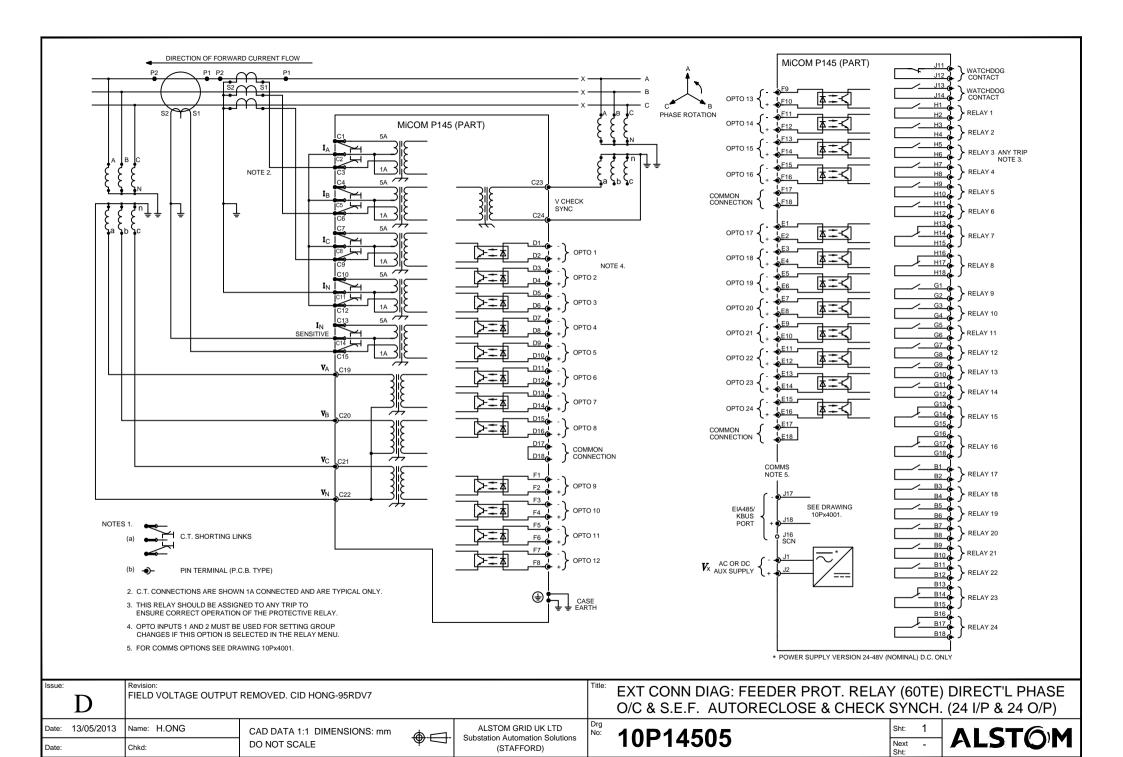


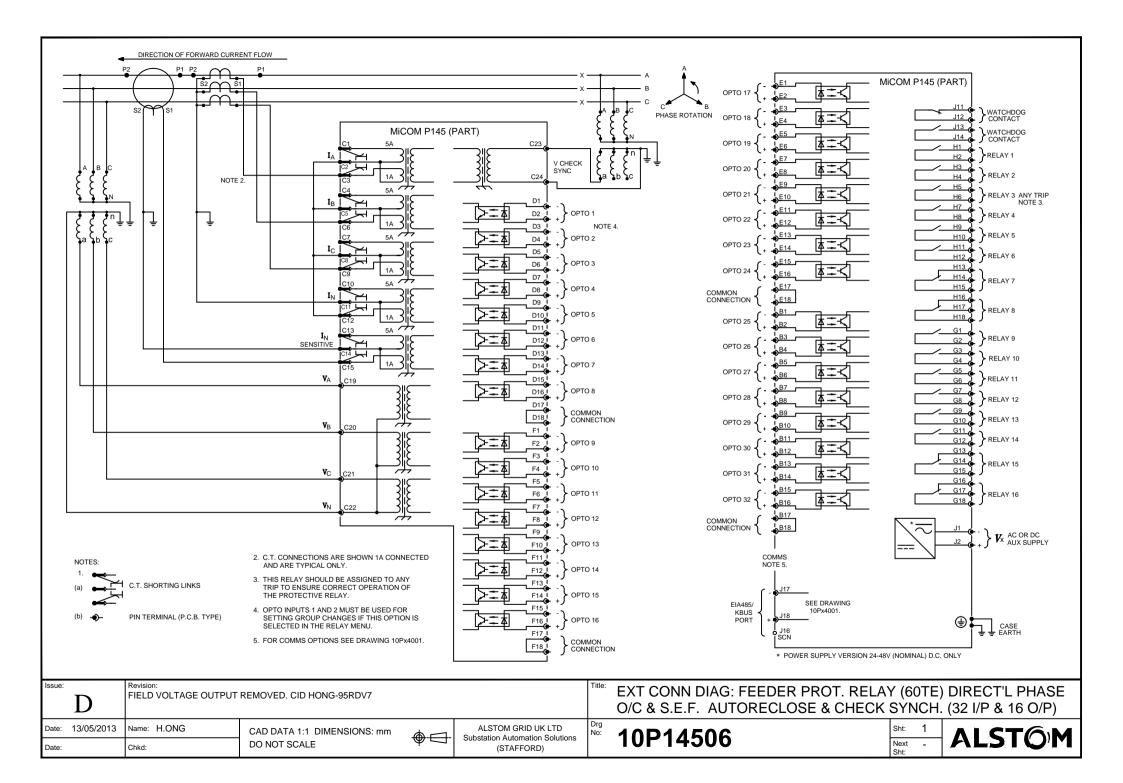


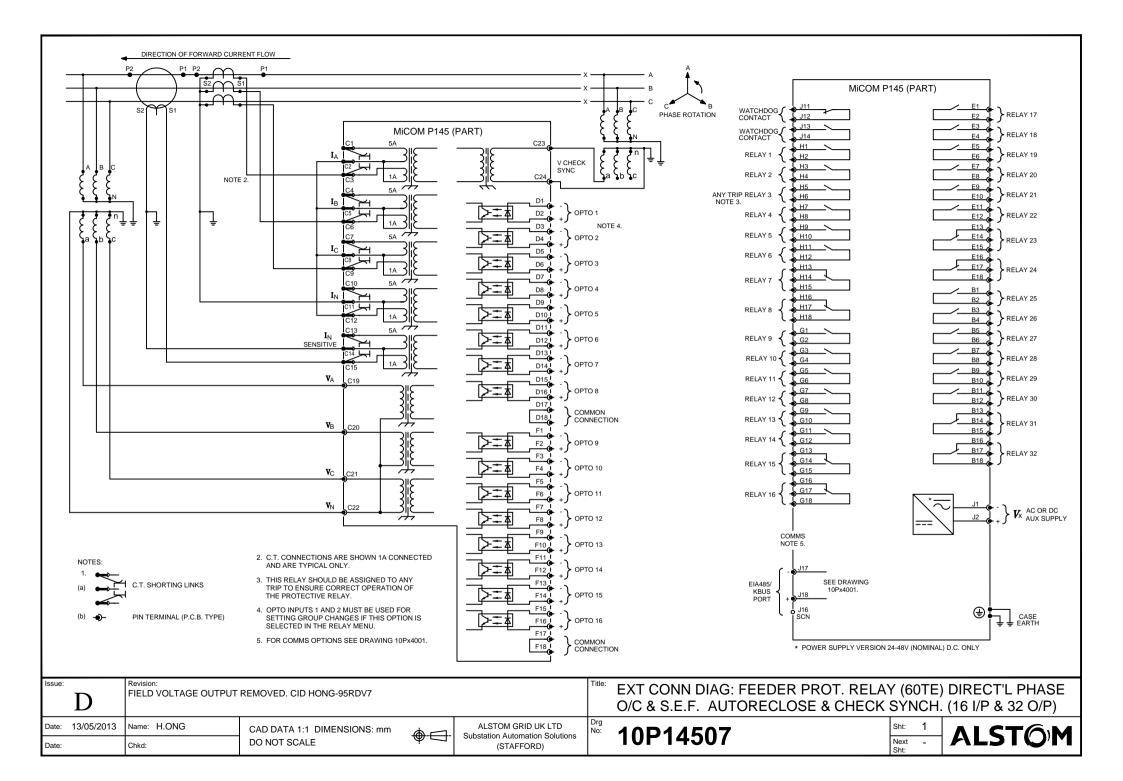


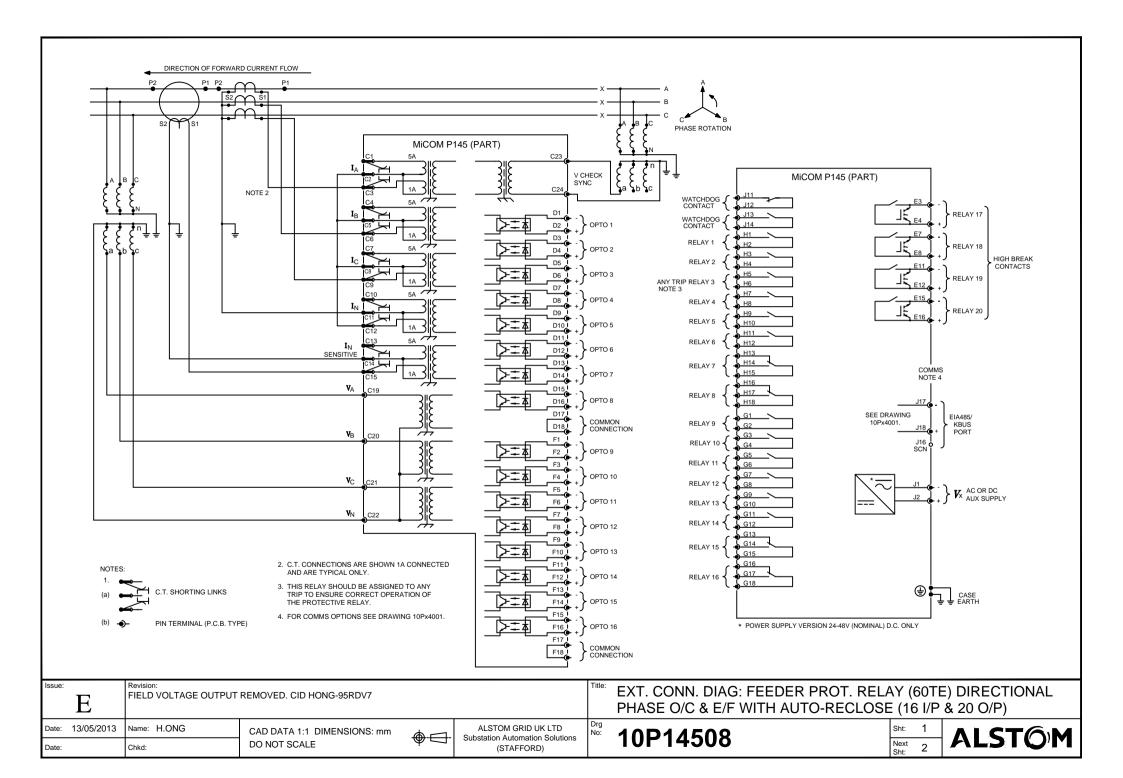


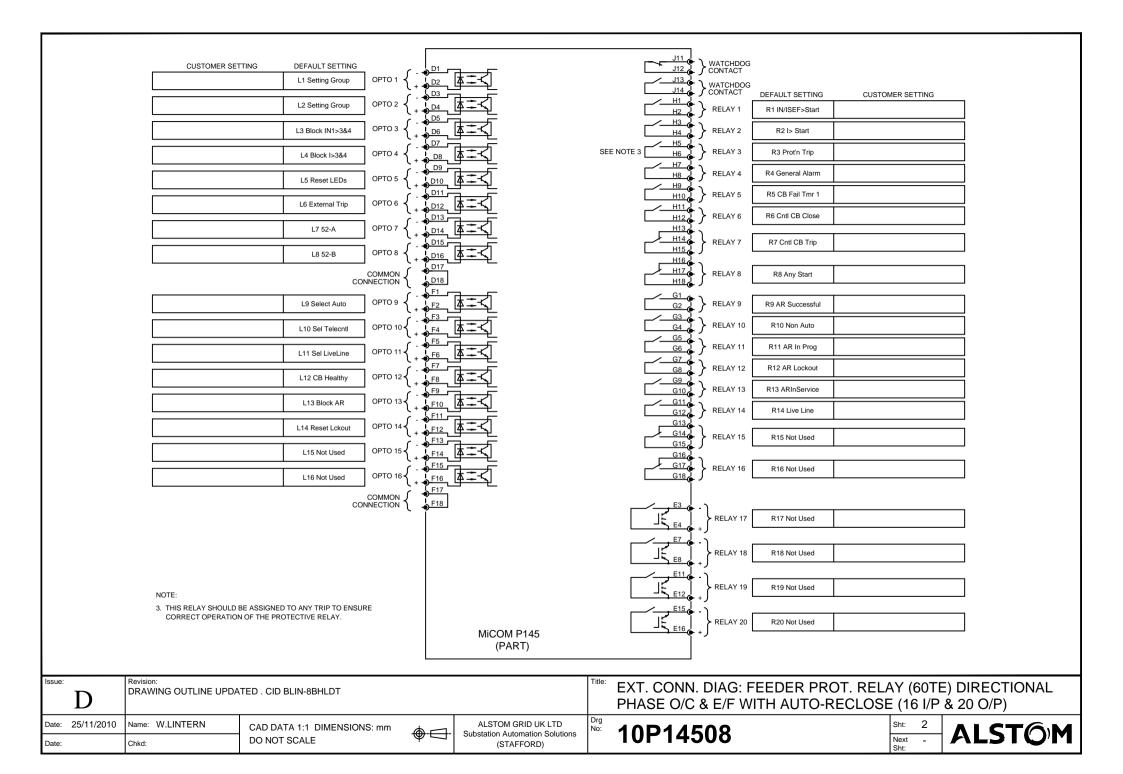


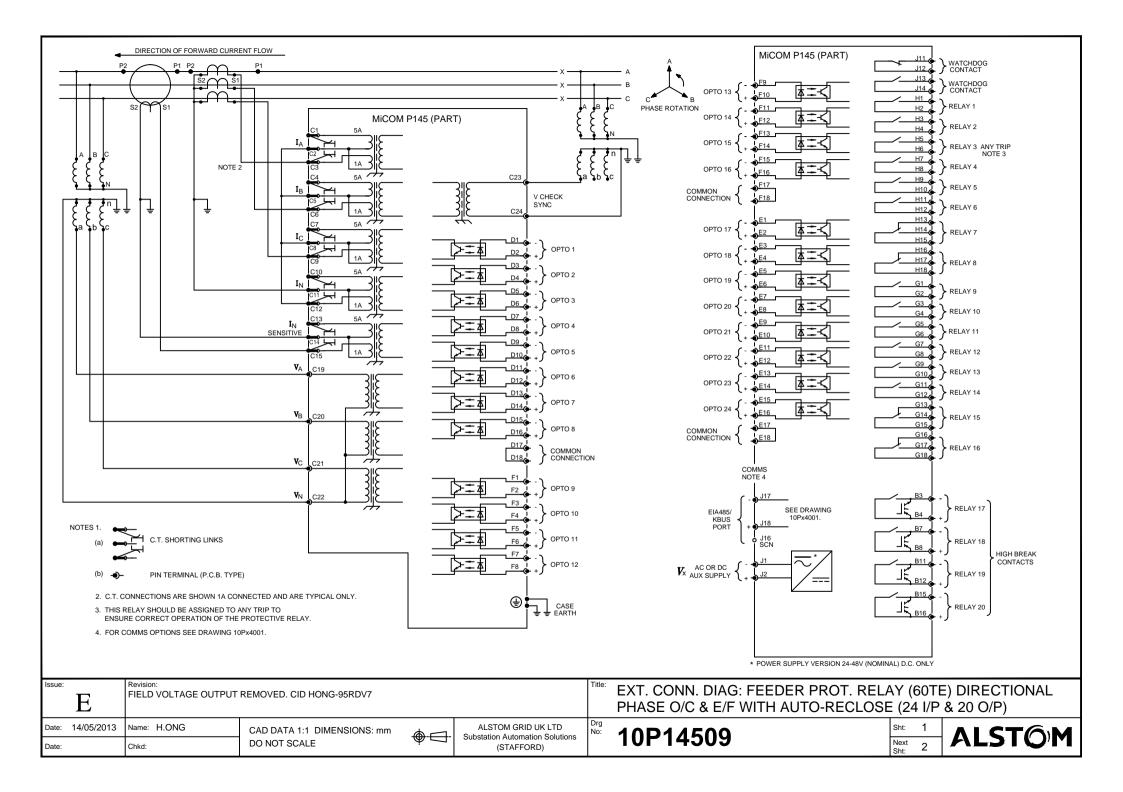


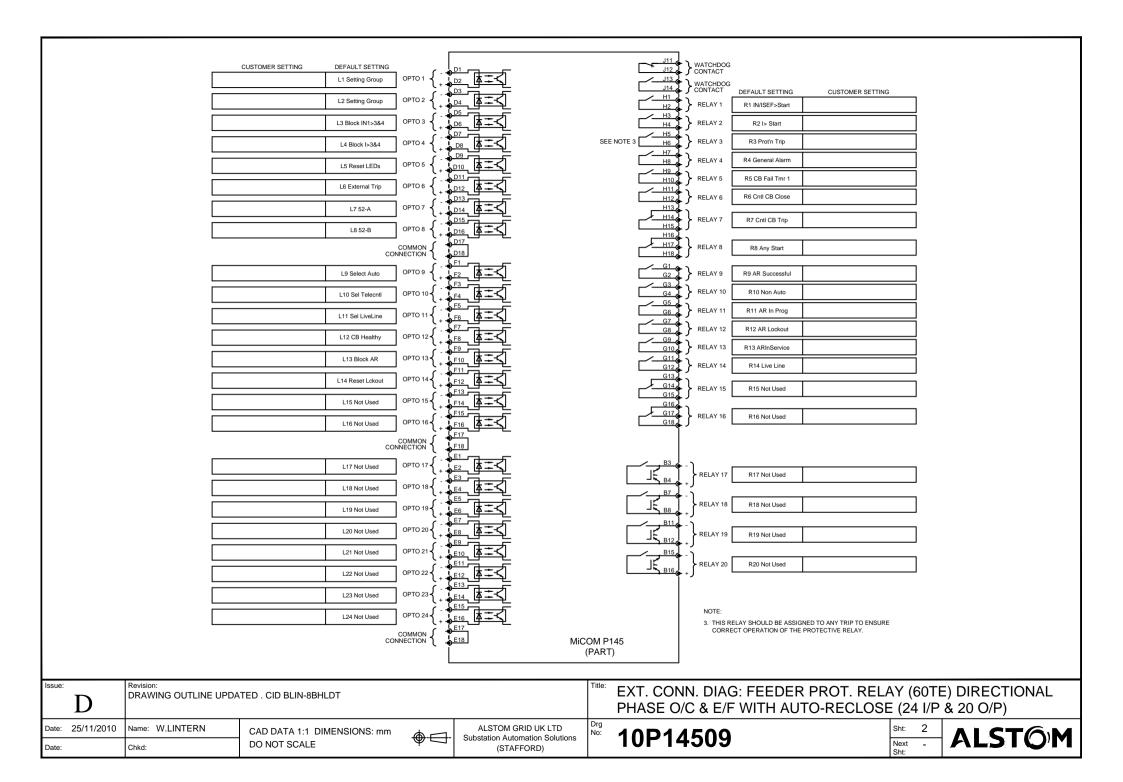


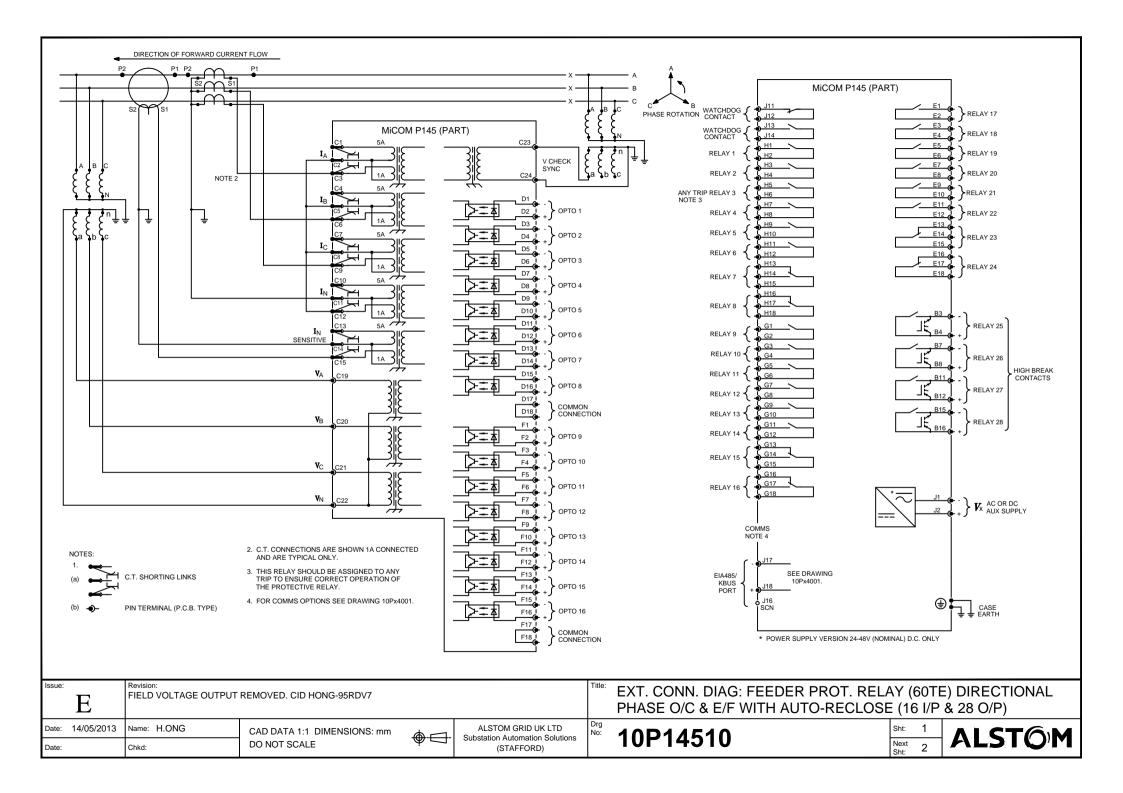


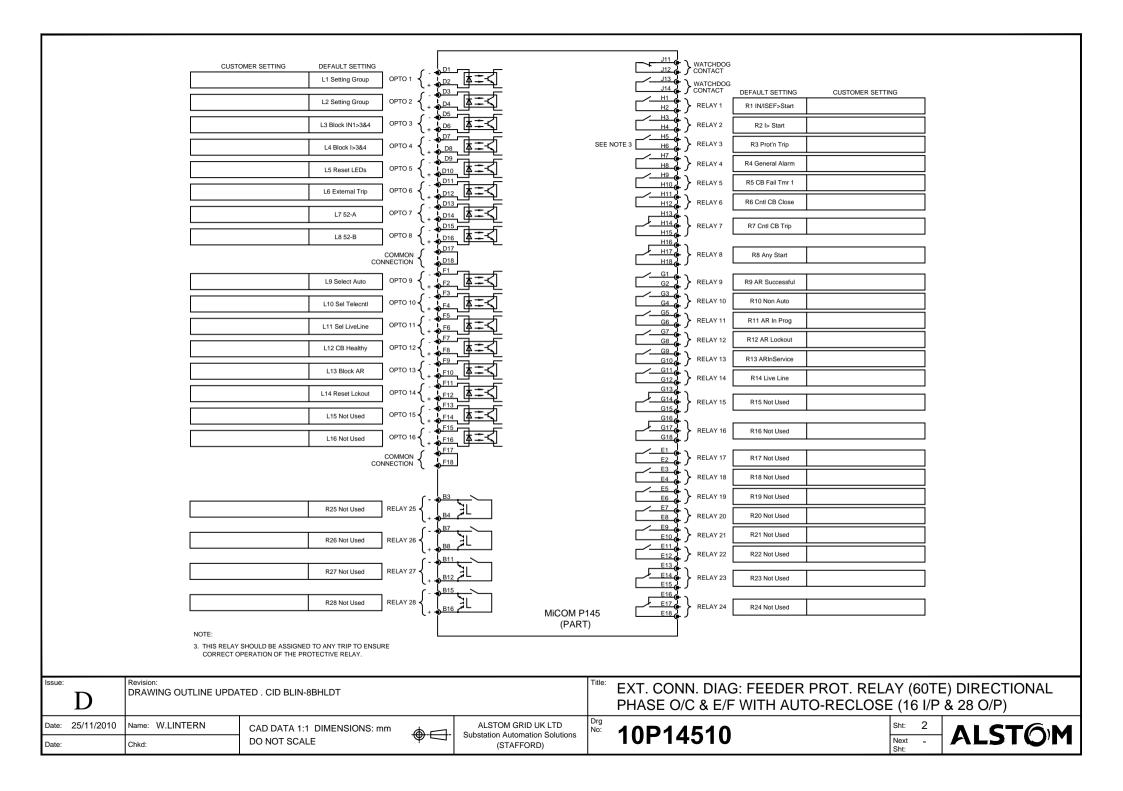


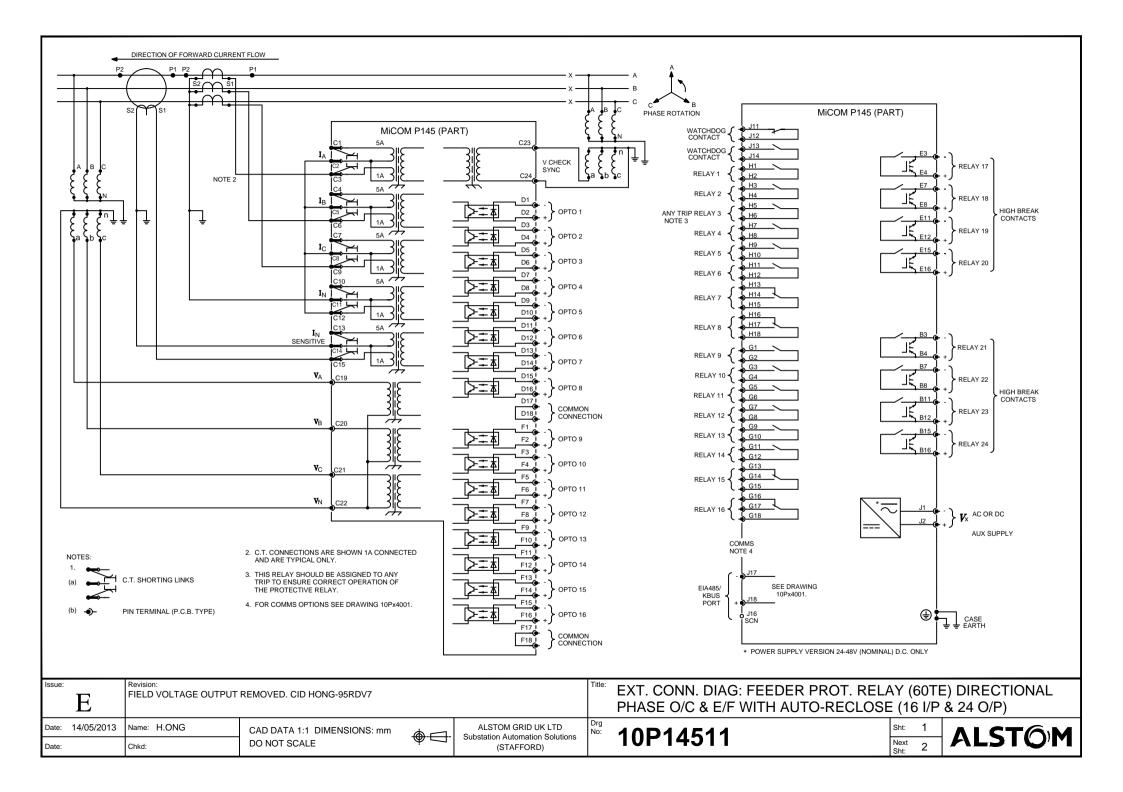


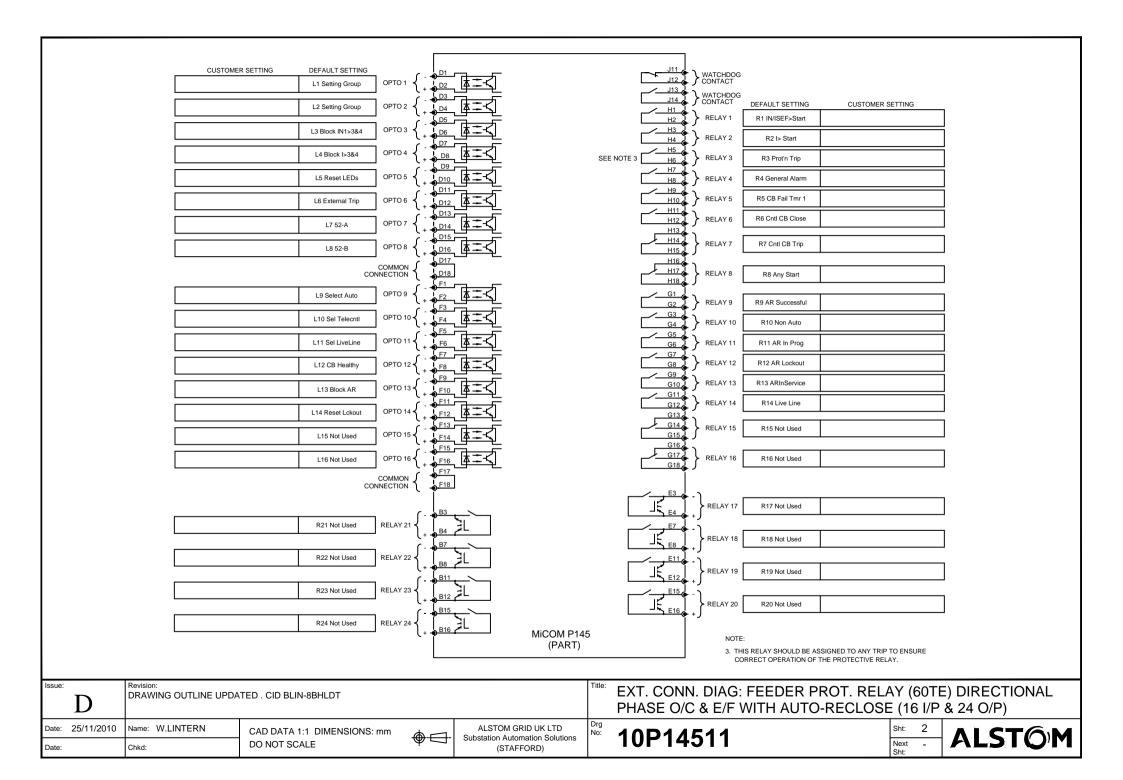














Imagination at work

Grid Solutions St Leonards Building Redhill Business Park Stafford, ST16 1WT, UK +44 (0) 1785 250 070 www.gegridsolutions.com/contact

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